PS29FS001

1 Mb (128K x 8) Ultra High-Speed Boot Sector Flash Memory

FEATURES

- **Ultra High-Performance FLASH Memory**
  - **25, 35 & 45 ns Read Access**
  - **Eliminates Need for Shadow-RAM**
- **Single Voltage Operation**
  - **Single 2.7 - 3.6V Supply Voltage**
  - **Maximum Supply Current < 15mA**
  - **Maximum Standby Current < 10µA**
- **Flexible Sector Architecture**
  - **One 64K x 8 Sector**
  - **One 32K x 8 Sector**
  - **One 16K x 8 Sector**
  - **Two 8K x 8 Sectors**
- **Top or Bottom Boot Sector Available**
- **Fast Erase and Write Cycles**
  - **2ms Page Write Cycle**
  - **20ms Page Erase Cycle**
  - **500ms Sector Erase Cycle**
- **Internal Program/Erase Controller**
  - **Automatic Program/Erase Timing**
  - **Data Polling and Toggle Bit Support**
- **Easy System Operation**
  - **Low-Voltage CMOS I/O Compatibility**
  - **Standard JEDEC Flash Pinouts**
  - **Standard JEDEC Software Commands**
- **High Reliability Technology**
  - **Endurance: >100,000 Cycles**
  - **Data Retention: >20 Years**
  - **ESD Protection: >2,000V**
- **Available Packages**
  - **32-Pin DIP**
  - **32-Pin TSOP**

PRODUCT DESCRIPTION

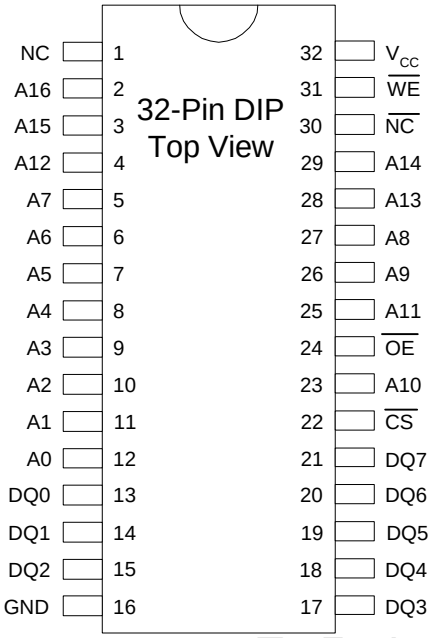
The PS29FS001 is a very high-speed CMOS FLASH Memory providing a total of 1Mb of storage. The device is organized as 128K words of 8 bits each. The device operates on a single 2.7V - 3.6V power supply, and is optimized for use in high-performance applications where very fast memory access is essential. The PS29FS001 offers exceptional access times as fast as 25nS. This allows the designer to eliminate the SRAM typically used, and operate fast processors and controllers directly from FLASH memory with zero wait-states.

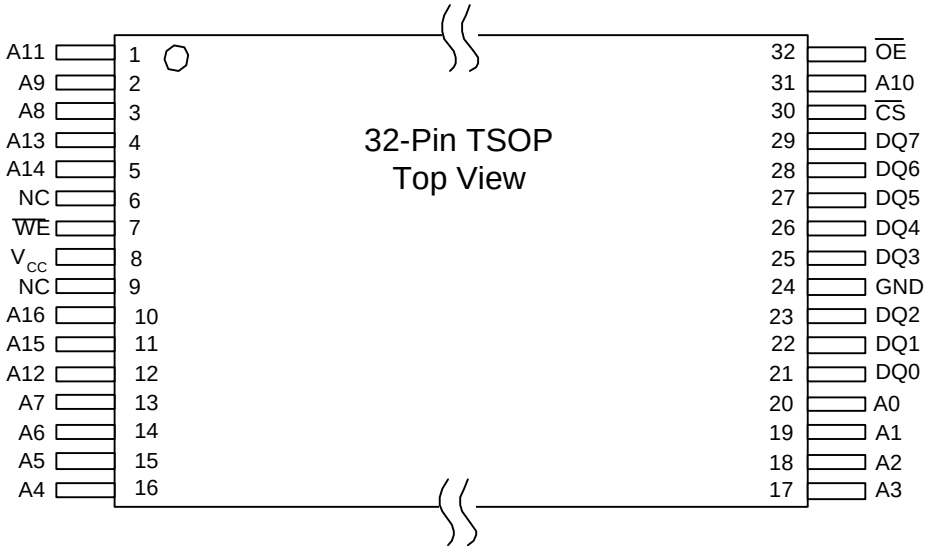
The memory is organized into multiple sectors. Each sector can be erased and reprogrammed without changing the data in other sectors. There is one 64K byte sector, one 32K byte sector, one 16K byte sector, and two 8K byte sectors. These smaller sectors are usually used to store boot code. Versions are available with the boot sector at either the top or bottom of the address map to support a variety of microprocessor protocols.

Device operations are simple, with an internal program/erase controller handling all of the internal operations needed. The device operates from a single supply voltage and supports both the regulated and unregulated voltage range. No external high voltage is needed for program or erase operations. The PS29FS001 is compatible with the JEDEC standard software command set.

The PS29FS001 provides a minimum endurance of 100,000 cycles and minimum data retention of 20 years. It comes in the JEDEC standard FLASH memory pinout, and is available in a variety of package types, including the standard 32-pin DIP and the high-density 32-pin TSOP package.

CONNECTION DIAGRAMS





PIN DESCRIPTIONS

Address (A_0–A_{16}) (Input)

These inputs provide the memory addresses. For sector operations addresses A_{16}–A_{14} are used to select the desired sector. For page operations addresses A_{16}–A_8 select the desired page. The address inputs are equipped with a Schmitt trigger and a narrow pulse filter (<50ns) for improved noise suppression.

Data (DQ_0–DQ_7) (Input/Output)

During Read cycles data is output to these pins. During Write cycles, these pins are used for the input data to be stored in the device. The serial clock controls the serial bus timing for data. When $\overline{OE}$ or $\overline{CS}$ are HIGH the data pins are placed into high-impedance mode.

Chip Select ($\overline{CS}$) (Input)

The Chip Select input is an active LOW input, and is used to enable the device for all operations. When $\overline{CS}$ is HIGH the device goes into a low power standby mode and the data outputs are placed into high-impedance mode.

Output Enable ($\overline{OE}$) (Input)

The Output Enable input is an active LOW input, and is used to enable or disable the output buffers on the Data pins. When $\overline{OE}$ is HIGH the data outputs are placed into high-impedance mode.

Write Enable ($\overline{WE}$) (Input)

The Write Enable input is an active LOW input, and is used to enable or disable normal write operations. If $\overline{WE}$ is held HIGH all write operations are disabled and the memory array is protected. If $\overline{WE}$ is LOW new data can be written into the device.

Reset ($\overline{RESET}$) (Input)

The Reset input is an active LOW input, and provides the means for a hardware reset of the device. When $\overline{RESET}$ is HIGH the device is in standard operation mode. When $\overline{RESET}$ is LOW any operation in progress is halted, and all data pins are placed into high-impedance mode. The internal controller is also reset, such that when $\overline{RESET}$ is again HIGH the device returns to the Read or Standby mode.

DEVICE OPERATION

The PS29FS001 is designed for easy operation. READ mode is straightforward, using the $\overline{CS}$, $\overline{OE}$, and $\overline{WE}$ pins to control the device. WRITE (Program) and ERASE modes are controlled by the use of command sequences. This ensures that data in the device will not be inadvertantly altered.

TABLE 1. OPERATING MODES

Operation	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Addresses	DQ
Read	L	L	H	H	A_{IN}	D_{OUT}
Write (Program)	L	H	L	H	A_{IN}	D_{IN}
Standby	H	X	X	H	X	High-Z
Write Protect	X	X	H	H	X	High-Z/D_{OUT}
Write Protect	X	L	X	H	X	D_{OUT}
Erase	L	H	L	H	Page or sector address	X
Reset	X	X	X	L	X	High-Z

COMMAND SEQUENCES

Commands are sent to the PS29FS001 using standard microprocessor write timings. These commands are then stored in the internal command register, which drives the internal circuits controlling all program and erase operations. (The command register does not use any user addressable memory location, but is used to store the commands, along with the address and data needed to perform the specified operation.) This allows all operations to be internally self-timed. The PS29FS001 is compatible with the JEDEC standard Flash command set (Table 2).

Upon initial power-up the device will be in the READ or standby mode depending upon the state of the $\overline{CS}$, $\overline{OE}$, and $\overline{WE}$ inputs (see Table 1). In order to perform a PROGRAM or ERASE operation a series of command sequences are entered into the device. The command is written by pulling $\overline{WE}$ LOW while holding $\overline{CS}$ LOW and $\overline{OE}$ HIGH. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs last. The data is latched on the rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first. Note that the addresses used in the command sequence are not affected by entering the command sequence.

TABLE 2. SOFTWARE COMMAND SET

Command Sequence[1]	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
	Addr[2]	Data[3]	Addr[2]	Data[3]	Addr[2]	Data[3]	Addr[2]	Data[3]	Addr[2]	Data[3]	Addr[2]	Data[3]
Program	5555	AA	2AAA	55	5555	A0	WA[4]	Data				
Page-Erase	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	PA[5]	30
Sector-Erase	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[6]	50
Chip-Erase	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Software-ID	5555	AA	2AAA	55	5555	90						
ID Exit[7]	XX	F0										
	5555	AA	2AAA	55	5555	F0						

Notes: (1) All Address and Data values are specified in Hexadecimal format
(2) Address format A_{16}-A_0 (Hex), Address A_{17} is "Don't Care" for Command sequence
(3) Data format DQ_7–DQ_0 (Hex).
(4) WA = Program word address
(5) PA for Page-Erase; uses address lines A_{16}–A_8
(6) SA, for Sector-Erase; uses address lines A_{16}–A_{14}
(7) Both Software ID Exit operations are equivalent

READ OPERATIONS

No command sequence is needed for READ operations. To access device data, the $\overline{WE}$ pin is held HIGH, while the $\overline{CS}$ and $\overline{OE}$ pins are LOW. Data stored at the addressed memory location will be output on the Data pins. When either $\overline{CS}$ or $\overline{OE}$ are HIGH the Data pins will be placed into high-impedance mode.

ERASE OPERATIONS

The PS29FS001 provides the user with the ability to erase the memory on a page-by-page, sector, or chip basis. There are a total of 1024 pages in the device, with a uniform page size of 1K bits. There are a total of 5 sectors in the device, with sizes ranging from 64K to 512K .

Page-Erase Operation

The Page-Erase operation requires a six-byte command sequence. The Page-Erase command (30H) and page address are latched in the last bus cycle. The page erase will begin following the rising edge of $\overline{WE}$ on the sixth cycle. The erase operation is internally self-timed, and no additional control signals are needed. Any additional commands issued during the erase operation are ignored. The end of the Page-Erase operation can be determined by using either the Data Polling or Toggle Bit methods.

Sector-Erase Operation

The Sector-Erase operation requires a six-byte command sequence. The Sector-Erase command (50H) and sector address are latched in the last bus cycle. The sector erase will begin following the rising edge of $\overline{WE}$ on the sixth cycle. The erase operation is internally self-timed, and no additional control signals are needed. Any additional commands issued during the erase operation are ignored. The end of the Sector-Erase operation can be determined by using either the Data Polling or Toggle Bit methods.

Chip-Erase Operation

The PS29FS001 also supports Chip-Erase, which allows the user to easily erase the entire memory in a single operation.

The Chip-Erase operation is started with a six-byte command sequence. The Chip-Erase command (10H) and a dummy address (5555H) are latched in the last bus cycle. The erase will begin following the rising edge of $\overline{WE}$ on the sixth cycle. The erase operation is internally self-timed, and no additional control signals are needed. Any additional commands issued during the erase operation are ignored. The end of the Chip-Erase operation can be determined by using either the Data Polling or Toggle Bit methods.

PROGRAM OPERATIONS

The PS29FS001 is programmed on a word-by-word basis. The Program operation requires a four-byte command sequence. The first two bytes indicate a valid command sequence. The third byte contains the Program command (A0H). The fourth byte contains the target word address and data to be written. The target address is latched on the falling edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs last. The data to be written is latched on the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first. The rising edge of $\overline{CS}$ or $\overline{WE}$ also starts the actual internal program operation. The Program operation is internally self-timed, and no additional control signals are needed. Any additional commands issued during the Program operation are ignored. The end of the Program cycle can be determined by using either the Data Polling or Toggle Bit methods.

ERASE/PROGRAM STATUS DETECTION

Two different techniques are available to determine the status of a Program or Erase operation. Use of the Data Polling (DQ_7) or Toggle Bit (DQ_6) technique will allow the system to minimize total write cycle time.

Data Polling (DQ_7)

During an Erase operation, the status of the operation can be determined by reading the state of the DQ_7 pin. When the erase is in progress, the device will output a LOW(0) on the DQ_7 pin. After the Erase operation has finished the device will output a HIGH(1) on the DQ_7 pin. The Data Polling function is valid as soon as the Erase operation begins.

Similarly, the status of a Program operation can be determined by reading the state of the DQ_7 pin. During the Program operation, the value present on the DQ_7 pin will be the complement of the actual data programmed on DQ_7. After the Program operation has finished the value present on the DQ_7 pin will be the data programmed on DQ_7. The Data Polling function is valid as soon as the Program operation begins.

Toggle Bit (DQ_6)

During an Erase or Program operation, the status of the operation can also be determined by evaluating the data present on the DQ_6 pin. If the operation is still in progress, successive read operations (to any address) will result in the data on the DQ_6 pin toggling between HIGH(1) and LOW(0). When the operation has completed, the DQ_6 pin will stop toggling. The Toggle Bit function is valid as soon as the Erase or Program operation begins.

PRODUCT IDENTIFICATION

The PS29FS001 supports both hardware and software modes for manufacturer and device identification. The hardware mode is primarily designed to be used by device programming equipment to ensure the correct programming algorithm has been selected. This mode requires a voltage outside the normal operating range (V_{HH}) to be applied to address pin A_9. The manufacturer and device ID codes can then be read on pins DQ_0–DQ_7.

The software mode can be used to identify the device when it is in a system. The Software-ID operation requires a three-byte command sequence. (See Table 2). The first two bytes indicate a valid command sequence. The third byte contains the Software-ID command (90H). Once the Software-ID operation has been initiated the data may be read any number of times. A read operation at address 0000H will return the Manufacturer ID Code. A read operation at address 0001H will return the Device ID code. (See **Table YY**).

To return to normal device operation an ID-Exit operation must be performed. The ID-Exit operation also serves as a device reset, and can be used to return the PS29FS001 to read mode in case of any abnormal operation. As shown in Table 2, the ID-Exit operation can be either a one-byte or three-byte command sequence, with the final byte containing the ID-Exit command (F0H). The ID-Exit operation will always return the device to read mode.

Absolute Maximum Ratings

Operating Temperature ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... -0.5V to V_{CC} + 0.5V
Maximum Operating Voltage 4.0V
DC Output Current 50mA

Recommended Operating Range

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Operating Temperature	0	70	°C

NOTICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliablity.

DC CHARACTERISTICS (Over Recommended Operating Range)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage		-0.5		0.8	V
V_{IH}	Input HIGH Voltage		0.7xV_{CC}		V_{CC}+0.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA, V_{CC} = V_{CC} min.			0.4	V
V_{OH1}	Output HIGH Voltage	I_{OH} = –2mA, V_{CC} = V_{CC} min.	0.85xV_{CC}			V
V_{OH2}	Output HIGH Voltage	I_{OVL} = –100µA, V_{CC} = V_{CC} min.	V_{CC}–0.2			V
V_{HH}	Supervoltage for Auto Select	$\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} V_{CC} = 2.5V	11.5	12.0	12.5	V
I_{LI}	Input Leakage Current	GND < V_{IN} < V_{CC}, V_{CC} = V_{CC} max.			1	µA
I_{LO}	Output Leakage Current	GND < V_{OUT} < V_{CC}, V_{CC} = V_{CC} max.			1	µA
I_{LH}	Supervoltage Leakage Current	$\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} V_{CC} = V_{CC} max., A_9 = V_{HH} max.			30	µA
I_{CC}	Active Supply Current[1] Read Program/Erase	f = f_{max} $\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, V_{CC} = V_{CC} max. $\overline{CS}$ = $\overline{WE}$ = V_{IL}, $\overline{OE}$ = V_{IL}, V_{CC} = V_{CC} max.			 15 15	mA mA mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}, V_{CC} = V_{CC} max.			10	µA

Notes: (1) Address Inputs at V_{IL} or V_{IH}.

Pin Capacitance T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Test Conditions	Max.	Units
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$[2]	Input/Output Capacitance	V_{IN} = 0V	10	pF

Notes: (2) This parameter is characterized and periodically sampled

AC CHARACTERISTICS (Over Recommended Operating Range)

Read Operations

Symbol		Parameter	–25		–35		–45		Units
Std.	JEDEC		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	t_{AVAV}	Read Cycle Time	25		35		45		nS
t_{AA}	t_{AVQV}	Address Access Time		25		35		45	nS
t_{CE}	t_{ELQV}	Chip Enable Access Time		25		35		45	nS
t_{OE}	t_{GLQV}	Output Enable Access Time		15		25		35	nS
t_{CLZ}	t_{ELQX}	Chip Enable to Output Active	0		0		0		nS
t_{OLZ}	t_{GLQX}	Output Enable to Output Active	0		0		0		nS
t_{CHZ}	t_{EHQZ}	Chip Enable to Output High-Z		15		25		35	nS
t_{OHZ}	t_{GHQZ}	Output Enable to Output High-Z		15		25		35	nS
t_{OH}	t_{AXQX}	Output Hold Time	0		0		0		nS

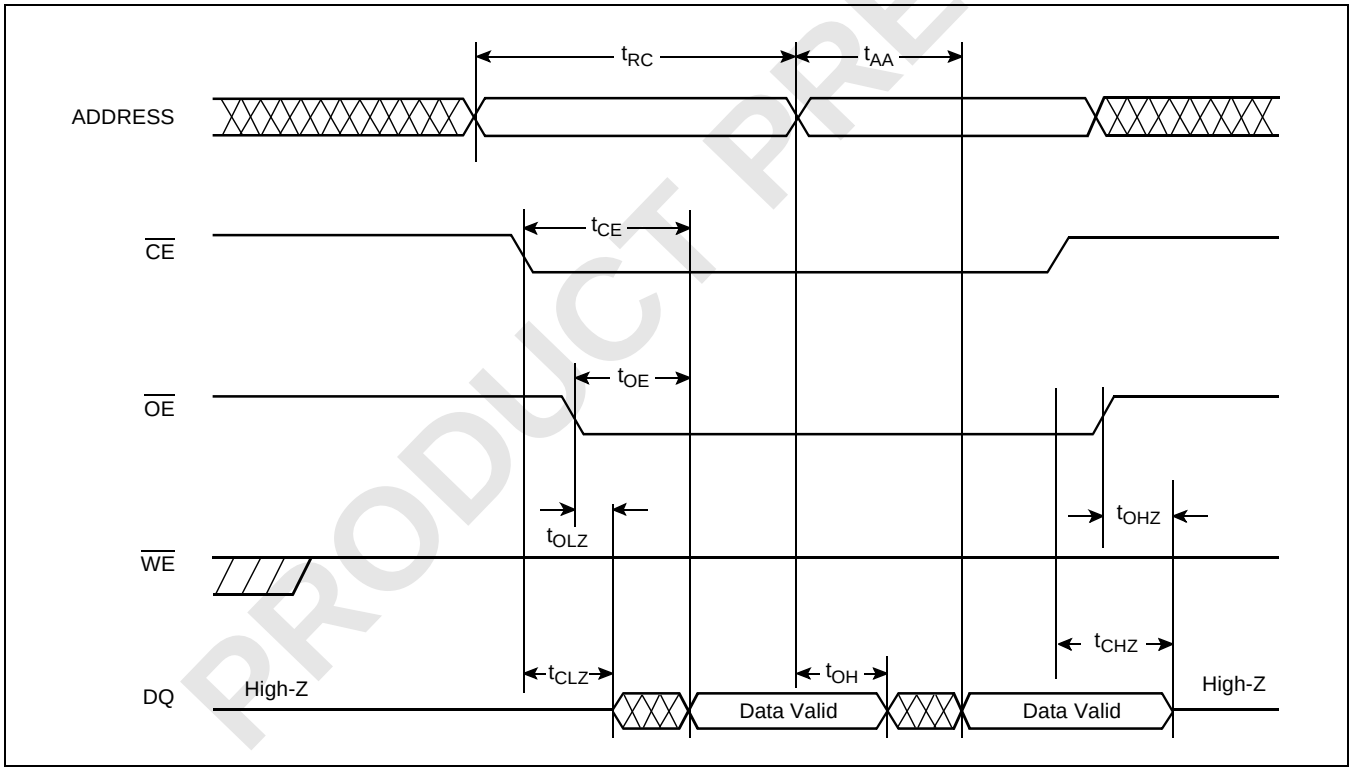
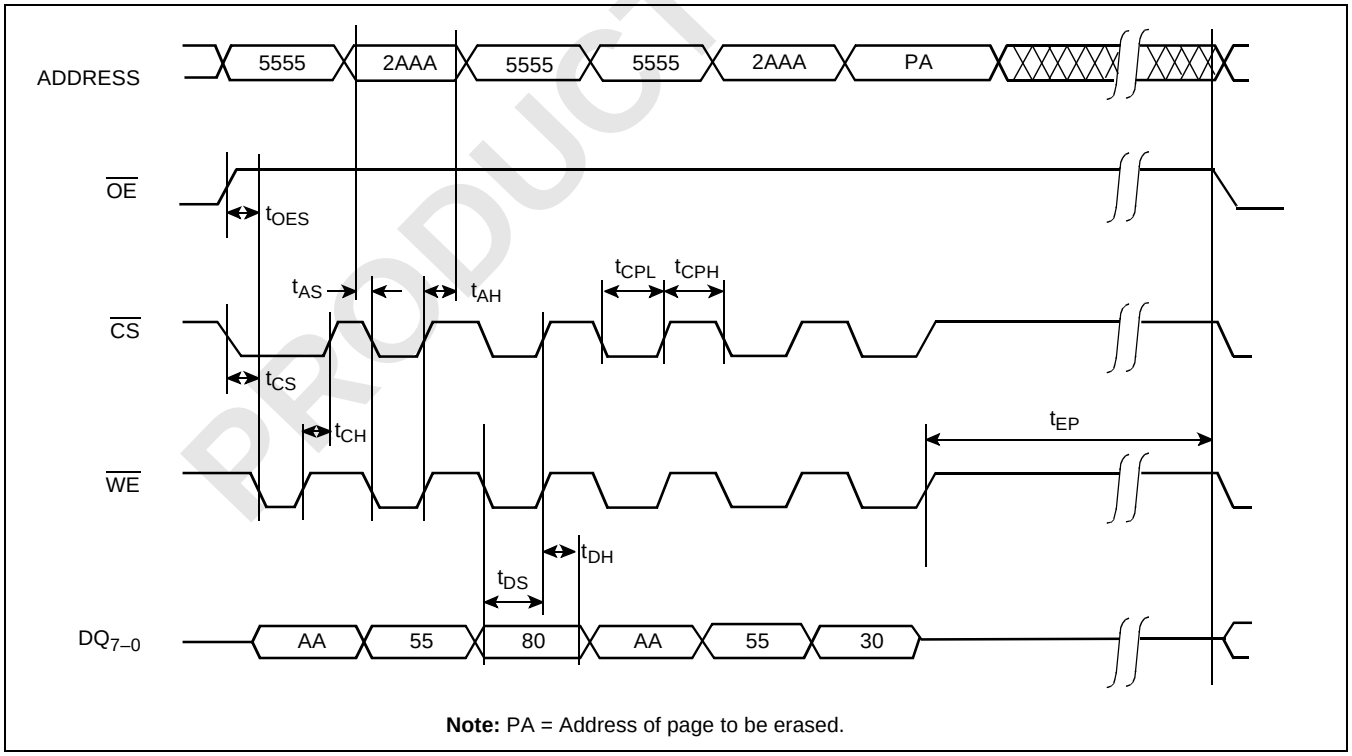


FIGURE 1. READ CYCLE TIMING DIAGRAM

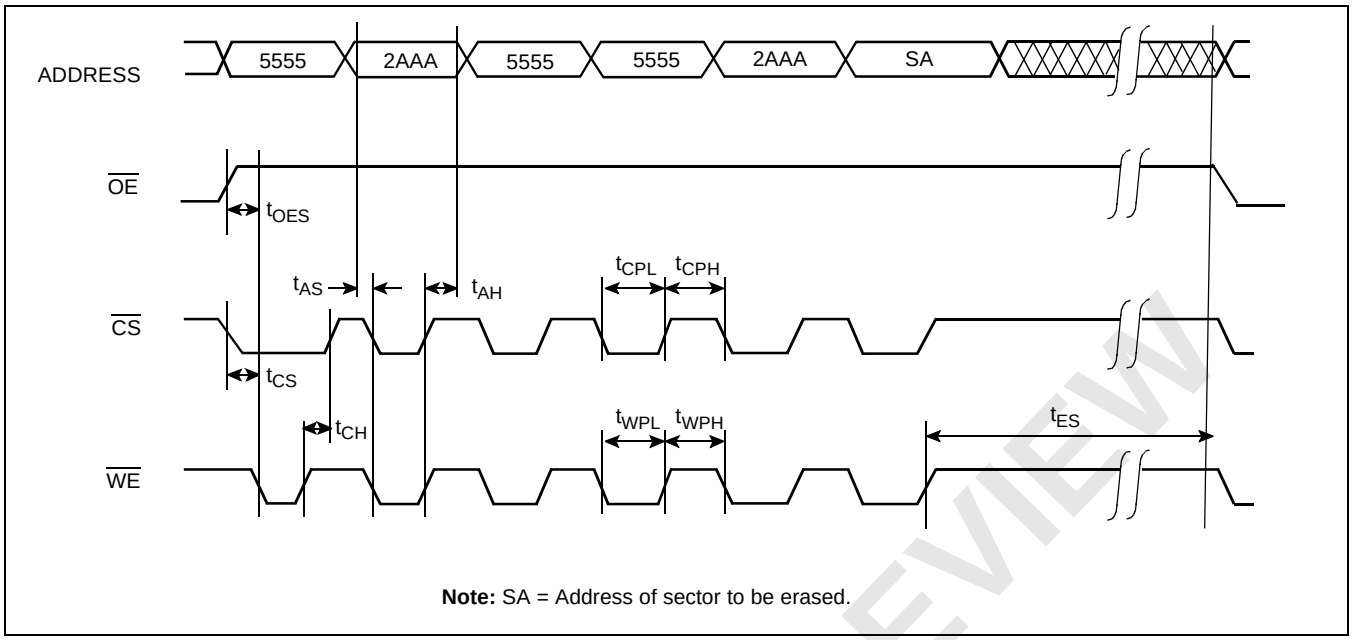
Erase/Program Operations

Symbol		Parameter	-25		-35		-45		Units
Std.	**JEDEC**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{AS}	t_{AVWL}	Address Setup Time	0		0		0		nS
t_{AH}	t_{WLAX}	Address Hold Time	15		25		30		nS
t_{DS}	t_{DVWH}	Data Setup Time	15		25		30		nS
t_{DH}	t_{WHDX}	Data Hold Time	0		0		0		nS
t_{CS}	t_{ELWL}	Chip Enable Setup Time	0		0		0		nS
t_{CH}	t_{WHEH}	Chip Enable Hold Time	0		0		0		nS
t_{OES}	t_{GHWL}	Output Enable Setup Time	0		0		0		nS
t_{OEH}	t_{GLWH}	Output Enable Hold Time	0		0		0		nS
t_{CPL}	t_{ELEH}	Chip Enable LOW Pulse Width	15		20		25		nS
t_{CPH}	t_{EHEL}	Chip Enable HIGH Pulse Width	10		15		20		nS
t_{WPL}	t_{GLGH}	Output Enable LOW Pulse Width	15		20		25		nS
t_{WPH}	t_{GHGL}	Output Enable HIGH Pulse Width	10		15		20		nS
t_{EP}		Page Erase Time	10		10		10		mS
t_{ES}		Sector Erase Time	200		200		200		mS
t_{EC}		Chip Erase Time	500		500		500		mS
t_{WP}		Word Program Time		10		10		10	µS



Note: PA = Address of page to be erased.

FIGURE 2. PAGE-ERASE TIMING DIAGRAM



Note: SA = Address of sector to be erased.

FIGURE 3. SECTOR-ERASE TIMING DIAGRAM

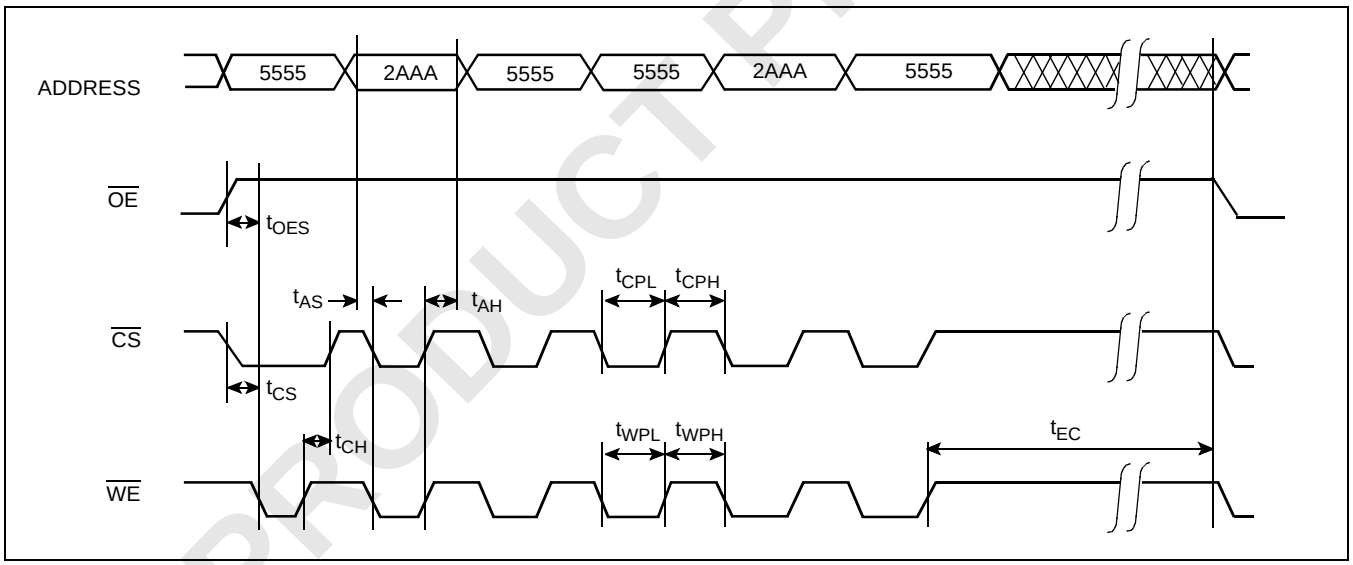
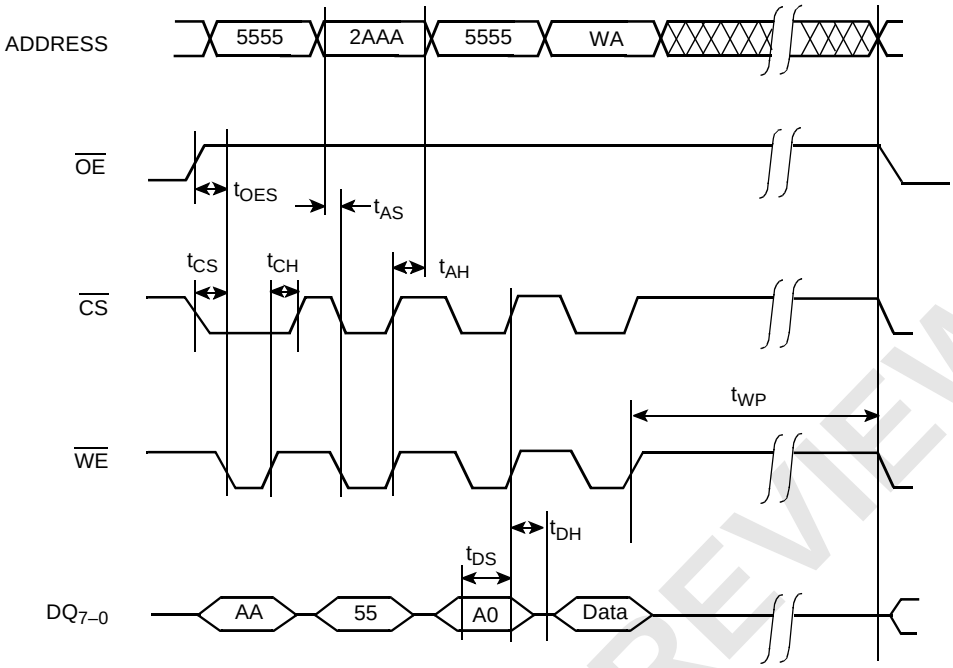


FIGURE 4. CHIP-ERASE TIMING DIAGRAM



Note: WA = Address of word to be programmed.

FIGURE 5. WORD-PROGRAM TIMING DIAGRAM

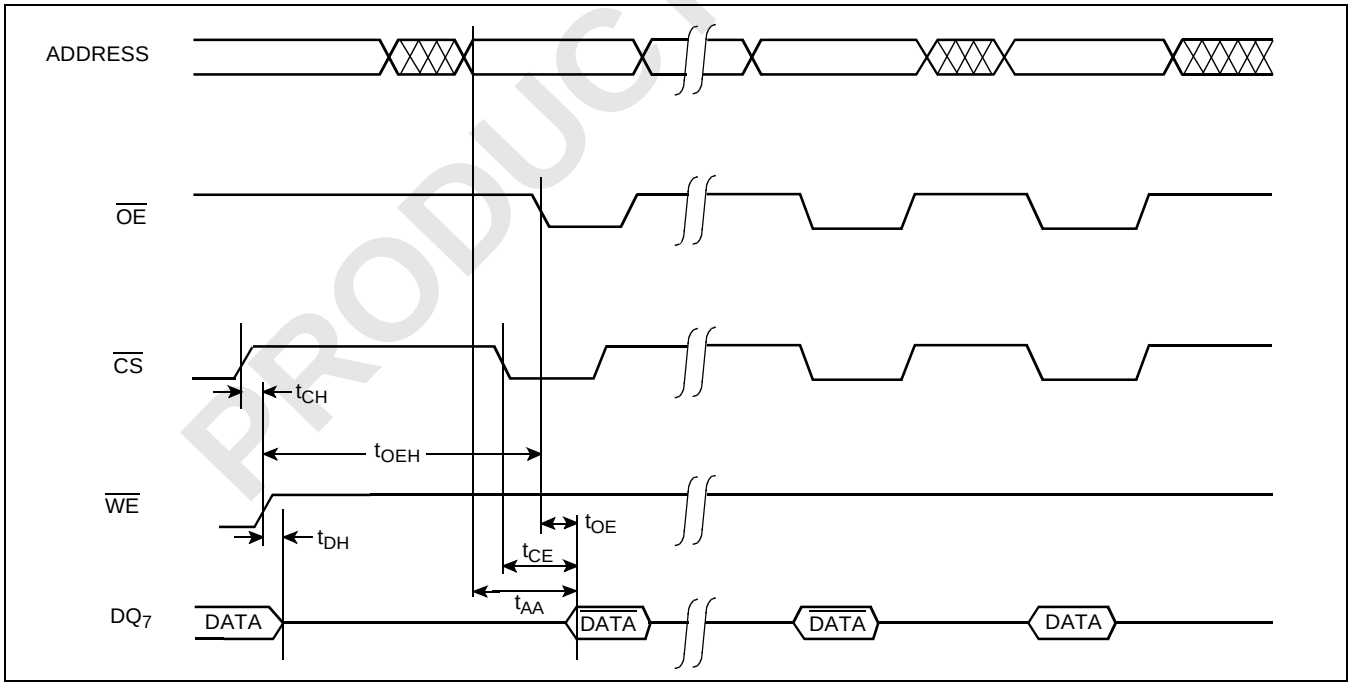
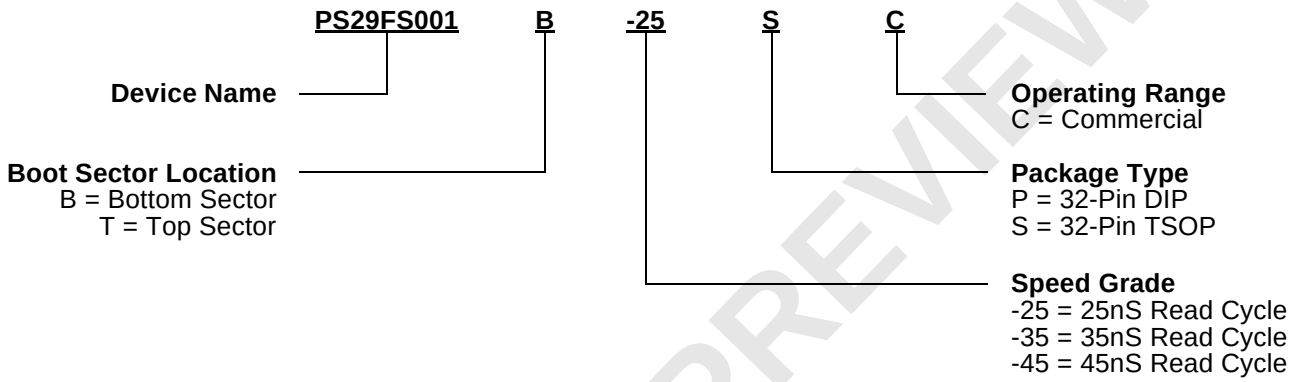


FIGURE 6. $\overline{\text{DATA}}$ POLLING TIMING DIAGRAM

PACKAGING INFORMATION

PACKAGING INFORMATION

ORDERING INFORMATION



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