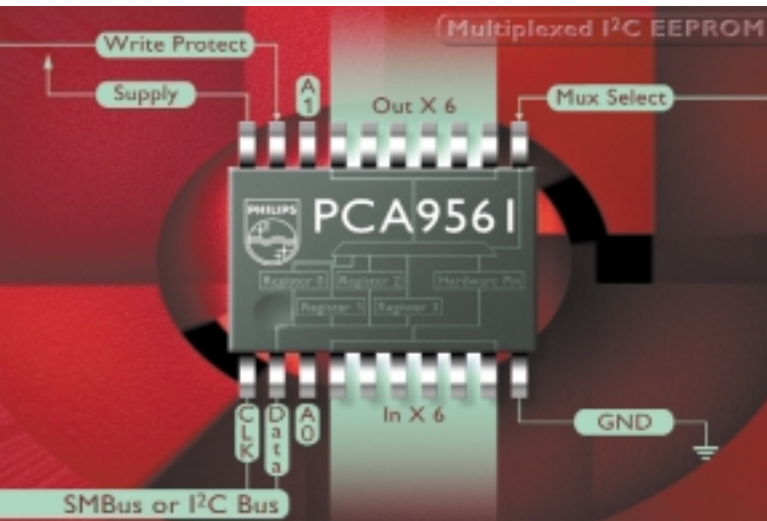


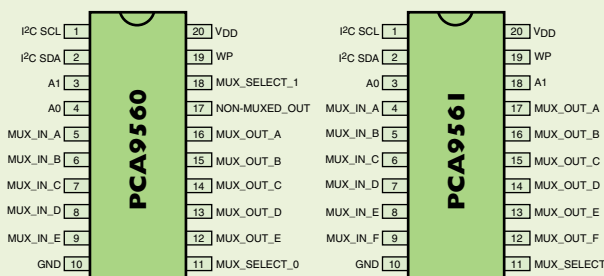


Philips Configuration System Management ICs

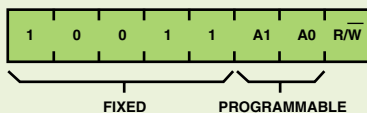


The PCA9560 supports Mobile and Desktop VID Configuration, where 3 preset values (2 sets of internal non-volatile registers and 1 set of external hardware pins) set processor voltage for operation in either performance, deep sleep or deeper sleep modes. The PCA9561 provides five sets of 6-bit values (4 internal and 1 external) offering 2 additional settings.

Pin Configurations



I2C Slave Address



PCA9560 and PCA9561

Selection Guide

	Nb of non-volatile registers	Nb of register bits	Nb of hardware input pins	Nb of muxed outputs	Non-muxed outputs
PCA9560	2	6	5	5	Yes
PCA9561	4	6	6	6	No

Order Information

Package	Container	PCA9560	PCA9561
SO	Tube	PCA9560D	PCA9561D
	T&R	PCA9560D-T	PCA9561D-T
TSSOP	Tube	PCA9560PW	PCA9561PW
	T&R	PCA9560PW-T	PCA9561PW-T

PCA9560

Dual 5-bit Multiplexed
1-bit Latched
I2C/SMBus EEPROM

PCA9561

Quad 6-bit
Multiplexed
I2C/SMBus EEPROM

Description

The PCA9560 is a 20-pin CMOS device with a dual 5-bit 3-to-1 multiplexer and 1-bit latch, while the PCA9561 is a 20-pin CMOS device with a quad 6-bit 5-to-1 multiplexer. Both devices enable DIP switch-free or jumper-less system configuration. They both have 2 address pins, allowing up to 4 identical devices to be placed on the same I2C bus or SMBus. They can be used for CPU VID (Voltage IDentification code) configuration, with the PCA9560 providing an additional non-multiplexed, latched output. The PCA9560 consists of two 6-bit non-volatile EEPROM registers, 5 hardware pin inputs and a 5-bit multiplexed output with one latched EEPROM bit. The PCA9561 consists of four 6-bit non-volatile EEPROM registers, 6 hardware pin inputs and a 6-bit multiplexed output. Both products have an I2C/SMBus interface. SMBus or System Management bus is a specific implementation of the I2C protocol, widely used in mobile and desktop PC motherboard architecture.

In the VID configuration application, the PCA9560 or PCA9561 typically reside between the CPU and Voltage Regulator Module (VRM). They are used to bypass the CPU-defined VID values and provide a different set of VID values to the VRM, if a change in the CPU voltage is desired. An increase in CPU voltage combined with an increase in CPU frequency leads to a performance boost of up to 7.5%. Lower CPU voltage reduces power consumption. The main advantage of the PCA9560 over the older PCA9559 device is that it contains two internal non-volatile EEPROM registers instead of just one, allowing three independent settings (performance operation, deep sleep mode and deeper sleep mode) instead of only two (performance operation and deep sleep mode). The main advantage of the PCA9559/60/61 over the PCA8550 are their open-drain buffers which allow them to work with all generations of processors instead of only 2.5 V processors. The PCA9560 is footprint compatible and a drop-in replacement for the PCA9559, without any software modifications required. The PCA9561 offers the possibility to extend to 5 different settings (4 stored internally and 1 external) and allows a more accurate CPU voltage tuning depending on specific applications.

All multiplexed EEPROMs are also useful in server and telecom/networking applications when used to replace DIP switches or jumpers, where system settings can easily be changed via I2C/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.

PCA9560/61 Features

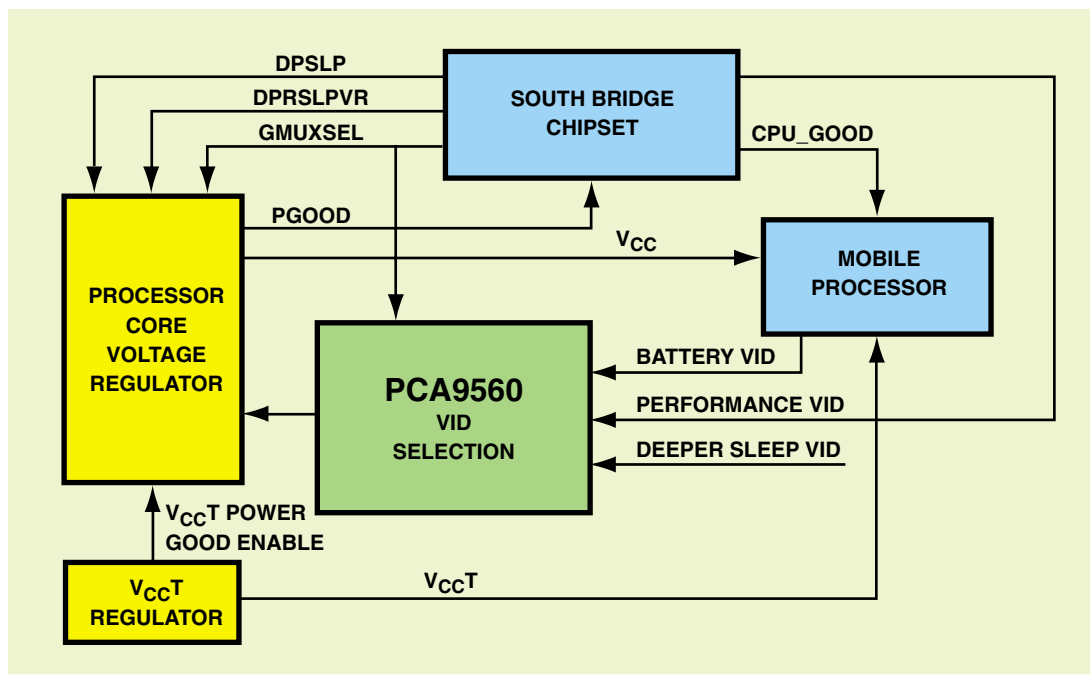
- Internal non-volatile EEPROM registers with a minimum of 3,000 write cycles and a minimum of 10 year memory cell data retention
- Internal non-volatile registers programmable and readable via I2C/SMBus
- Input hardware pins readable via I2C/SMBus
- Selection between input hardware pins and non-volatile EEPROM registers
- Write protect feature controls the ability to write to the non volatile EEPROM registers
- 2 address pins, allowing up to 4 identical devices on the I2C/SMBus
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- JEDEC Standard JESD78 Latch-up testing exceeds 100 mA
- Offered in 20-pin SO (D) and TSSOP (PW) packages

PCA9560/61 Operating Characteristics

- Operating voltage of 3.0 V to 3.6 V
- 5.0 V tolerant open drain outputs
- 5.0 V and 2.5 V tolerant inputs
- Operating temperature of 0 °C to 70 °C
- Operating frequency up to 400 kHz



VID Selection using the PCA9560



The PCA9559 was developed to support high volume programs for major computer OEMs in the Mobile and Desktop PC market segments. It extends the functionality of the existing PCA8550 from 4-bit to 5-bit, providing flexibility to utilize I²C/SMBus in wider bit system architectures.

The PCA9560 was developed to expand usage of the PCA9559 into Mobile and Desktop PC architecture even further, where three pre-set values (two internal EEPROM registers and the external hardware pins) provide processor settings for performance operation (AC Power), deep sleep mode and deeper sleep mode. The PCA9560 is footprint compatible and a drop-in replacement for the PCA9559, with no software modifications required. The PCA9559 has only one MUX_SELECT pin to choose between the MUX_IN values and the single non-volatile EEPROM register. Since the PCA9560 has two internal non-volatile EEPROM registers, if Register 1 values are left to all 0's (default condition) then the MUX_SELECT_1 pin

can function the same way as the PCA9559 OVERRIDE# pin and MUX_SELECT_0 pin can function the same way as the PCA9559 MUX-IN pin. The PCA9560 can read the MUX_IN_X values via I²C/SMBus, while the PCA9559 cannot perform this operation. Another difference is that the MUX_SELECT_X control pins can be overridden by I²C/SMBus. To replace the PCA9559 with the PCA9560, the function table for the MUX_OUT OUTPUTS and the NON_MUXED_OUT OUTPUT must stay the same and the MUX_SELECT pin functions should not be overridden via I²C/SMBus.

The PCA9561 is not backwards compatible with the PCA9559 or PCA9560 and is designed for applications where multiple independent 6-bit values need to be immediately available via the mux select for use in processor selection or simply as an I²C controlled DIP switch or jumper replacement.

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2800 Wells Branch Parkway
Mailstop P-411
Austin, Texas 78728
United States

Tel: +1 800 234 7381
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E-mail: P411webinq.smi@harte-hanks.com

Europe, Africa, Middle East and South America

Philips Semiconductors International
Fulfillment and Sales Support Center
P.O. Box 366
2700 AJ Zoetermeer
The Netherlands

Fax: +31 79 3685126

Asia Pacific

Philips Semiconductors Asia Pacific
Market Response Management Center
P.O. Box 68115
Kowloon East Post Office
Hong Kong

Fax: +852 2756 8271

Japan

Philips Semiconductors
Philips Building 13-37
Kohnan 2-chome
Minato-ku,
Tokyo 108-8507

Tel: +81 3 3740 5130
Fax: +81 3 3740 5057

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