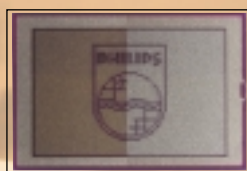


Philips Semiconductors announces PCF8811, 80 x 128 Display Driver using multiple row addressing algorithm MRA for optical enhancement

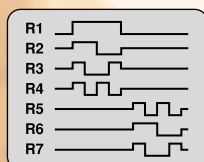
PCF8811: 80 x 128 Display Driver

DISPLAY PERFORMANCE

IAPT addressing



MRA addressing



MSD689

Features:

- Display size 80 rows, 128 columns
- Display data RAM 80 x 128 bits
- Low power consumption <0.3mW
- MRA multiple row addressing
- Power save mode

• Display features

- Better display contrast achieved by MRA technology.
- Icon row for up to 128 indicators.
- Partial display mode with mux 1:16 to 1:80.
It reduces power consumption.
- The MRA drive technique allows lower frame rates for power savings or use of higher frame rates for faster responding liquid crystals e.g. needed for animations.
Therefore the frame rate can be varied from 30 to 60 f/s.
- Number (p) of simultaneously driven rows is automatically set depending on multiplex rate.
- Temperature compensation.
8 linear gradients can be selected.

• Interfaces

- 8 bit parallel
- I²C-bus, up to 3.4MHz
- 3/4 line serial SPI, up to 9MHz
- 3 line serial, up to 9MHz

• Voltage ranges

- Logic supply: 1.5 to 3.3V
- Analog supply: 1.8 to 3.3V
- Display supply: 1.8 to 3.3V
- Display operation: up to 9V

• Architecture

- MRA multiple row addressing drive technique, P=2...8
- Row / column outputs can be configured: mirrored/swapped. This eases software architecture and cell lay-out for chip-on-glass or TCP assembly.
- Vertical or horizontal addressing.
- Mirroring in X and in Y.
- V^{LCD} generation: built-in voltage multiplier 2X...7X, no external charge pump capacitors.
- V^{LCD} can be calibrated on module level with patented OTP cells (one time programmable).

• Delivery form

- Chip with gold bumps in tray for chip-on-glass (COG) and chip-on-foil (COF,TCP) applications.

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