PEREGRINE SEMICONDUCTOR

ADVANCE INFORMATION

# PE4231

## SPDT High Power MOSFET RF Switch

### Features

- Optimized for 75-ohm systems
- Single +3-volt power supply
- Low insertion loss: 0.80 dB at 1.0 GHz
- High isolation: 44 dB at 1.0 GHz
- Typical input 1 dB compression point of +32 dBm
- Single-pin CMOS or TTL logic control
- Low cost

## Product Description

*The PE4231 SPDT High Power MOSFET RF Switch is designed to cover a broad range of applications from DC to 1.3 GHz. This single-supply reflective switch integrates on-board CMOS control logic driven by a simple, single-pin CMOS or TTL compatible control input. Using a nominal +3-volt power supply, a typical input 1 dB compression point of +32 dBm can be achieved. The PE4231 also exhibits input-output isolation of better than 44 dB at 1.0 GHz and is offered in a small 8-lead MSOP package.*

*The PE4231 SPDT High Power MOSFET RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.*

**Figure 1. Functional Schematic Diagram**

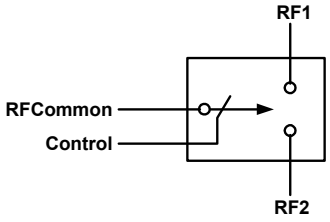


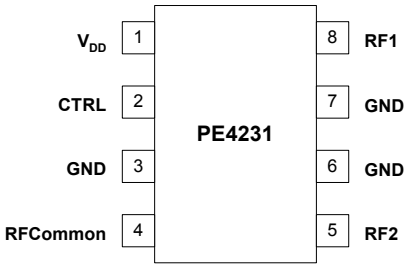

**Figure 2. Package Type**


**Table 1. Electrical Specifications @ +25 °C, $V_{DD}$ = 3 V** ($Z_S$ = $Z_L$ = 75 Ω)

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Operation Frequency[1] | | DC | | 1300 | MHz |
| Insertion Loss | 1 MHz<br>1000 MHz | | 0.45<br>0.80 | | dB |
| Isolation – RFCommon to RF1/RF2 | 1000 MHz | | 44 | | dB |
| Isolation – RF1 to RF2 | 1000 MHz | | 35 | | dB |
| Return Loss | 1000 MHz | | 16 | | dB |
| 'ON' Switching Time | CTRL to 0.1 dB final value, 2 GHz | | 200 | | ns |
| 'OFF' Switching Time | CTRL to 25 dB isolation, 2 GHz | | 90 | | ns |
| Video Feedthrough[2] | | | 15 | | $mV_{pp}$ |
| Input 1 dB Compression[3] | 1000 MHz | | 32 | | dBm |
| Input IP3[3] | 1000 MHz, 17 dBm | | 50 | | dBm |

Notes: 1. Device linearity will begin to degrade below 1 MHz.
2. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.
3. Measured in a 50 Ω system.

## Figure 3. Pin Configuration




## Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Nominal +3V supply connection. |
| 2 | CTRL | CMOS or TTL logic level:<br>High = RFCommon to RF1 signal path<br>Low = RFCommon to RF2 signal path |
| 3 | GND | Ground connection. Traces should be physically short and connected to ground plane for best performance. |
| 4 | RF Common | Common RF port for switch.[1] |
| 5 | RF2 | RF2 port.[1] |
| 6 | GND | Ground Connection. Traces should be physically short and connected to ground plane for best performance. |
| 7 | GND | Ground Connection. Traces should be physically short and connected to ground plane for best performance. |
| 8 | RF1 | RF1 port.[1] |

Note 1: All RF pins must be DC blocked with an external series capacitor or held at 0 $V_{DC}$.

## Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on any input except for the CTRL input | -0.3 | $V_{DD}$+ 0.3 | V |
| $V_{CTRL}$ | Voltage on CTRL input | | 5.0 | V |
| $T_{ST}$ | Storage temperature range | -65 | 150 | °C |
| $T_{OP}$ | Operating temperature range | -40 | 85 | °C |
| $P_{IN}$ | Input power (50Ω) | | 35 | dBm |
| $V_{ESD}$ | ESD voltage (Human Body Model) | | 200 | V |

## Table 4. DC Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| $I_{DD}$ Power Supply Current ($V_{DD}$ = 3V, $V_{CNTL}$ = 3V) | | 29 | 35 | μA |
| Control Voltage High | 0.7x$V_{DD}$ | | | V |
| Control Voltage Low | | | 0.3x$V_{DD}$ | V |

## Table 5. Control Logic Truth Table

| Control Voltage | Signal Path |
|---|---|
| CTRL = CMOS or TTL High | RFCommon to RF1 |
| CTRL = CMOS or TTL Low | RFCommon to RF2 |

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of $V_{DD}$. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the $V_{DD}$ pin when the control logic input voltage level exceeds $V_{DD}$.)

### Electrostatic Discharge (ESD) Precautions

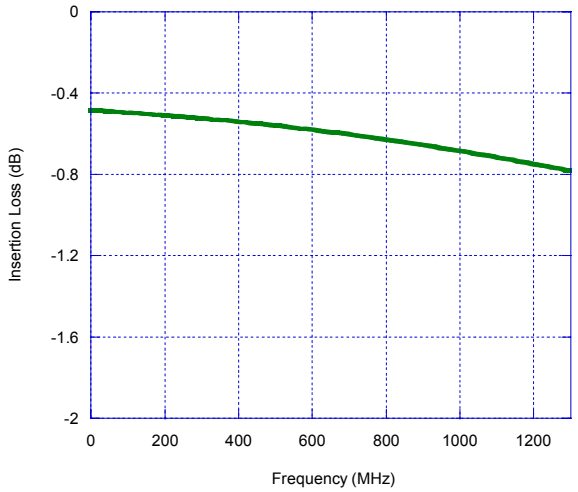
When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

### Latch-Up Avoidance

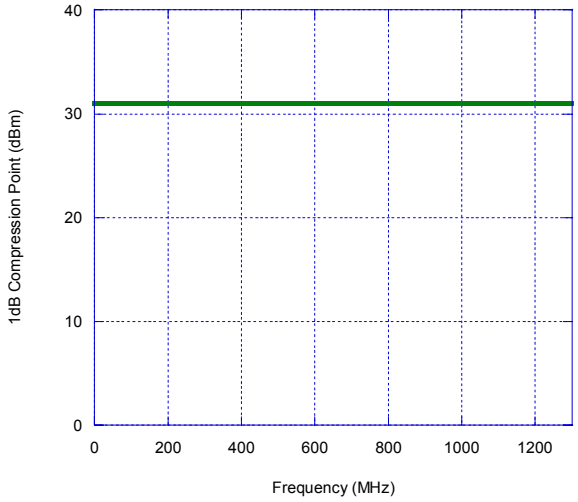
Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

## Typical Performance Data @ -25 °C

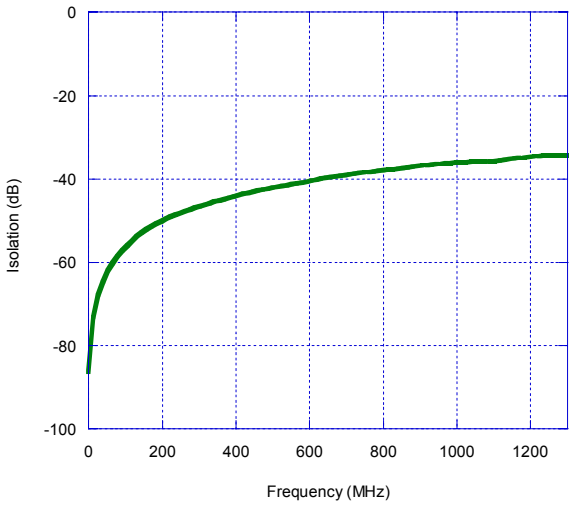
### Figure 4. Insertion Loss



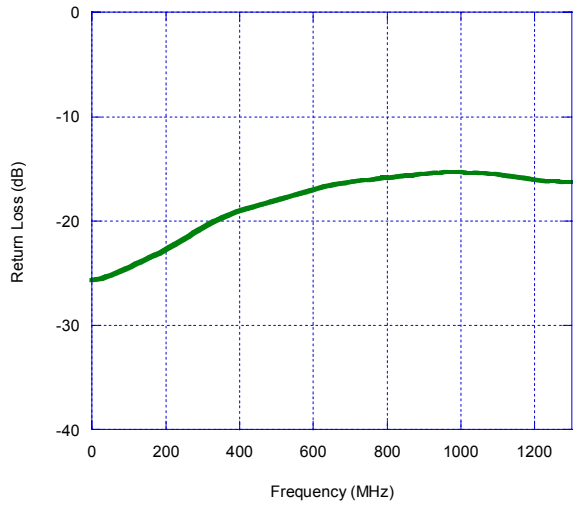

### Figure 5. Input 1dB Compression Point




### Figure 6. Isolation




### Figure 7. Return Loss



## Evaluation Kit Information

### Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4231 SPDT switch. The RF common port is connected through a 75Ω transmission line to the top left BNC connector, J1. Port 1 and Port 2 are connected through 75Ω transmission lines to the top two BNC connectors on the right side of the board, J2 and J3. A through transmission line connects BNC connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0014" and $\varepsilon_r$ of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device CNTL input. The fourth pin to the right (J6-7) is connected to the device $V_{DD}$ input. A decoupling capacitor (100 pF) is provided on both CNTL and $V_{DD}$ traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

**Figure 8. Evaluation Board Layouts**

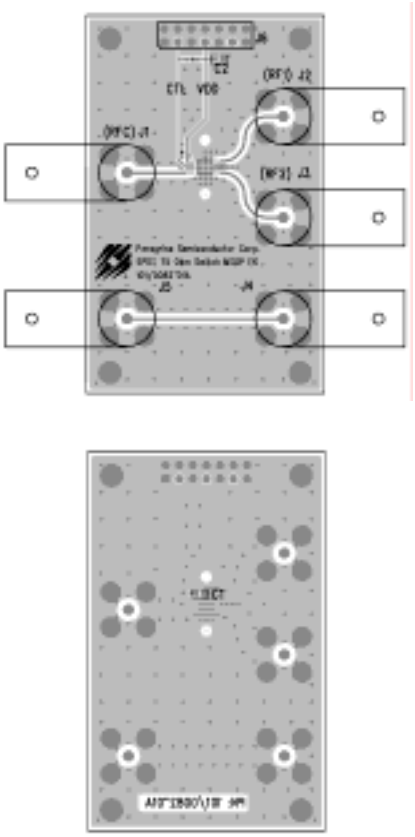
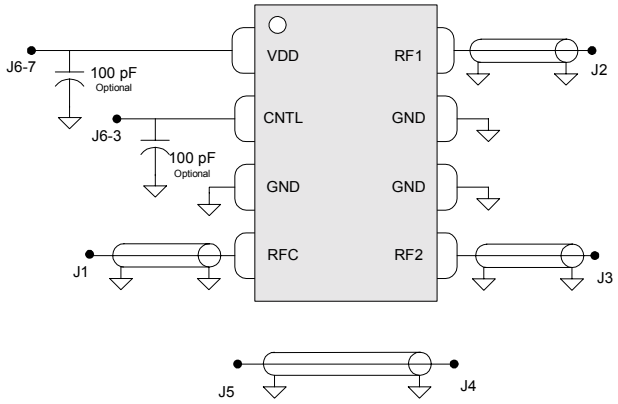
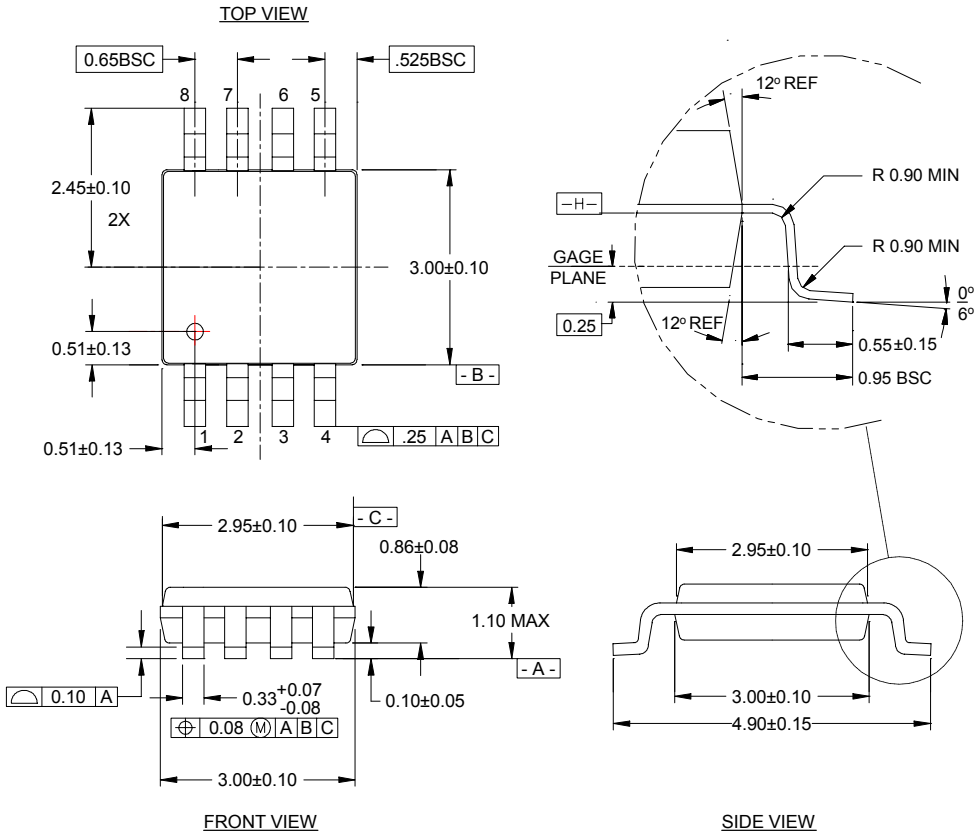


**Figure 9. Evaluation Board Schematic**



## Figure 10. Package Drawing

8-lead MSOP




## Table 6. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|---|---|---|---|---|
| 4231-01 | 4231 | PE4231-08MSOP-50A | 8-lead MSOP | 50 units / Tube |
| 4231-02 | 4231 | PE4231-08MSOP-2000C | 8-lead MSOP | 2000 units / T&R |
| 4231-00 | PE4231-EK | PE4231-08MSOP-EK | Evaluation Kit | 1 / Box |

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# Data Sheet Identification

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The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

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