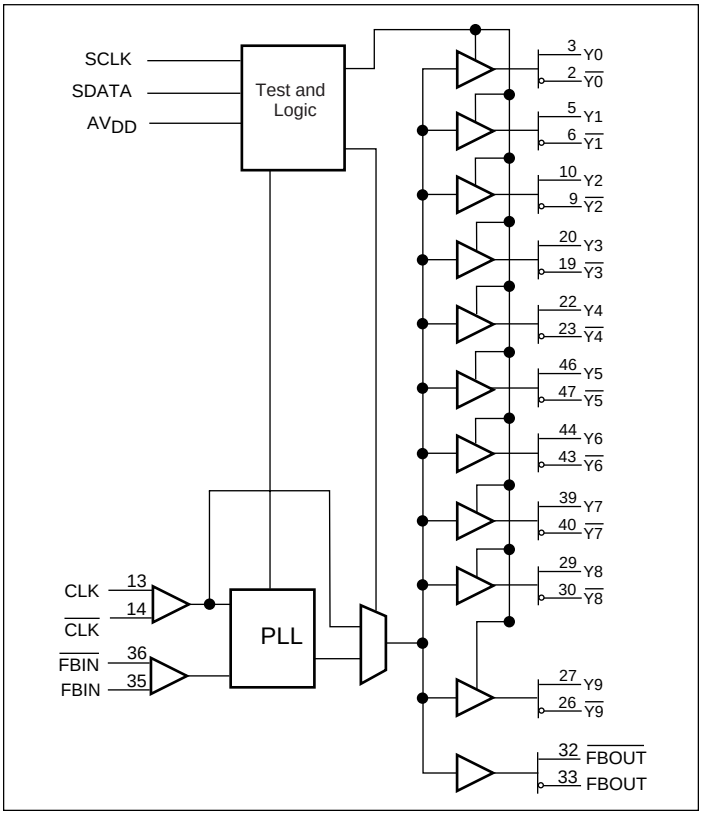
2.5-V Phase Lock Loop Clock Driver with I²C Control Interface

Features

- Phase-Lock Loop Clock Driver for Double Data Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 to 170 MHz
- Low Jitter (cycle-cycle): <|75ps|
- Distributes One Differential Clock Input to Ten Differential Outputs
- I ² C Serial Interface Provides Output Enable and Functional Control
- Three-State Outputs when I²C low-level control bit is written
- Operates from dual 2.5-V and 3.3 V Supplies
- External Feedback Pins (FBIN,$\overline{\text{FBIN}}$) are used to Synchronize the Outputs to the Input Clocks
- Low Jitter < 100ps
- Low Skew < 100ps
- Low Phase Offset: TBD
- 48-Pin TSSOP Package

Block Diagram



Description

PI6CV850 is a high-performance, low-skew, low-jitter zero-delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pair of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair feedback clock output (FBOUT,$\overline{\text{FBOUT}}$). Clock outputs are controlled by input clocks (CLK,$\overline{\text{CLK}}$), feedback clocks (FBIN,$\overline{\text{FBIN}}$), I²C Control Interface, and Analog Power input (AV_{DD}). I²C Control Interface can 3-state individual output clock pairs. When AV_{DD} is strapped LOW, PLL is turned off and bypassed for test purposes.

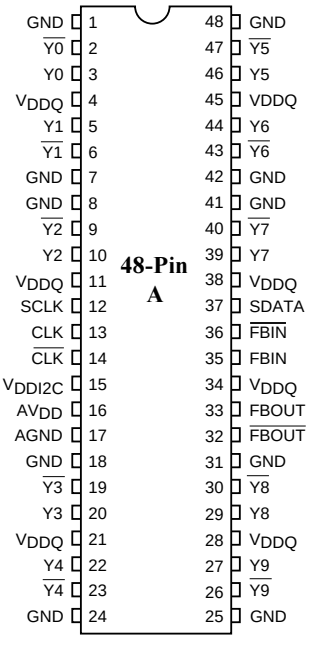
The device provides a standard mode (100kbits/s) I²C serial interface for device control. Implementation is as a slave/receiver, and address is specified in I²C device address table. Both I²C inputs (SDATA & SCLK) provide integrated pullup resistors (typically 140 kohms) .

Two 8-bit I²C registers provide individual enable control for each output pair. At powerup, all outputs default to enabled . Each pair can be placed in a 3-state mode with a low-level output when a low-level control bit is written to the control register. Registers must be accessed in sequence (random access of the registers not supported).

For reduced EMI, the PI6CV850 also tracks Spread Spectrum Clocking .

Since the PI6CV850 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. Also required are changes to various I²C controls that effect the PLL.

Pin Configuration



Pinout Table

Pin Name	Pin No.	I/O Type	Description
CLK $\overline{CLK}$	13 14	I	Reference Clock input
Yx	3,5,10,20,22,27, 29,39,44,46	O	Clock outputs.
$\overline{Yx}$	2,6,9,19,23,26, 30,40,43,47		Complement Clock outputs.
FBOUT $\overline{FBOUT}$	33 32		Feedback output.
FBIN $\overline{FBIN}$	35 36	I	Feedback input.
V_{DDQ}	4,11,21, 28,34,38,45	Power	Power Supply for I/O. 2.5Volts
AV_{DD}	16		Analog /core power supply. AV_{CC} can be used to bypass the PLL for testing purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. 2.5Volts
AGND	17	Ground	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	1,7,8,18,24,25, 31,41,42,48		Ground
SDATA	37	I^2C	Serial Data in for Serial Configuration port
SCLK	12		Clock Input for Serial Configuration port
V_{DDI^2C}	15	Power	2.5V or 3.3V Supply for I^2C Interface

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{CC}	I/O supply voltage range and analog/core supply voltage range	– 0.5	3.6	V
V_I	Input voltage range	– 0.5	V_{DDQ}+0.5	
V_O	Output voltage range	– 0.5		
Tstg	Storage temperature	– 65	150	°C

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Specifications

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
AV_{CC}	Analog/core supply voltage	2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	
V_{IL}	Low-level input voltage for I^2C	Vss– 0.3		0.8	
V_{IH}	High-level input voltage for I^2C	2.0		V_{DDQ} +0.3	
V_{OH}	High-level output voltage, I_{OL} = –12mA	1.7		V_{DDQ}	
V_{OL}	Low-level output voltage, I_{OL} = 12mA	0		0.6	
V_{IX}	Input differential-pair crossing voltage	(V_{DDQ}/2) –0.2		(V_{DDQ}/2) +0.2	
V_{OX}	Output differential-pair crossing voltage at the DRAM clock input	(V_{DDQ}/2) –0.2		(V_{DDQ}/2) +0.2	
V_{IN}	Input voltage level	–0.3		V_{DDQ} +0.3	
V_{ID}	Input differential voltage between CK and $\overline{CK}$	0		0.71	
$V_{DD}I^2C$	2.5V or 3.3V for I^2C supply	2.3		3.6	
V_{OD}	Output differential voltage	0.7		V_{DDQ} +0.6	
T_A	Operating free air temperature	0		70	°C

Electrical Characteristics

Parameter		Test Conditions	A_{VCC}, V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All inputs	I_I = –18mA	2.3V			–1.2	V
I_I	CK, FBIN	V_I = V_{DDQ} or GND	2.7V			±10	µA
	SDATA, SCLK	V_I = V_{DDQ} or GND				±5	
I_{DDQ}	Dynamic supply current					300	mA
C_I	CK and $\overline{CK}$	V_I = V_{DD} or GND	2.5V	2.0		3.0	pF
	FBIN and $\overline{FBIN}$						

Timing Requirements (Over recommended operating free-air temperature).

Symbol	Description	A_{VCC}, V_{DDQ} = 2.5V ±0.2V		Units
		Min.	Max.	
f_{CK}	Operating clock frequency(1,2)	60	170	MHz
	Application clock frequency(3)	95	170	
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	PLL stabilization time after powerup		100	µs

Notes:
1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

AC Specifications

Switching characteristics over recommended Operating free-air temperature range (unless otherwise noted)

Parameter	Description	Diagram	AV_{CC}, V_{DDQ} = 2.5V ±0.2V			Units
			Min.	Nom.	Max	
tjit(cc)	Cycle-to-cycle jitter	see Figure 3	–75		75	ps
t(θ)	Static phase error(1)	see Figure 4		0		
tsk(o)	Output clock skew	see Figure 5			100	
tjit(per)	Period jitter	see Figure 6	–75		75	
tjit(hper)	Half-period jitter	see Figure 7	–100		100	
tsl(i)	Input clock slew rate(2)	see Figure 8	1.0		2.0	V/ns
tsl(o)	Output clock slew rate(2)	see Figure 8	1.0		2.0	
The PLL on the PI6CV850 meets all the above parameters while supporting SSC synthesizers(3) with the following parameters.						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
	PLL loop bandwidth			2		MHz
	Phase angle				–0.031	degrees

Notes:
1. Static Phase Error does not include Jitter.
2. The slew rate is determined from the IBIS model and not from the test load.
3. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

Function Tables

Select Functions

INPUTS			OUTPUTS†				PLL
AV_{DD}	CLK	$\overline{CLK}$	Y[0:9]	$\overline{Y[0:9]}$	FBOUT	$\overline{FBOUT}$	
GND	L	H	L	H	L	H	Bypassed/Off
GND	H	L	H	L	H	L	Bypassed/Off
2.5V (nom)	L	H	L	H	L	H	On
2.5V (nom)	H	L	H	L	H	L	On

† Each output pair can be 3-state via the I²C interface, except FBOUT and $\overline{FBOUT}$

I²C Device Address

The following section describes the I2C interface programming.

A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	0	1	0

Writing to the I²C Interface

1. Send the address $D2_{(H)}$
2. Send the dummy bytes and command code.
3. Send the number of data bytes.

Clock Generator Addr (7 bits)	ACK	+8-Bits dummy command code	ACK	+8-Bits dummy	ACK	Data Byte 1	ACK	Data Byte 4	ACK
A(6:0)& R/W#									
$D2_{(H)}$									

I²C Configuration Command Bitmap

Byte 0: Enable/Disable Register
(H=Enable, L=Disable)

Bit	Pins	PWD	Description
7	3,2	H	Y0, $\overline{Y0}$
6	5,6		Y1, $\overline{Y1}$
5	10,9		Y2, $\overline{Y2}$
4	20,19		Y3, $\overline{Y3}$
3	22,23		Y4, $\overline{Y4}$
2	46,47		Y5, $\overline{Y5}$
1	44,43		Y6, $\overline{Y6}$
0	39,40		Y7, $\overline{Y7}$

Note: Disable/Output held HiZ.

Byte 1: Enable/Disable Register
(H=Enable, L=Disable)

Bit	Pins	PWD	Description
7	29,30	H	Y8, $\overline{Y8}$
6	27,26		Y9, $\overline{Y9}$
5	–		Reserved
4	–		
3	–		
2	–		
1	–		
0	–		

Note: Disable/Output held HiZ.

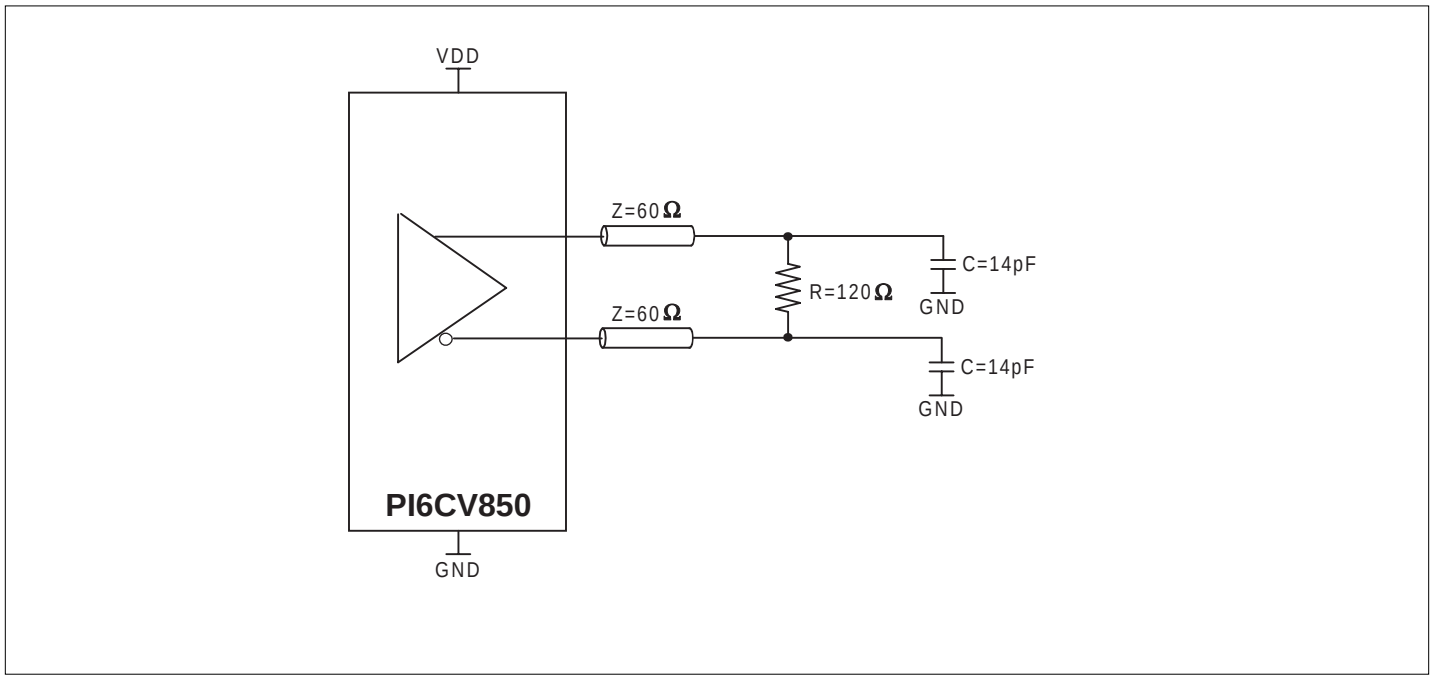


Figure 1. Output Load

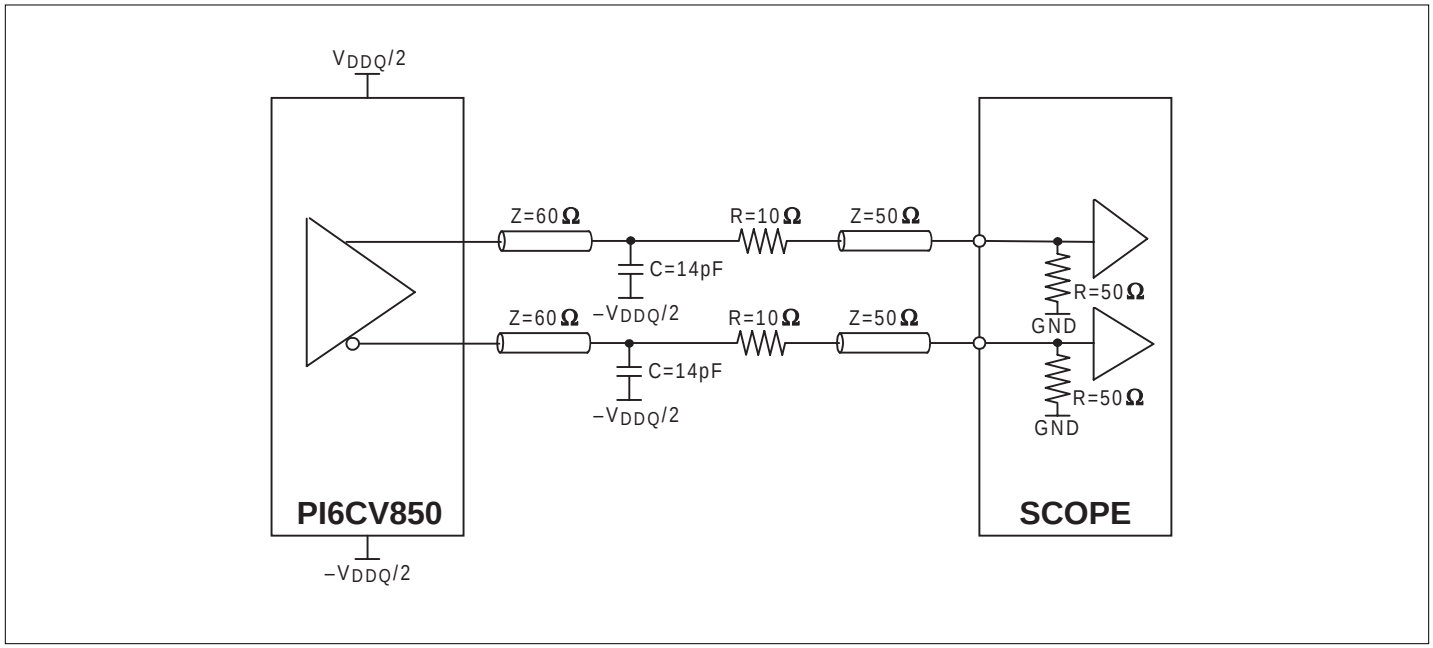
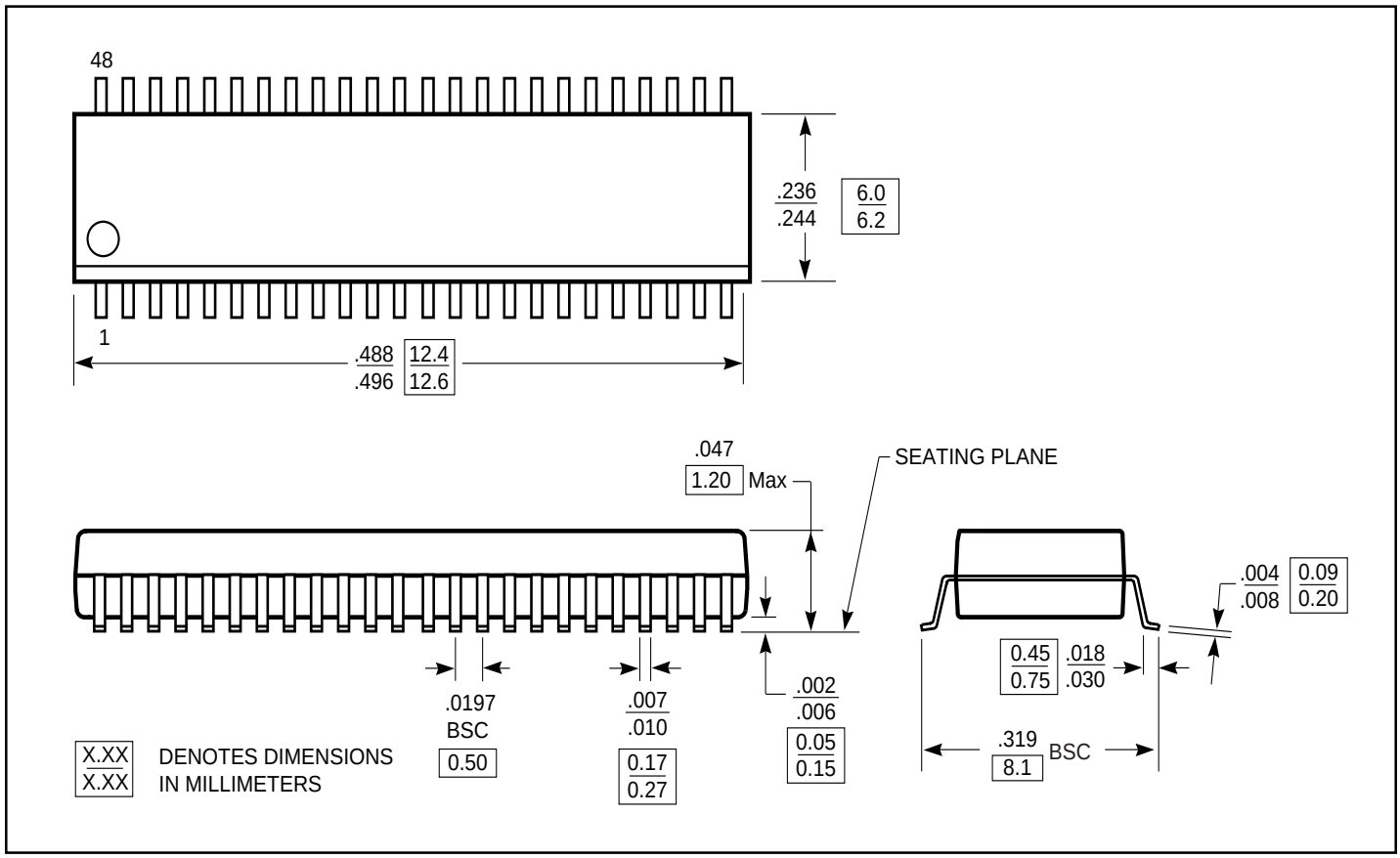


Figure 2. Output Load Test Circuit

48-Pin TSSOP Mechanical Drawing (A)



Ordering Information

P/N	Description	Temp
PI6CV850	48-Pin TSSOP package	Commercial