Zero-Delay Bus Switches

1. Bus Switch Features

Pericom's bus switch product family has many features that are useful in logic circuit design that are not provided by TTL logic ICs. These devices are bus connect switches that use an enable/disable control, with no propagation delay. Using bus switches, a logic designer can accomplish certain design goals with a very simple and effective circuit.

Pericom bus switches are high-speed TTL bus connect devices. When they are enabled, they directly connect two buses with a resistance of less than 5ohms. Since these devices directly connect the bus signals between two buses, they introduce no propagation delay, timing skew, or noise. They are inherently bidirectional and dissipate very little power.

Figure 1 shows the equivalent circuit of a bus switch when enabled. The switch provides a low resistance connection between inputs and outputs for input or output voltages below 3 volts. As compared with competitor devices, Pericom's bus switches have lower resistance. This low resistance feature makes them ideal for bus switching applications.

When the bus switch is disabled, the N-channel transistor gate is at 0V, and the transistor is off. Figure 2 shows that the input pin A and the output pin B are fully isolated when the transistor is off.

The resistance characteristic is shown in Figure 3. If the voltage at point A or point B of Figure 1 is 1 volt, then most of Pericom's bus switches have only 2 to 3.5 ohm resistance. As the I/O voltage rises above 3 volts at points A and B of Figure 1, the switch resistance increases until the switch turns off, at approximately 4 volts.

When the I/O voltages are below 3 volts, the voltages at A and B are identical, since they are connected by an equivalent resistor of less than 5 ohms. Note that the resistance value is determined by the lower of the voltages on the two I/O pins (points A and B). When the input voltage at point A rises above 4 volts, the output voltage at point B does not follow the input voltage, but rises and maintains at $V_{CC} - V_T$, where V_{CC} is the supply voltage at pin 24 or pin 20, and V_T is the threshold voltage of the N-channel transistor, typically 1V.

Pericom's bus switches are low-power devices with quiescent power supply current Icc = 3.0μA. Excellent for Green PC and notebook PC applications.

Pericom's bus switch products are available in three package types: 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and industry's new 150 mil wide plastic QSOP. The pin-to-pin pitch of the SOIC package is 50 mils. The pin-to-pin pitch of the QSOP package is only 25 mils. As shown in Figure 4, the SOIC package saves 44 percent of board space compared with a plastic DIP package. Amazingly, the QSOP package saves 81 percent of board space as compared with the plastic DIP package.

Pericom's bus switch has many unique applications which cannot be easily implemented by competing devices.

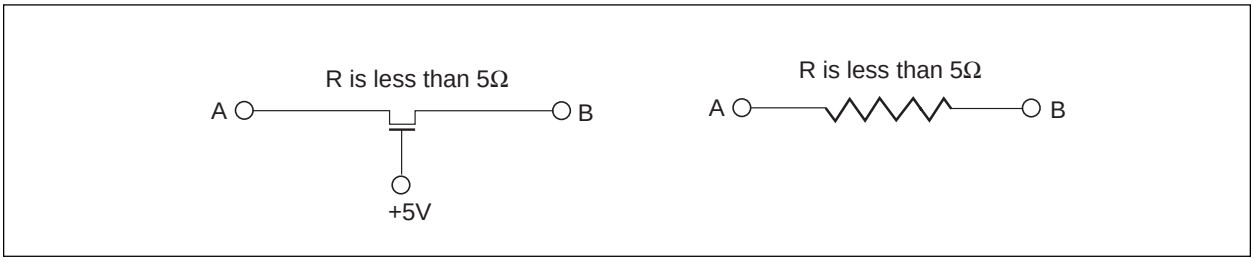


Figure 1. Bus Switch Equivalent Circuit When Enabled.

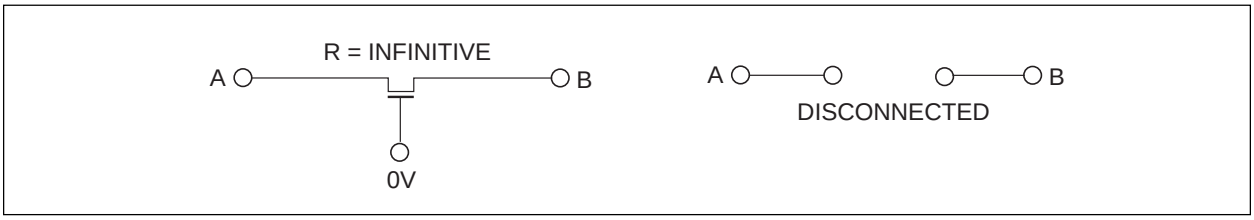


Figure 2. Bus Switch Equivalent Circuit When Disabled.

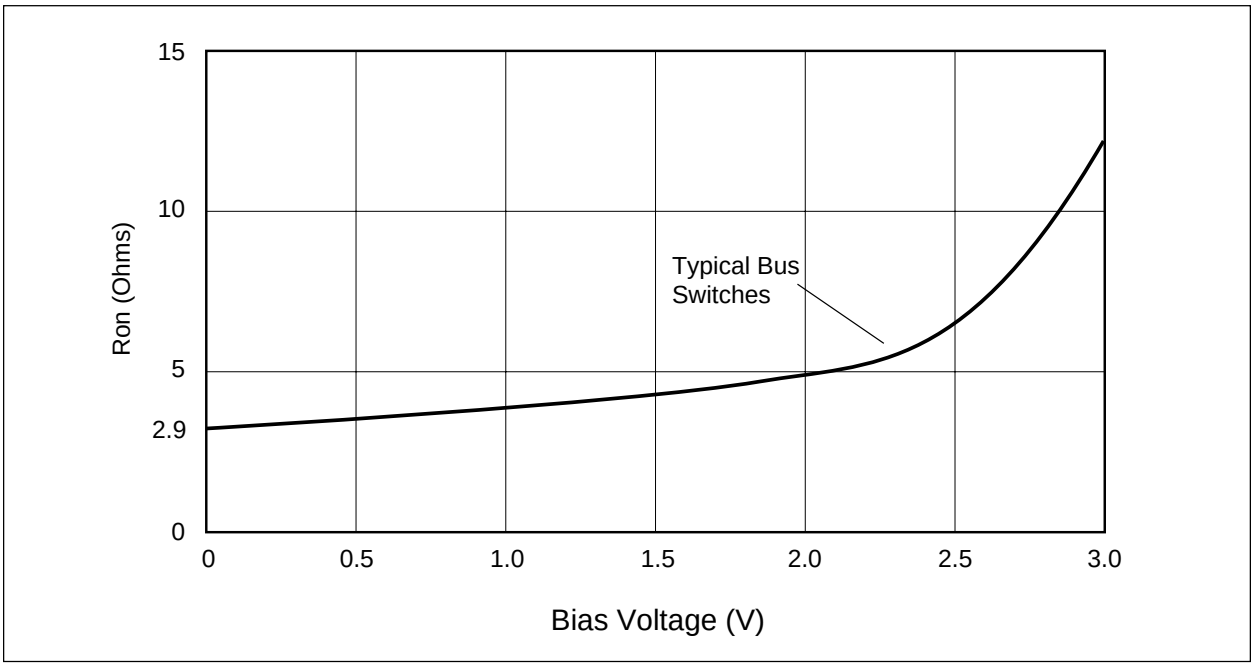
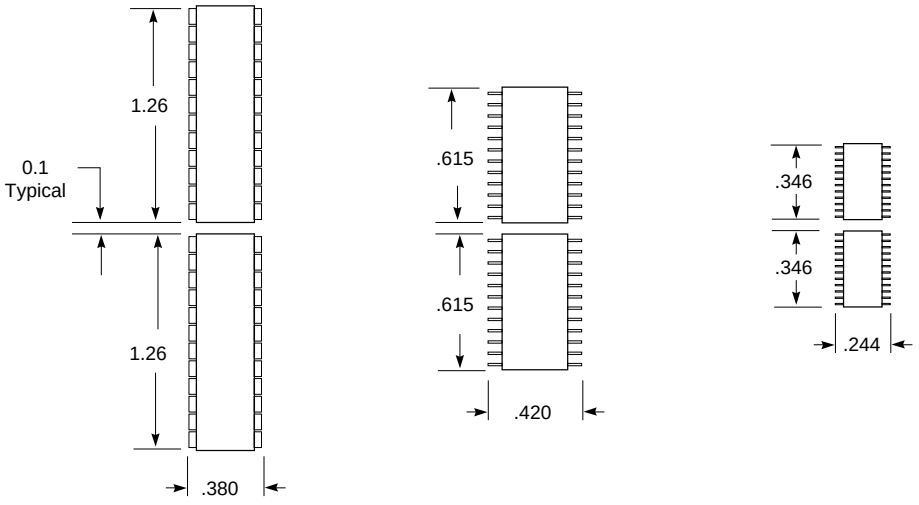


Figure 3. ON-Resistance of Pericom Semiconductor's Bus Switch, at V_{CC} = 4.75V.



	Two 24-pin DIP	Two 24-pin SOIC	Two 24-pin QSOP
Area (sq. in.)	0.996	0.559	0.193
Reduction:	0%	44%	81%

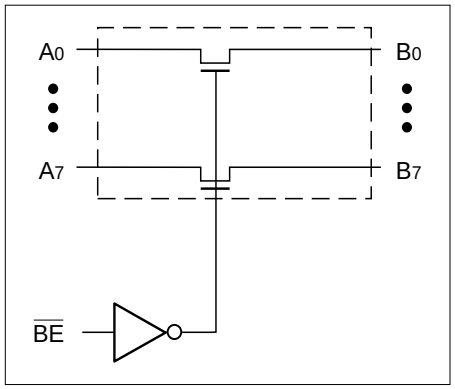
Figure 4. Package Comparison Board Space Requirements.

2. Bus Isolation and Multiplexing

The PI5C3245 and PI5C3861 CMOS bus switches are ideal for bus isolation applications. A logic block diagram of the PI5C3245 that is pin compatible with the 74 x 245 TTL transceiver is shown in Figure 5. This device, when enabled, allows eight signals at bus A to be connected to eight signals at bus B. Since the corresponding bus signals are directly connected, the bus switch does not introduce propagation delay, timing skew, or noise, compared with a traditional TTL 74F245 transceiver or 74F244 driver. The purpose of bus isolation may be zero delay bus multiplexing or bus loading reduction for isolating the loads, which are not currently in use.

Figure 6 shows the application of bus load reduction. The microprocessor's output driver can drive only one bank of SRAMs. It cannot drive two banks simultaneously because of capacitive loading of memory arrays. By address decoding, only one bank is enabled at a time. Each data driver of each SRAM does not tie with the other bank's SRAM. The driver loading is reduced and the bus switch transceiver does not have any propagation delay. As a result, the access time of the SRAM array is reduced. This is an ideal application for a high-performance system.

Logic Block Diagram



Truth Table(1)

Function	$\overline{BE}$	A0–7
Disconnect	H	Hi-Z
Connect	L	B0–7

Note:
H = High Voltage Level
L = Low Voltage Level
Hi-Z = High Impedance

Figure 5. PI5C3245, 8-Bit, 2-Port Bus Switch, or PI5C3384, 10-bit, 2-Port Bus Switch for Zero Delay Multiplexing.

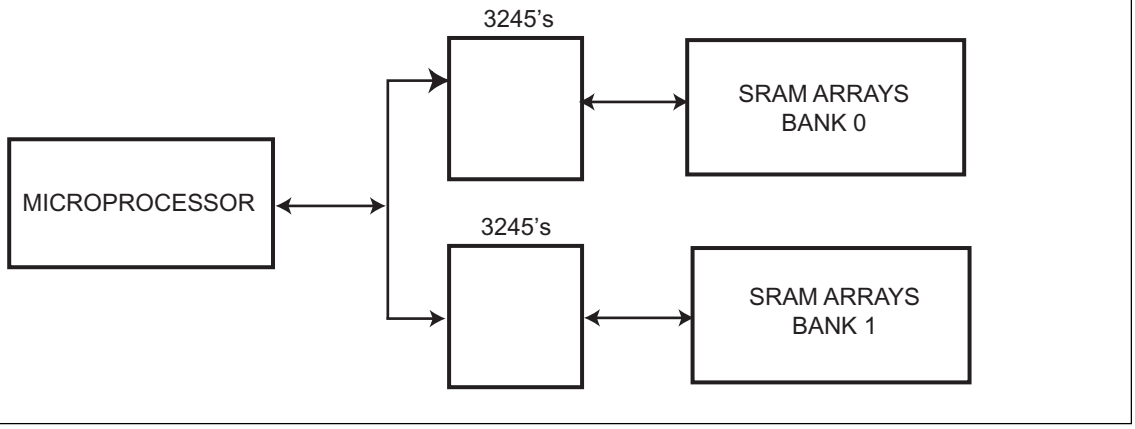


Figure 6. Bus Isolation by PI5C3245, for Bus Load Reduction

3. Zero Delay Bus Transceiver

To eliminate system propagation delay of transceiver bus switches, PI5C3245 and PI5C3861 can replace 74F245/F86TTL transceivers. In this application, the driver of the input pin of the bus switch can drive the output load at the output pin. Since the bus switch directly connects two buses, it provides no drive of its own but relies on external drive. In addition to a zero delay benefit, the bus switch also has an advantage over a TTL transceiver which requires complex timing of the direction signal to direct the data flow either from A bus to B bus or from B bus to A bus. To avoid a current glitch at the power/ground plane, the TTL transceiver's direction signal must remain unchanged while the transceiver is enabled (see Figure 7). The direction signal may switch only during the window of time when a TTL transceiver is disabled. The bus switch does not require a direction signal. Therefore, the bus switch does not need the logic circuit generating the appropriate direction signal and does not have the problem of ground glitch because of the direction signal's improper switching time.

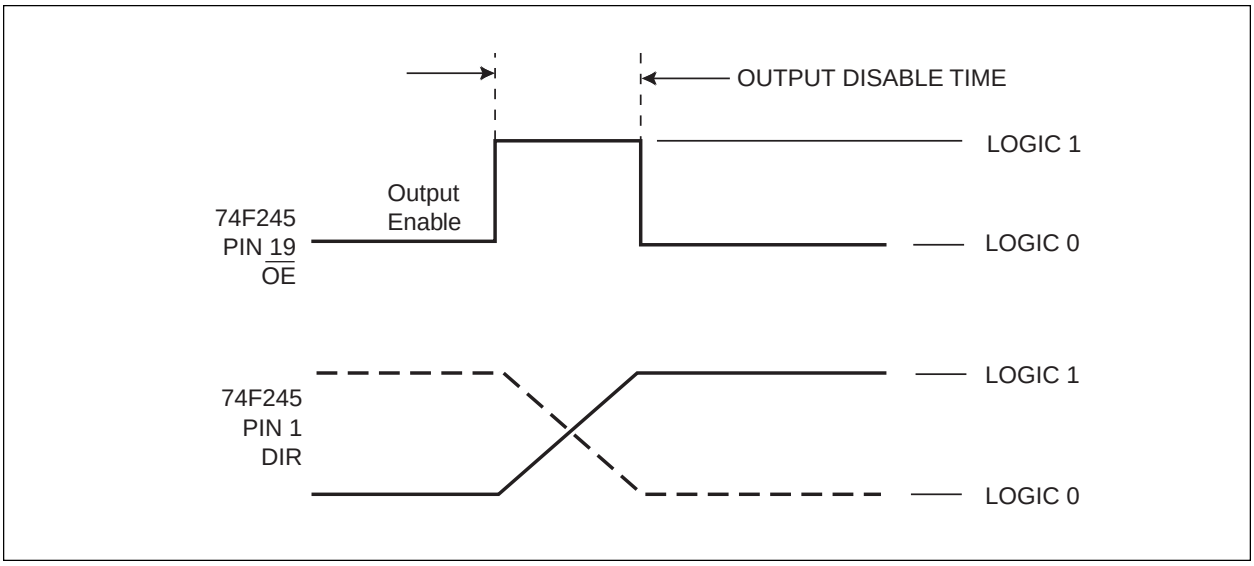


Figure 7. Time Relationship Between OE and DIR of 74F245 Transceiver.

4. Conversion Between 5V and 3V Logic

With microprocessors continuously striving to reach higher speeds and lower power consumption, the trend is to use low voltage processes with smaller feature sizes. As a result we often find mixed voltage systems where microprocessors, chip sets, and other components require different power-supply voltages.

When 5V and 3V logic devices need to communicate with each other, since many of the 3V ICs are not 5V Tolerant, there is a need to provide level shift/translation functions. Pericom's bus switches are widely used to provide these functions

Battery operated computers, such as notebook computers, use 3V TTL logic families for both high-speed and low power. Most systems have a mixture of 5V TTL and 3V TTL logic, because peripheral/peripheral controllers still need 5V TTL logic. The conversion between the two types is required to prevent damage to the 3V TTL even though their logic levels are compatible, since the 3V TTL often cannot tolerate any input voltage swing above 3.3V. To assure a proper interface between the two types, a bus switch can be used as shown in Figure 8.

If the diode has 0.8V drop, the Vcc voltage is at 4.2V. The internal enabling signal at point A is 4.2V max. When signals B are connected to the 3V TTL circuit from the 3384 bus switches, voltage will be 3.2V max, which does not cause any problem to the 3V TTL circuit. R1 pull up may be required to ensure that the switch turns on properly. R2 is needed if 3V data needs to be pulled up to 5V.

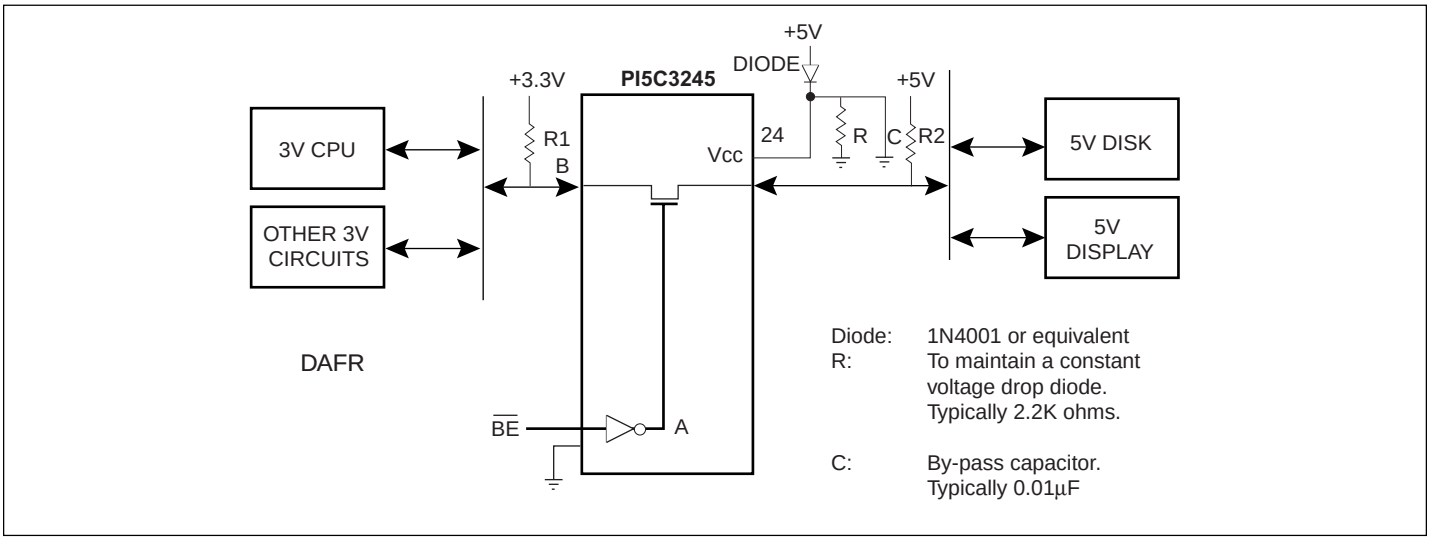


Figure 8. 5V TTL to 3V TTL Conversion.

To assume a reliable voltage drop across the diode, the circuit must consist of the following:

1. A diode that is capable of maintaining a constant voltage drop, such as 1N4001.
2. A resistor R is to provide a 2.3mA pre-loaded forwarding current to help the diode working in the I-V area that is less sensitive to the current caused by signal activities and may reduce 0.1V V_{CC} ripple.
   PI5C3384 or PI5C3384C, however, does not need R because these switches are not sensitive to V_{CC} ripples.
3. The typical value of C is from 0.1uf to 0.47uf.

For cost savings, one of this kind of diode circuit may provide the 4.2V Vcc that will be shared by several bus switches.

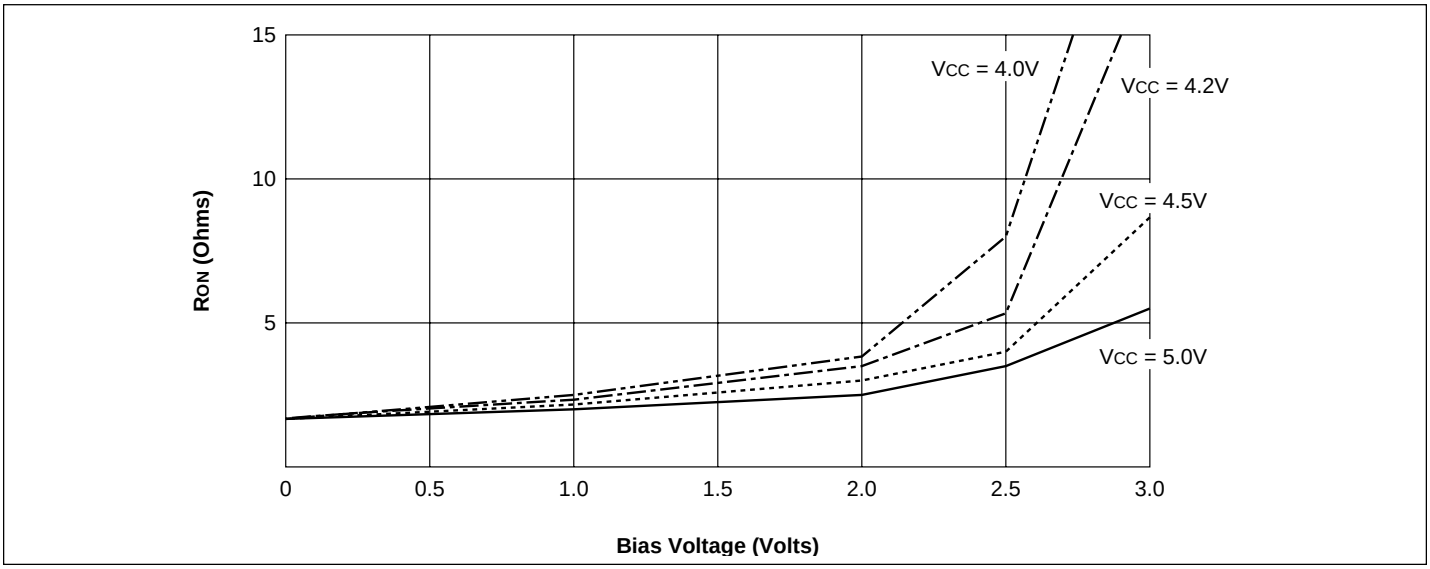


Figure 9. On-Resistance R_{ON} Increases Only Slightly when V_{CC} Voltage Drops Below 5.0V, for TTL Signals Between 0V and 2.5V.

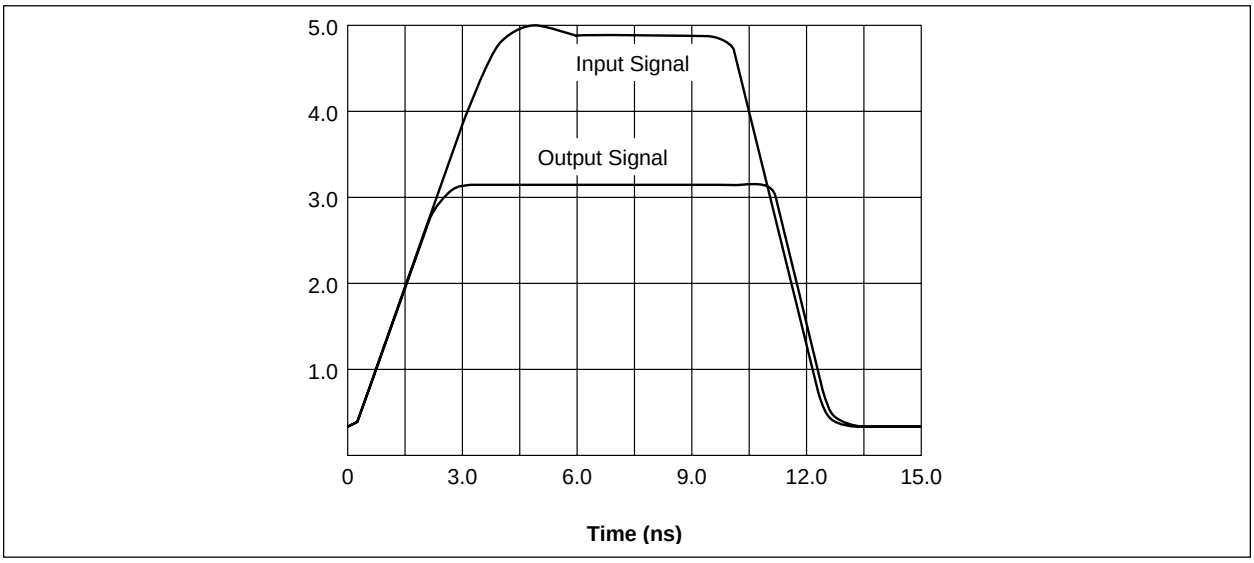


Figure 10. Input and Output Signals at V_{CC} = 4.2V. Output Signal Stays Below 3.3V.

5. Multiplexing Analog Signals with a Bus Switch

Bus switches are ideal devices to multiplex small analog signals. They offer many advantages over traditional analog switching devices. Pericom's bus switch has only 5 ohms of resistance, while traditional analog switching devices have from over 80 ohms to several hundred ohm resistance. The bus enable/disable time of a bus switch is 10 to 100 times faster, compared with traditional analog switching devices.

In multimedia applications, for example, it is desired to multiplex video signals without any signal loss in a multiplexing circuit. The VGA signals are 0V to 0.7V peak-to-peak. The bus switch is the best device for this application, and at a lower cost.

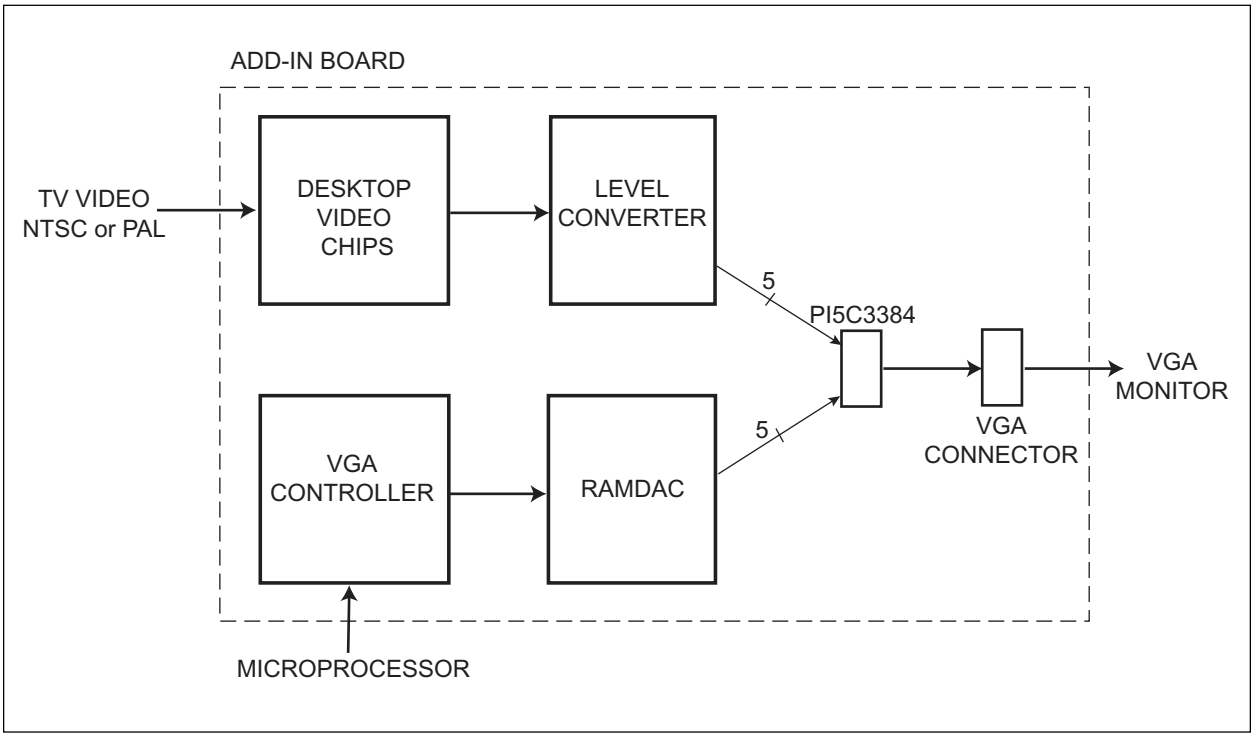


Figure 11. One Pericom Bus Switch, PI5C3384, Multiplexes the VGA Signals from VGA Controller and TV Video Signal.

Propagation Delay

Because they add less than 5 ohm resistance to the VGA signal propagation path, Pericom's Bus switches are able to offer zero propagation delay.

Enable/Disable Time

Pericom's Bus Switches enable/disable a bus at 6.5ns max. Since it is less than one VGA clock time period, the switch is very easy to be used as a VGA multiplex circuit. For comparison, a traditional analog switching device needs enable/disable time in the order of 10ns to over 100 ns.

Crosstalk and Off-isolation

Crosstalk measures the noise that couples from a switching signal to another signal at adjacent channels. Off-isolation measures the noise that couples from a switching signal to the output of an open switch.

The noise level of crosstalk and off-isolation depends on circuit layout and circuit loading. For VGA applications, crosstalk and off-isolation of Pericom's bus switches are equivalent to traditional analog switching devices.

Insertion Loss

Insertion loss is the attenuation of an analog signal propagating from an input to an output of a bus switch. Since Pericom's bus switch resistance is very small, its insertion loss is similarly very small for VGA applications.

Package

Pericom's bus switches are packaged in small SOIC or tiny QSOP packages, resulting in tremendous board space savings.

6. Hot-Plug

Certain computer systems, such as airline reservations, manufacturing control, and telecommunication, cannot be regularly shut down for maintenance services or adding new hardware enhancement. These systems must allow installation/ removal of hardware without turning off power. Hot-plug means the ability to replace a plug-in board in a system while the system power is fully active. When a board is plugged in, it must not disturb the operation of the system, even though it initially has no power. Bus switches are useful to entirely isolate the connector of the plug-in board from the bus until the bus switch is enabled by the system.

Figure 12 shows the application. The CPU must run all the time, even for the purpose of adding new hardware or repair service. The PI5C3384's isolate the bus completely when disabled. Adding a plug-in board or removing a plug-in board will not disturb the CPU operation while the bus switches are disabled.

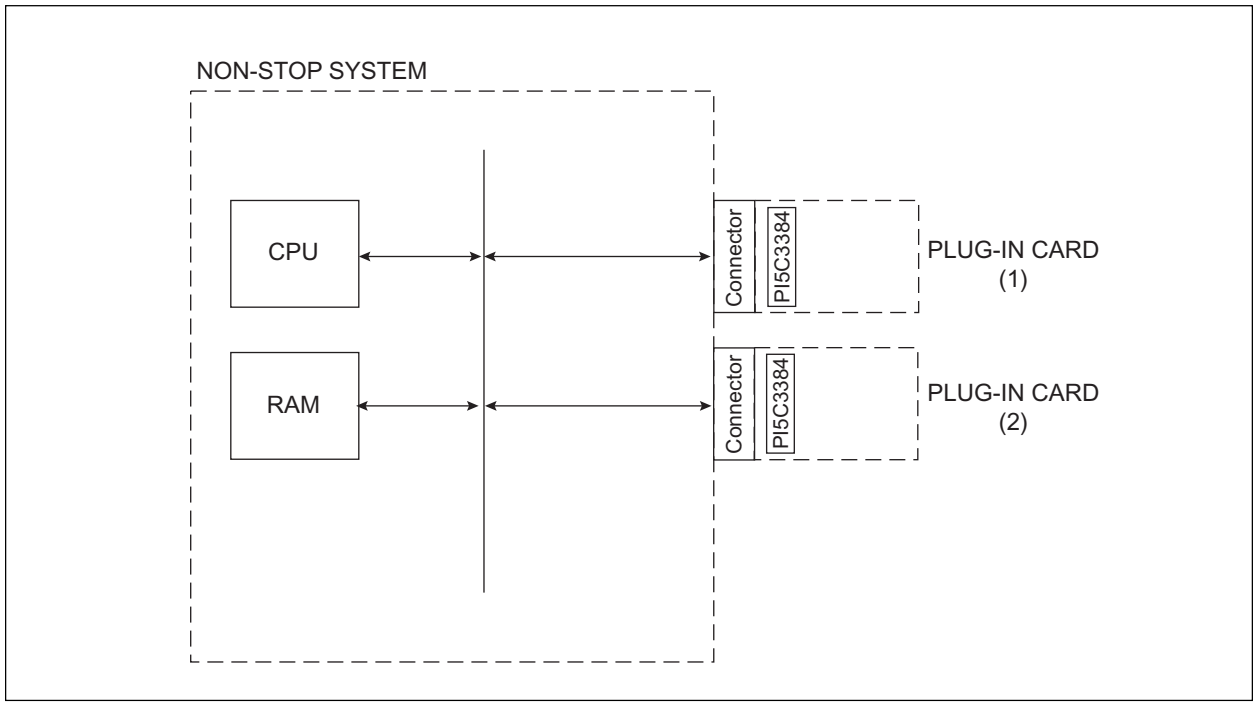


Figure 12. Hot-Plug System.

Staggered Pin Arrangement for an Edge Connector:

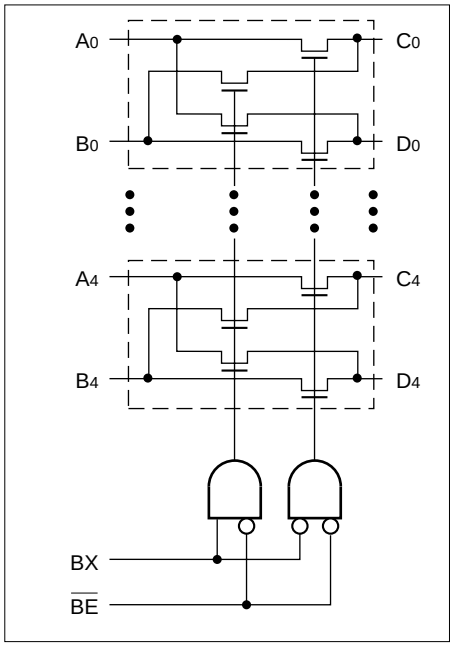
A staggered edge connector arrangement can be adopted to provide control of an output enable pin ($\overline{OE}$), ensuring high impedance on the back-plane. It will satisfy both insert and removal requirements. By offsetting the $\overline{OE}$ pin, $\overline{OE}$, driven by the backplane, will reach a high level before V_{CC} is applied or $\overline{OE}$ remains at a high level during V_{CC} ramp.

Pericom's bus switch devices offer the features required by hot plug applications. During the process of plugging in the card, when V_{CC} is not connected, all signal pins at the bus interface remain floating. See Figure 2, "Staggered" Finger Arrangement for Hot Plug Applications in Application Note 5.

7. Bus Exchange for Shared Memory

Figure 14 shows the logic diagram of Pericom's PI5C3383 CMOS 5-bit, 4-Port Bus Switch designed with a low ON-resistance. When the exchange control BX is LOW and BE is active, A-bus is directly connected with C-bus while B-bus is directly connected with D-bus. When the exchange control BX is HIGH, A-bus is connected with D-bus while B-bus is connected with C-bus. This exchange configuration allows bit swapping of buses in systems. Figure 15 shows Host CPU and DSP CPU exchange Memory A and Memory B. In this configuration, Host CPU and DSP CPU are allowed to access Memory A and Memory B simultaneously, for high-performance system application. A typical DMA configuration does not allow such a simultaneous memory access operation. A bus switch has many benefits over TTL transceivers: it does not incur a propagation delay, and does not require generation of a direction signal.

Logic Block Diagram



Pin Description

Pin Name	Description
$\overline{BE}$	Bus Enable Input (Active LOW)
BX	Bus Exchange Input
Ax	Bus A
Bx	Bus B
Cx	Bus C
Dx	Bus D

Truth Table(1)

Function	$\overline{BE}$	BX	A0–4	B0–4
Disconnect	H	X	Hi-Z	Hi-Z
Connect	L	L	C0–4	D0–4
Exchange	L	H	D0–4	C0–4

Note: 1. H = High Voltage Level
L = Low Voltage Level
Hi-Z = High Impedance
X = Don't Care

Figure 14. Pericom's PI5C3383, 5-Bit, 4-Port Bus Switch.

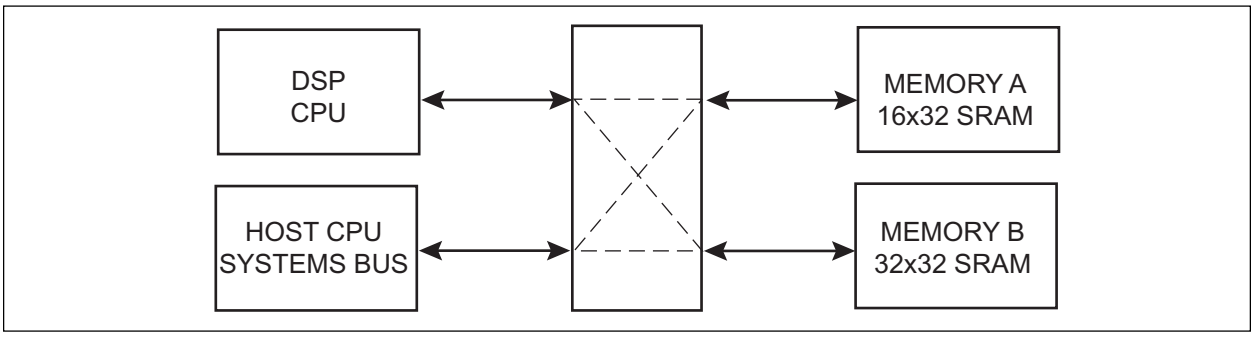


Figure 15. Bus Exchange for Share and Memory.

8. Bus Exchange for Crossbar Systems

Figure 16 shows the 3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration, where any CPU can be connected to any memory. The 3383 bus exchange switch is ideal for crossbar work because it introduces no delay of its own. The CPU sees a simple RAM interface.

If traditional bus transceivers are used, the multiple stages of bus switching require long propagation delays which will result in a complicated timing skew problem. Using bus switches eliminates the need for a complex logic circuit to generate the direction signals at a proper time.

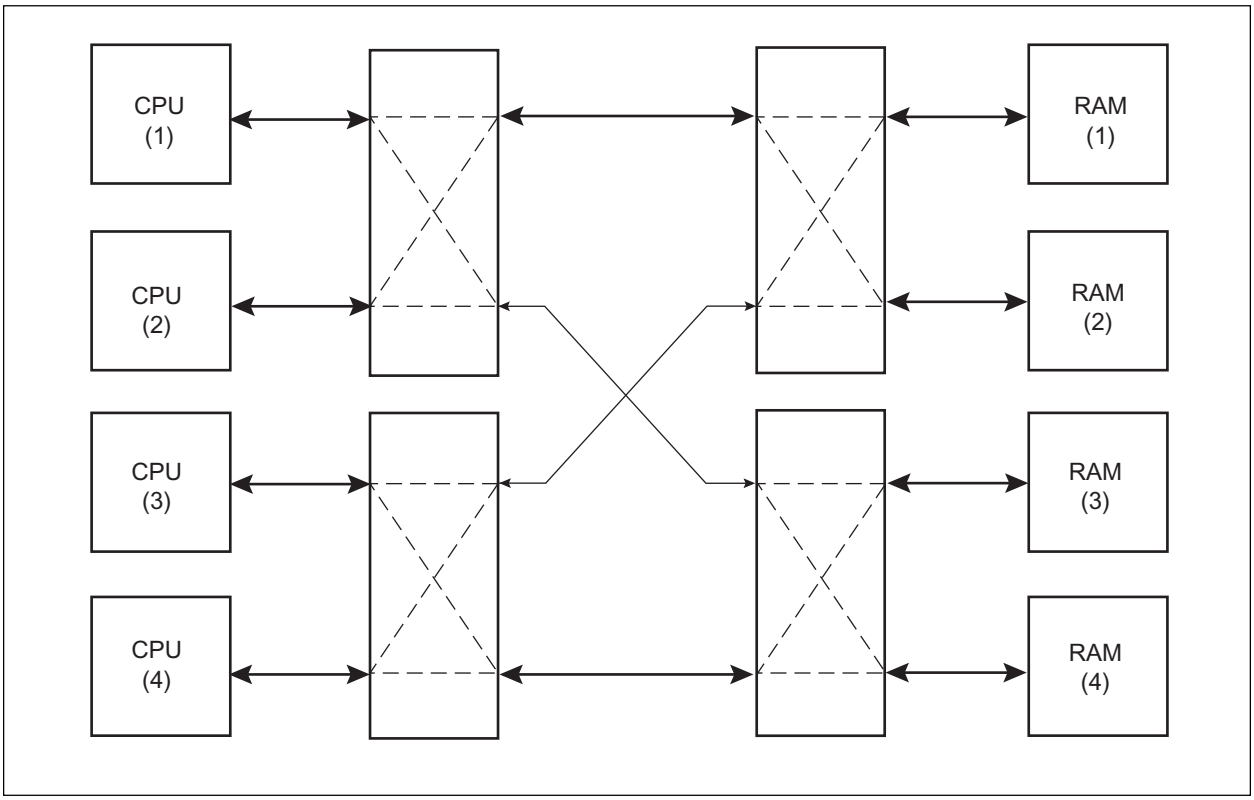


Figure 16. Crossbar Switch Between Four CPUs and Four RAMs.

9. Data Byte Swap in Hardware

Pericom's bus switches PI5C3245, PI5C3384 or PI5C3400 can be used to provide a byte swapping capability between a CPU and memory. Bus swap in hardware is extremely useful in systems where Big Endian and Little Endian byte orders are mixed within the same system. Figure 17 shows the Big and Little Endian memory formats and Figure 18 illustrates a conversion between the two memory formats.

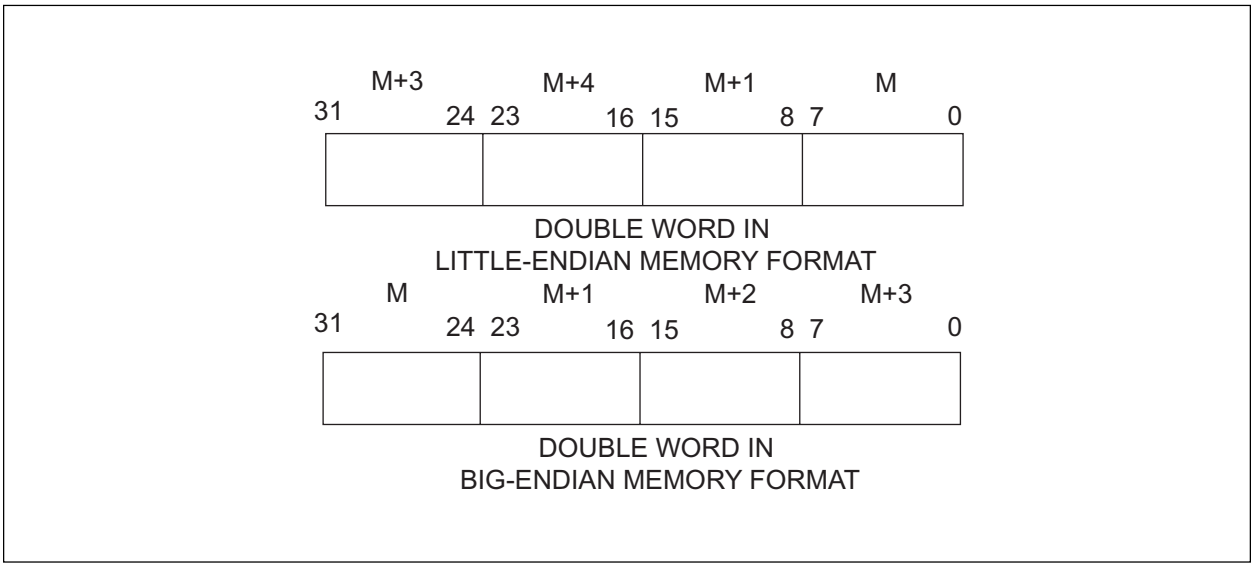


Figure 17. Big versus Little Endian Memory Format.

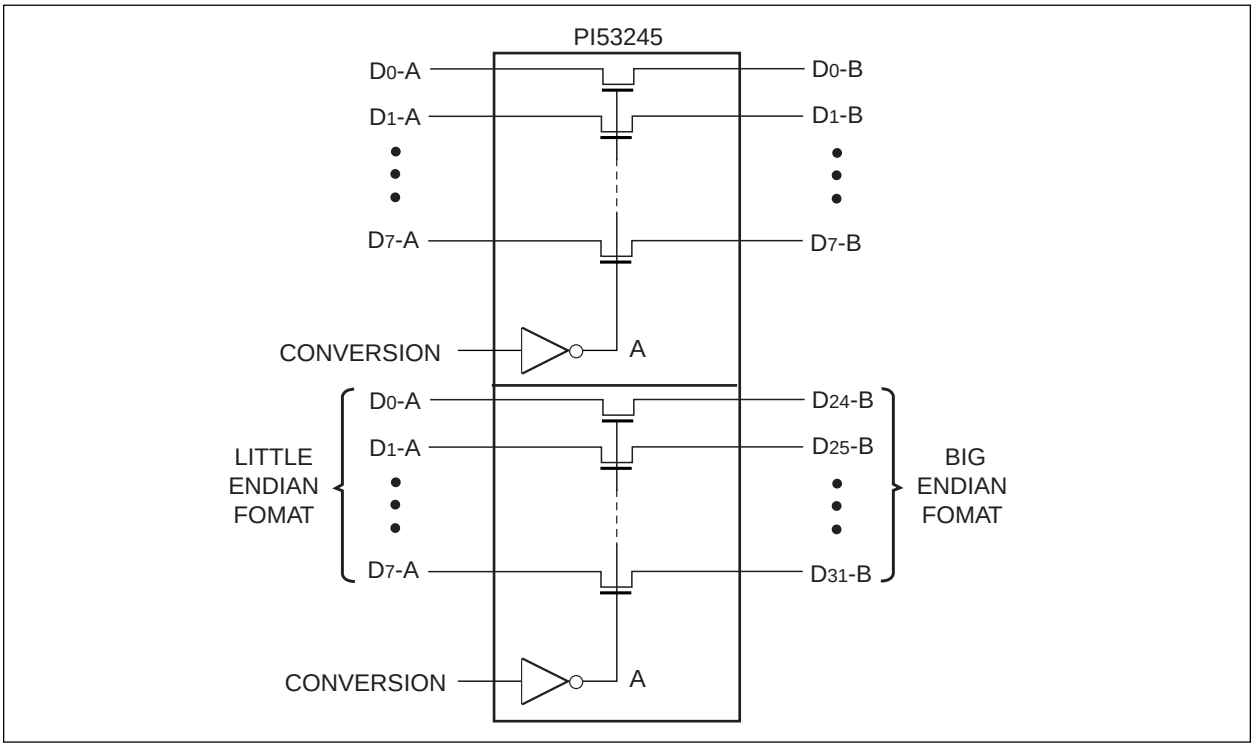


Figure 18. Conversion Between Little Endian and Big Endian Format.

10. Test Load/Driver or Test Channel Selection

Because it contributes no added load, the Bus Switch is an ideal circuit selection for automatic test equipment.

- ***ATE Load/Driver Switch***: Automated test equipment needs to test an output driver of a Device Under Test for different test loads. The bus switch allows the tester to switch to a new test load and isolate the old test load for an output pin (see Figure 19). The bus switch also allows a tester to select a different driver to drive an input pin.
- ***ATE Test Pin Function Selection***: Using Pericom's PI5C3400, each test pin can be programmed individually for different test functions. Figure 20 shows that a pin of a Device Under Test may be input or output. The PI5C3400 provides an individual control pin BXi. When BX0 is LOW, A0 and C0 are connected so driver of ATE drives the input pin X0 Device Under Test. Similarly, if BX1 is programmed HIGH, B1 is connected to C1 so comparator of ATE can test output pin X1 Device Under Test.

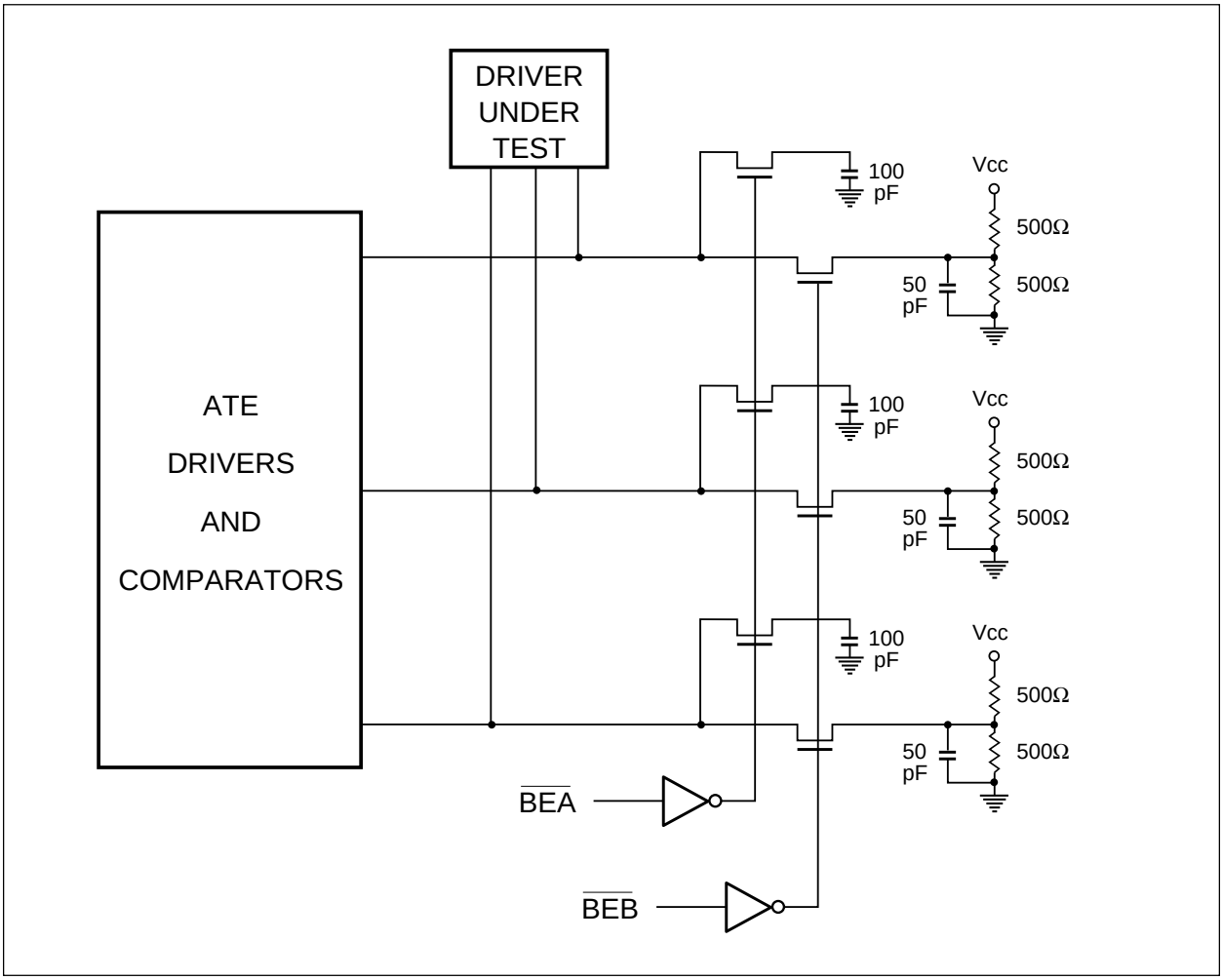


Figure 19. ATE Load Switch using Pericom's PI5C3384 Bus Switch.

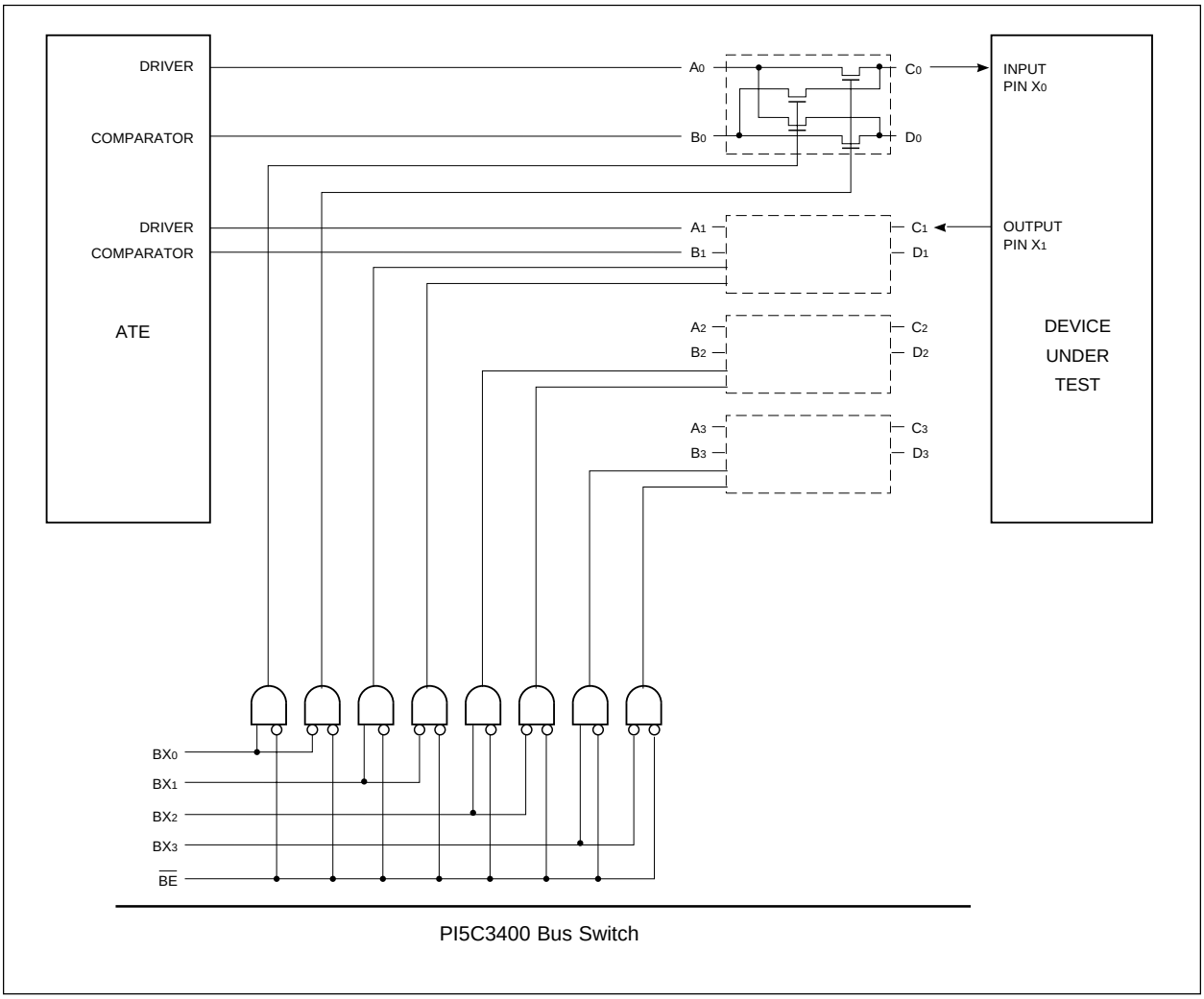


Figure 20. Test Pin Selection Under Individual Control.

PI5C3125 and PI5C3126 Low Cost Quad Bus Switch Devices With Individual Enables

11.1 Introduction

The Pericom's PI5C3125 and PI5C3126 CMOS Quad analog bus switch devices provide 4 bidirectional, high-speed switches that have separate enables. Useful from DC to more than 120MHz, these devices present a 5-ohm typical ON resistance and 8pF total capacitance when enabled.

Useful for a large variety of applications, these devices are both low in cost and small in size. They are suitable for desktop, notebook, and other space limited applications.

Bus switch devices are large analog transmission gates that exhibit low resistance, bidirectionality and extremely low power consumption. The devices do not provide any drive in themselves, but propagate signal levels between the source and drain pins with a minimum of signal distortion and attentuation. Since bus switches are bidirectional, there is no additional delay owing to turnaround typical of 74x245 type devices (PI5C3245 is functionally pin compatible with a 74x245 footprint, but the DIR pin is a no-connect).

These devices propagate signal levels from ground to approximately 1V below Vcc, where the signal level is cleanly clipped. This feature is very useful for extremely fast level translation between 3.3V and 5V system logic that is popular today.

Because there are applications that need impedance matching with a fast enable, Pericom bus switch devices are also offered with an integral 25-ohm resistor.

11.2 Applications

1. **Fast in-line signal enable/disable** without introducing additional propagation delay.
2. **Fast signal multiplexing** with a minimum of waveform distortion.
3. **Pull-up and pull-down** (up to 100mA) can be used in pairs for cable driving.
4. **Manual jumper replacement** on motherboards (pull-up, pull-down, and signal enable/disable) use one dip switch or hex switch to select user configurations.
5. **Load Isolation**: several parallel banks of load can be isolated by bus switches so that the controller sees only one bank at a time, and the bank sees only the controller. This is particularly useful for DRAM memory applications where the capacitance of several banks of DRAM can force additional wait states.
6. **Fast Local Bus Ready Control**: Peripheral controller cards that reside on a local processor bus (most architectures) need to pass or control handshake lines. In situations where the particular controller card is not being addressed, these critical control signals need to be passed on as quickly and as cleanly as possible, or the system will start introducing additional undesirable wait states. The Pericom PI5C3125 (or PI5C3126 for active high enables) can be placed near the connector and used to bypass the control signal (i.e. the LRDY# of the VESA bus) around the normal control logic if the card is not actually being addressed.
7. **Signal Blanking**: Where a signal needs to be suppressed during a critical interval, or where unnecessary clock data need to be removed from a data stream, the PI5C3125/ PI5C3126 can be used as a fast signal flow controller. One typical application is the data from CCD arrays, where clock and data are gated together. Once the clock is recovered from the data stream, the clock can then be used to blank the clock information in the data stream.
8. Applications that already use the 74xx126/126 parts that can benefit from a faster enable/disable time.
9. Small multiplex/demultiplex applications that need to be local to a particular part of the design. The 3125/3126 has four separate bidirectional gates with individual enables. Joining inputs and/or outputs together, custom mux/demux designs can be built efficiently. Requirements that need decoded enable/control signals can use the Pericom 3251/3253/3257 for mux/demux applications and the Pericom 3383/3400/ 3401 devices for switch matrix applications. Since the bus switch is inherently bidirectional, there is no direction control necessary.

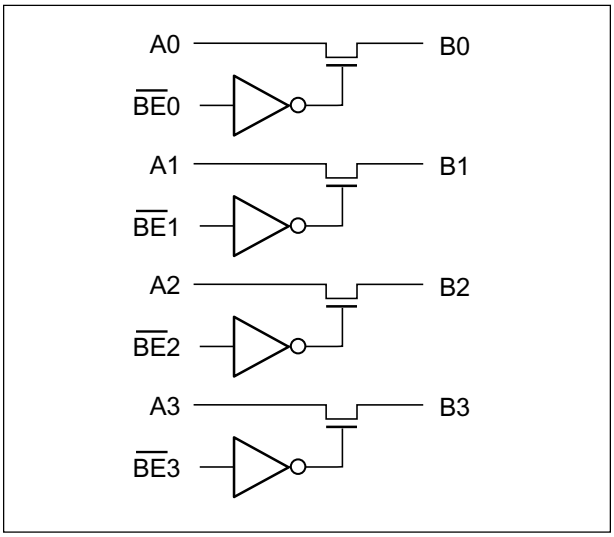
   Another multiplexer application that is particularly useful is on the VESA Video feature connector that allows a second device (video capture/playback for example) to gain access to the VGA connector. The bus switch provides an ideal solution for this application since the bus switch will not introduce any additional waveform distortion or signal-to-signal skew.
10. **Hot Plug and Hot Swap Isolation**: Pericom bus switch devices exhibit extremely low leakage (less than 0.2mA typical when disabled and/or when power is off). Since these gates are designed without "P" channel devices (which can cause latch-up) and do not have a diode clamp to Vcc, there is no leakage path when power is off and the signal level is above ground. Internal clamp diodes from signal to ground prevent false enable effects because of signal undershoot, up to better than 1V below ground level. As a result, the impact of a hot plug-in on a live circuit is minimized to the stray capacitance of the device and the layout. Good hot-plug module designs can minimize accidental pre-enables by carefully managing the connect pin strategy (ground then control

then Vcc) as well as using pull-ups on active low enables (and pull-downs on active high enables).

11.3 Product Features

- Near zero propagation delay (250ps typically)
- 5W switches connect input to outputs
- Direct us connection when switches are ON
- Fast Individual Enable (6ns typical)
- Ultra-Low Quiescent Power (0.2mA typical)
- Familiar 74xx125/126 footprint

  Packages: 14-pin 150 mil SOIC, 14-pin 300 mil P D I P or "1/4 size" 16-pin surface mount QSOP
- Quiescent power, package size and features are ideally suited for notebook applications.



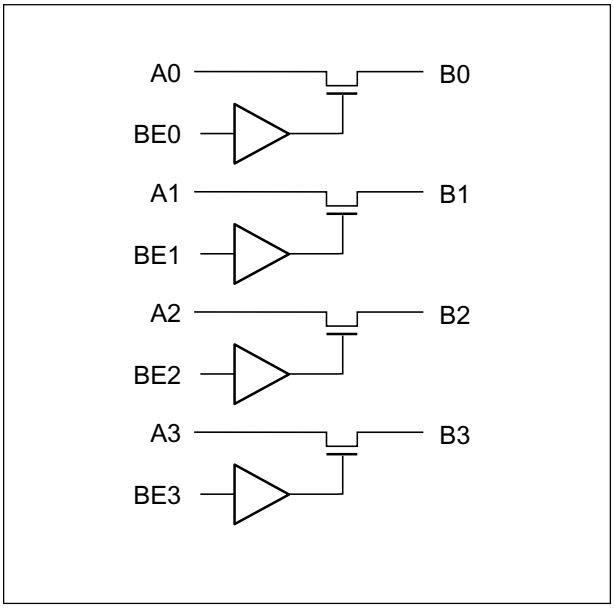
PI5C3125 Block Diagram

11.4 Product Description

Pericom Semiconductor's PI5C series of logic circuits are produced using the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

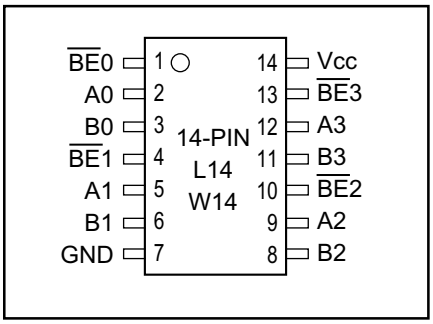
The PI5C3125 and PI5C3126 are 4-bit busswitches designed with 4 individual 5-ohm bus switches with fast individual enables in an industry standard 74XX125/126 pinout. When enabled via the associated Bus Enable (BE) pin, the "A" pin is directly connected to the "B" pin for that particular gate. The bus switch introduces no additional propagation delay or additional ground bounce noise.

The PI5C3125 device has active LOW enables, and the PI5C3126 has active HIGH enables.

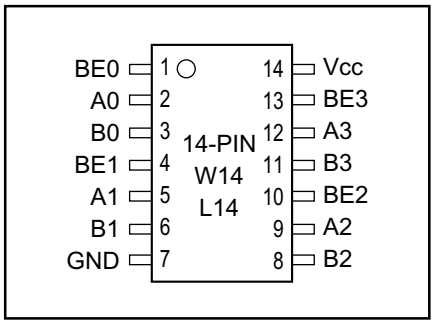


PI5C3126 Block Diagram

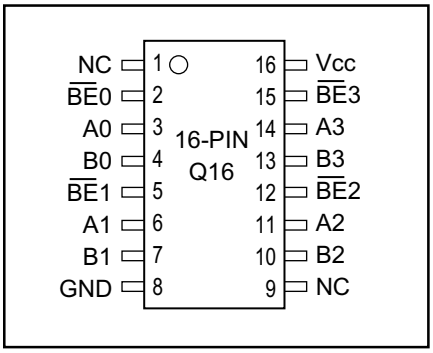
PI5C3125
14-Pin Product Pin Configuration



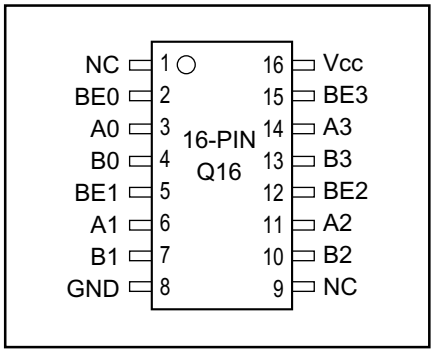
PI5C3126
14-Pin Product Pin Configuration



PI5C3125
16-Pin Product Pin Configuration



PI5C3126
16-Pin Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{BE}$n	Switch Enable (PI5C3125)
BEn	Switch Enable (PI5C3126)
A3-A0	Bus A
B3-B0	Bus B
Vcc	Power
GND	Ground

Truth Table(1)

PI5C3125 $\overline{BE}$n	PI5C3126 BEn	An	Bn	Vcc	Function
X*	X	Hi-Z	Hi-Z	GND	Disconnect
H	L	Hi-Z	Hi-Z	Vcc	Disconnect
L	H	Bn	An	Vcc	Connect

Notes:
1. H = High Voltage Level, L = Low Voltage Level
   Hi-Z = High Impedance, X = Don't Care
* A pull-up resistor should be provided for power-up protection.

Bus Switches as Multiplexer/Demultiplexer

Pericom offers four bus switch multiplexer/demultiplexers:

- ***PI5C3251 8:1 multiplexer/demultiplexer***
- ***PI5C3253 Dual 4:1 multiplexer/demultiplexer***
- ***PI5C3257 Qual 2:1 multiplexer/demultiplexer***
- ***PI5C3390 16:8 multiplexer/demultiplexer***

The first three are functionally pin-compatible with F-series multiplexers F251, F253, and F257, respectively.

Recall that a bus switch device, shown in Figure 1, when enabled, is equivalent to a 5-ohm resistor. The advantage of a bus switch device over an F-series multiplexer is that a bus switch device has nearly zero propagation delay. This is an ideal circuit for a system design, assuming that the output “A” providing the input signal to the bus switch device input "IN" can also drive the output load “L” of the bus switch device.

Figure 2 shows a 4:1 multiplexer PI5C3253. Selection signals S0 and S1 determine which one of the 4 input signals is connected to the output. This is exactly identical to the function of F253 multiplexer. Their pinouts are also identical.

Figure 3a shows a 4-bank circuit, whose output is tied together to produce a one data bit signal. Only one bank is enabled at a time. The output load is excessive and causes a slow down in throughput speed. Using a multiplexer, F253 or PI5C3253, the outputs from each bank are no longer tied together, and hence the load of each output is reduced to one quarter (see Figure 3b.) The data signal will be speeding up. If F253 is used, its 8ns propagation delay will slow down the circuit, but the zero propagation delay feature of the PI5C3253 bus switch will not slow it down.

Since a bus switch device, when enabled, is equivalent to a 5-ohm resistor, it is bidirectional. As a result, a multiplexer bus switch also can be used as a demultiplexer. Figure 4a illustrates an ASIC device driving an excessively overloaded circuit. Each bank is enabled by decoding certain upper address bits from the ASIC and only one bank is enabled at a time. Figure 4b shows that output A is now driving only two banks at one time, reducing the output loading to one half.

Designing a system with a large number of common bus signals always encounters two common problems:

1. Simultaneous switching of the address/data bus signals causes noise coupling and ground bounce on the adjacent signals traces, and
2. Large delay time caused by excessive capacitive loading from the large number of loads and long trace length.

The Pericom PI6C3xxx bus switch devices are ideal for solving these types of system problems because of their zero propagation delay, zero ground bounce, and low connection resistance (5 ohms) between an input pin and its output pin.

Figure 5a illustrates a large memory of eight banks, in which each address signal and each data signal are excessively loaded. Figure 5b shows the memory circuit can be improved by using a bus switch as both a demultiplexer and multiplexer. The PI6C3257 bus switch is used as a 2:1 demultiplexer to reduce the output load of the memory address bit MA0 to one half. PI6C3251 bus switch is used as a 8:1 multiplexer for a data bit D0 to reduce the output load of each D0-x to one-eighth. A significant performance increase and noise reduction can be achieved by the bus switch being used as demultiplexer and multiplexer, plus the zero propagation delay feature of the bus switch.

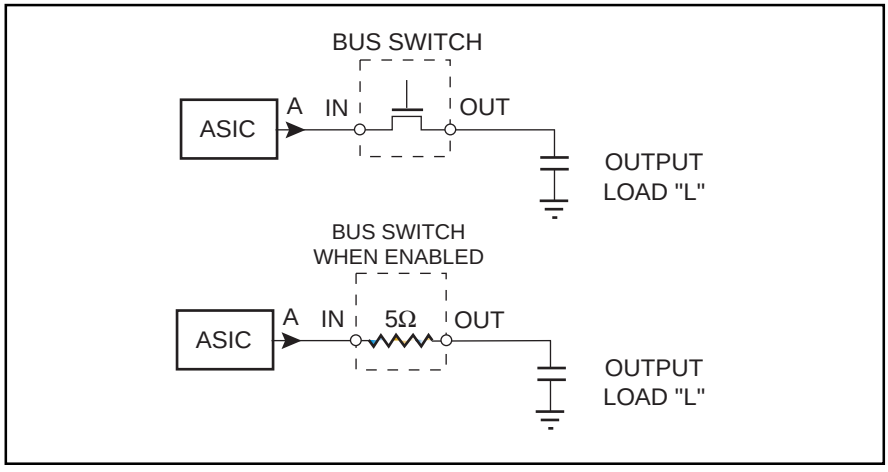


Figure 1. Equivalent Circuit of a Bus Switch

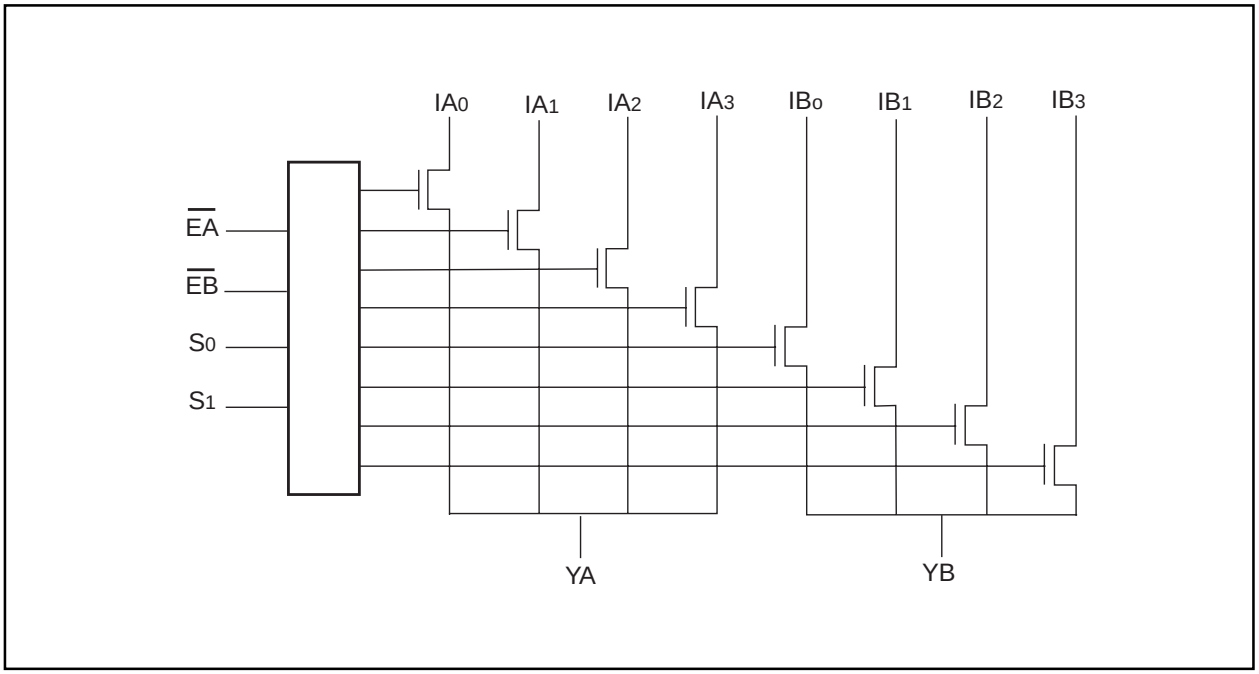


Figure 2. PI5C3253 Logic Block Diagram

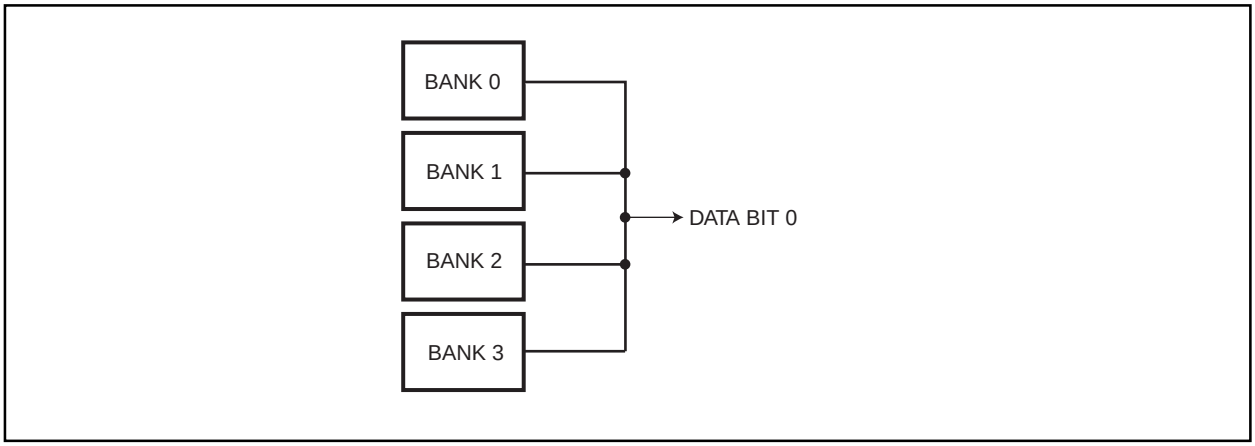


Figure 3a. Overloaded Data Bit

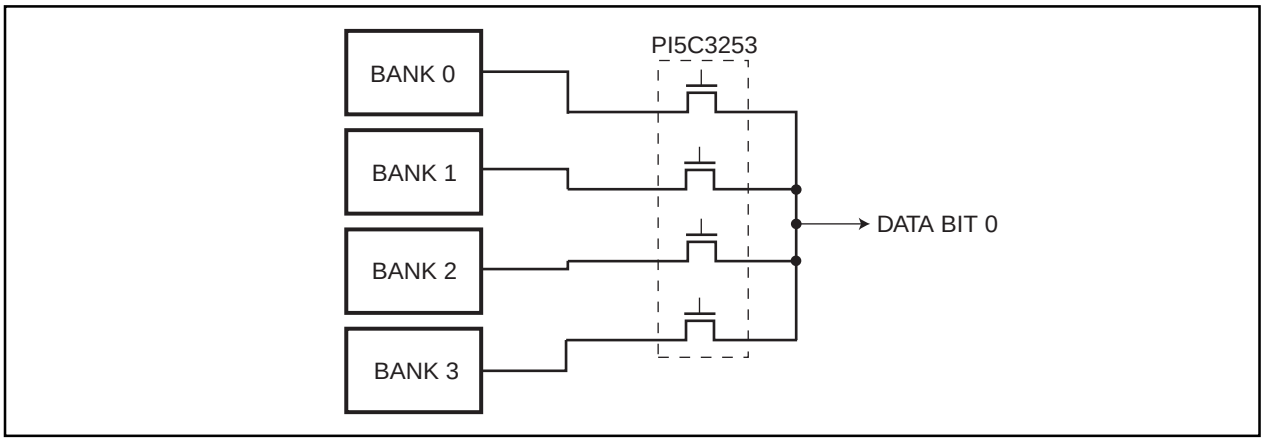


Figure 3b. Use PI5C3253 as a Multiplexer to Reduce Output Load and Increase Performance

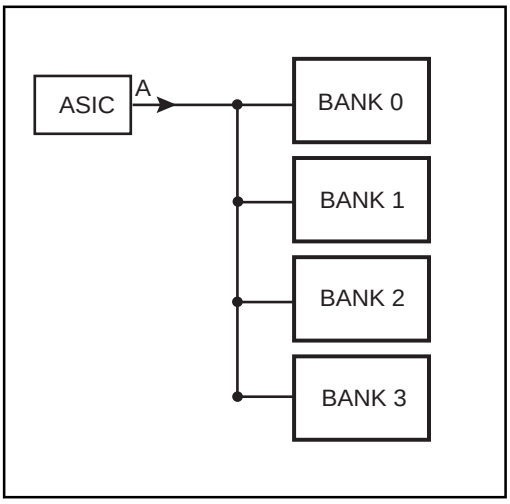


Figure 4a. The ASIC Output is Heavily Loaded by Four Banks of Circuits.

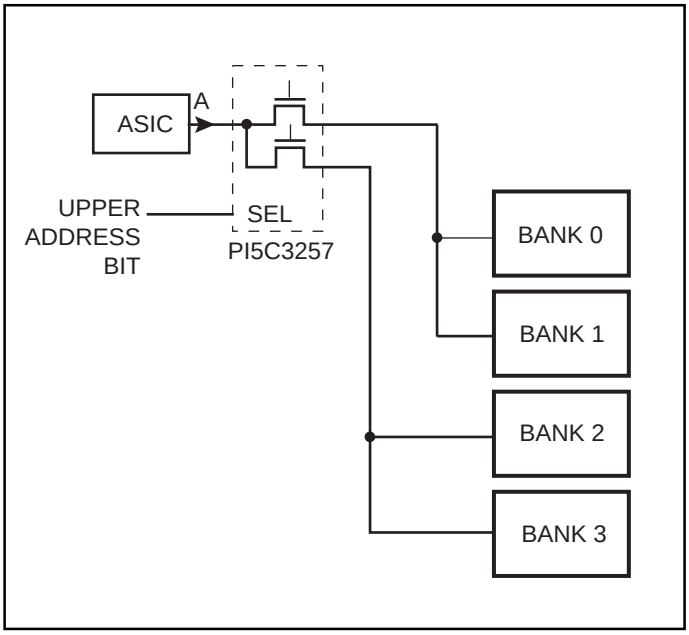


Figure 4b. Use PI5C3257 as a Demultiplexer to Reduce Output Load and Increase Performance.

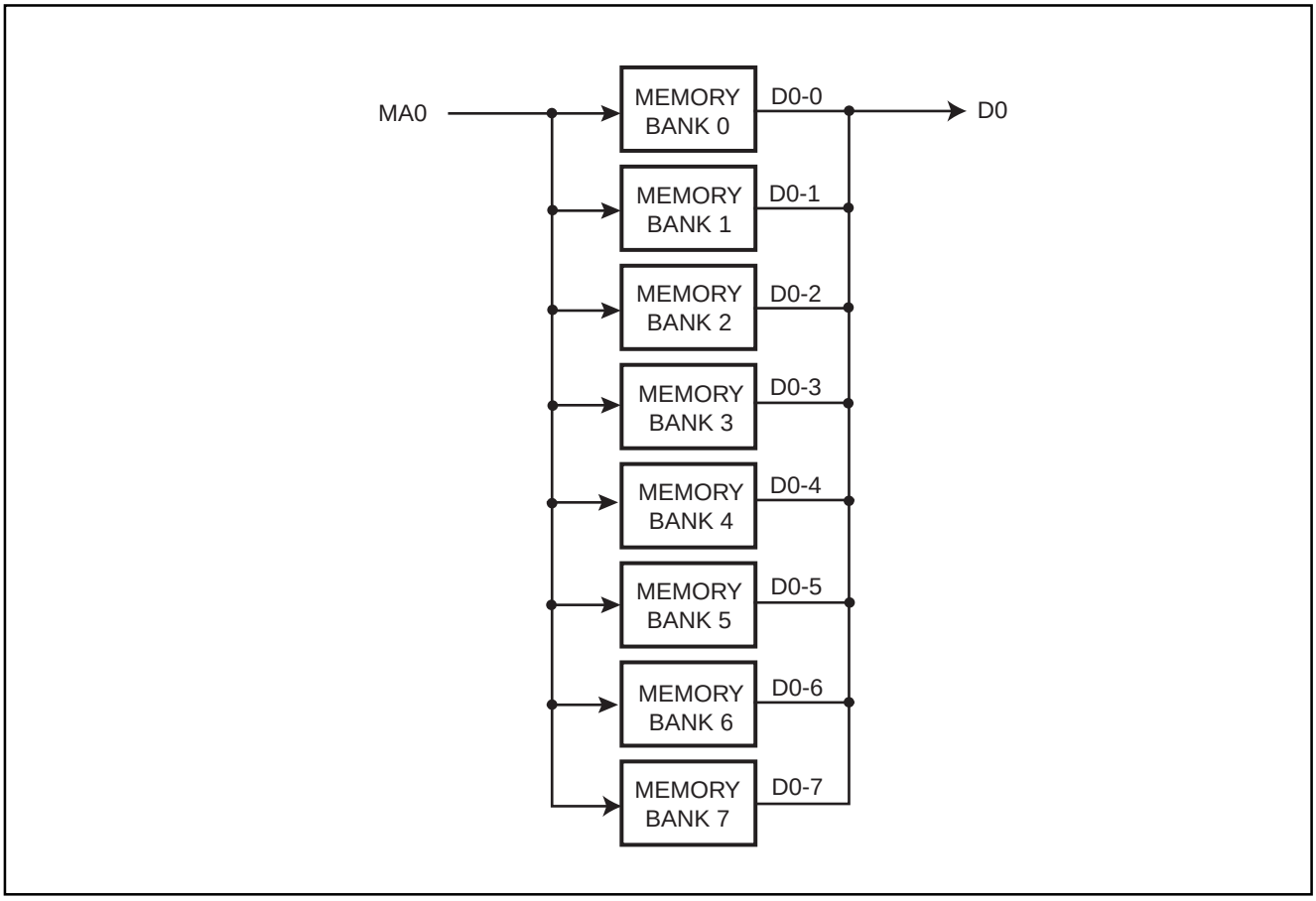


Figure 5a. A Large Memory of Eight Banks.

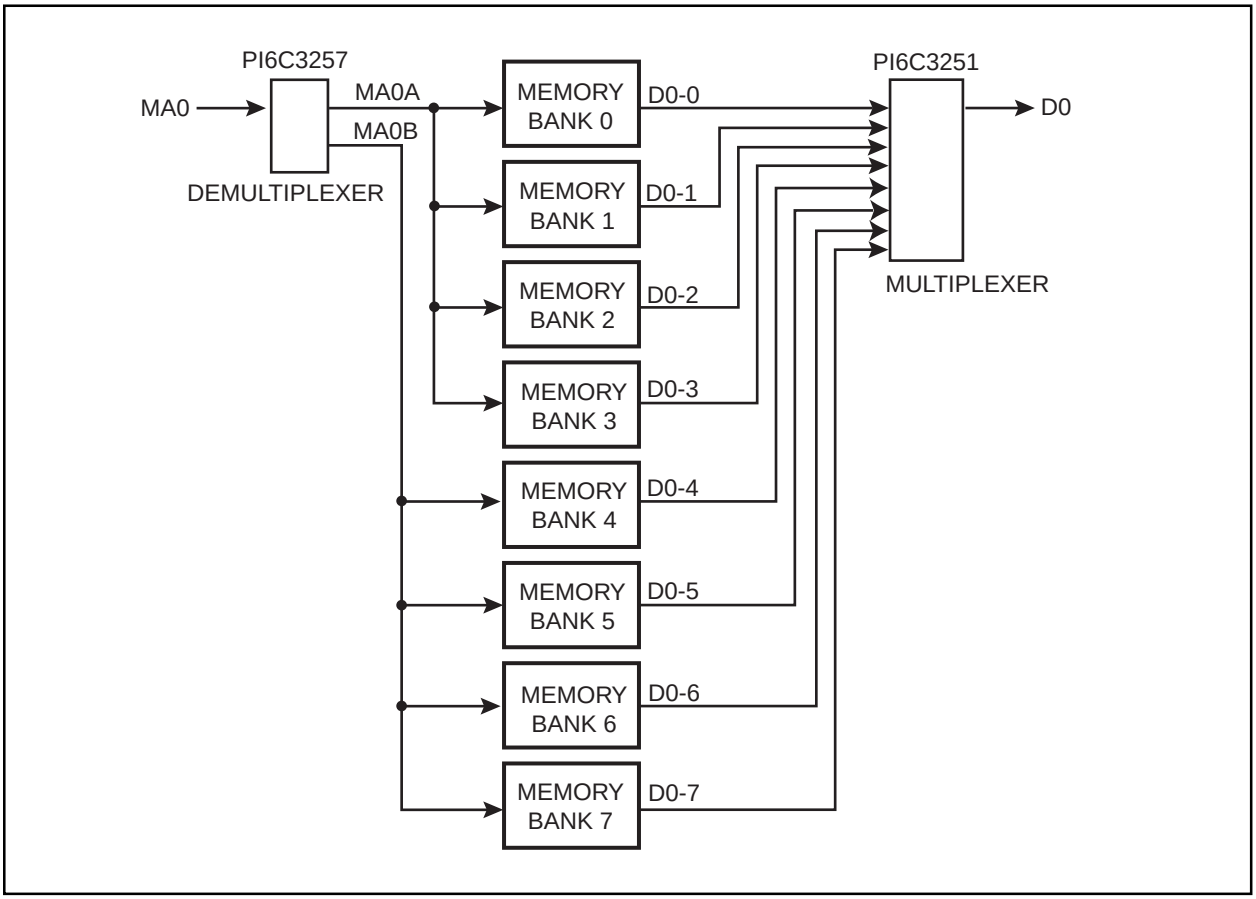


Figure 5b. A Large Memory of Eight Banks, Improved by Bus Switch Demultiplexer and Multiplexer.