

LOW CAPACITANCE TVS ARRAYS

APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ Cellular Phones
- ✓ Audio & Video Inputs
- ✓ Handheld Electronics
- ✓ FireWire, SCSI & USB Interfaces

IEC COMPATIBILITY (EN61000-4)

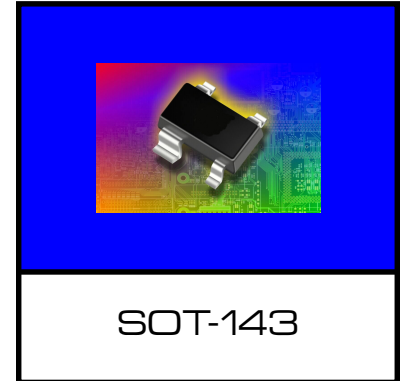
- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns

FEATURES

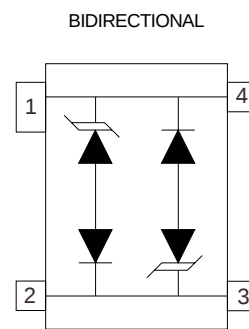
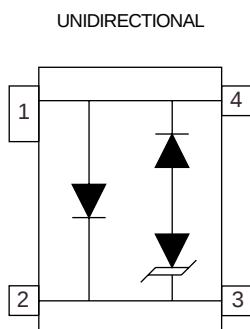
- ✓ ESD Protection > 40 kilovolts
- ✓ 350 Watts Peak Pulse Power per Line (8/20μs)
- ✓ Low Clamping Voltage
- ✓ Available in Multiple Voltage Types Ranging from 3V to 24V
- ✓ Unidirectional & Bidirectional Configurations
- ✓ **LOW CAPACITANCE - 10 pF**

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SOT-143
- ✓ Weight 0.1 grams (Approximate)
- ✓ Flammability Rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481-1-A
- ✓ Device Marking: Logo & Marking Code
- ✓ Pin One Defined By DOT on Top of Package



CIRCUIT DIAGRAMS



DEVICE CHARACTERISTICS

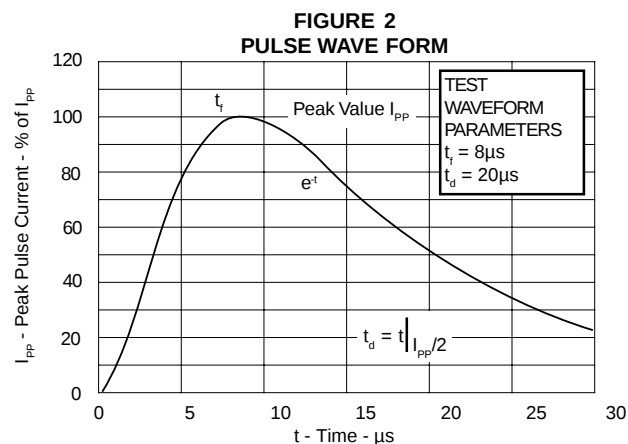
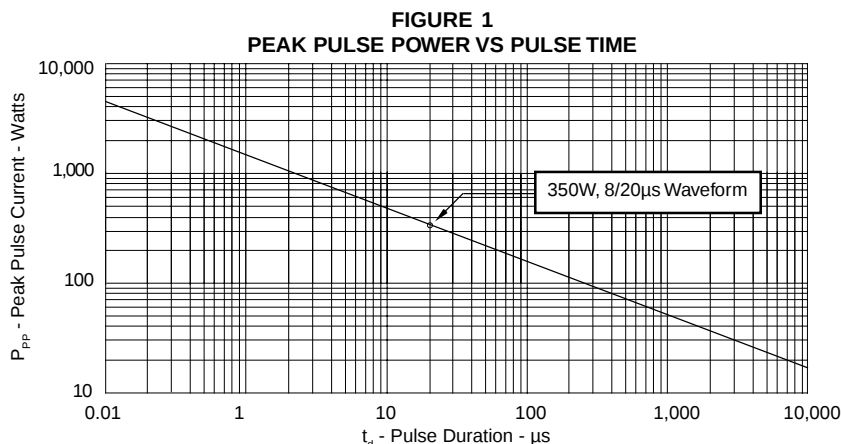
MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	350	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (See Notes 1, 2 & 3)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_p = 5A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20 μs $V_C @ I_{PP}$	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D μA	TYPICAL CAPACITANCE 0V @ 1 MHz C pF
PSLC03	3U	3.3	4.0	9.0	19.0V @ 20.0A	125	10
PSLC03C	3B	3.3	4.0	9.0	19.0V @ 20.0A	125	10
PSLC05	5U	5.0	6.0	11.0	18.3V @ 17.0A	20	10
PSLC05C	5B	5.0	6.0	11.0	18.3V @ 17.0A	20	10
PSLC08	8U	8.0	8.5	16.6	18.5V @ 17.0A	10	10
PSLC08C	8B	8.0	8.5	16.6	18.5V @ 17.0A	10	10
PSLC12	12U	12.0	13.3	24.0	28.6V @ 11.0A	1	10
PSLC12C	12B	12.0	13.3	24.0	28.6V @ 11.0A	1	10
PSLC15	15U	15.0	16.6	30.0	31.8V @ 10.0A	1	10
PSLC15C	15B	15.0	16.6	30.0	31.8V @ 10.0A	1	10
PSLC24	24U	24.0	26.7	N/A	56.0V @ 6.0A	1	10
PSLC24C	24B	24.0	26.7	N/A	56.0V @ 6.0A	1	10

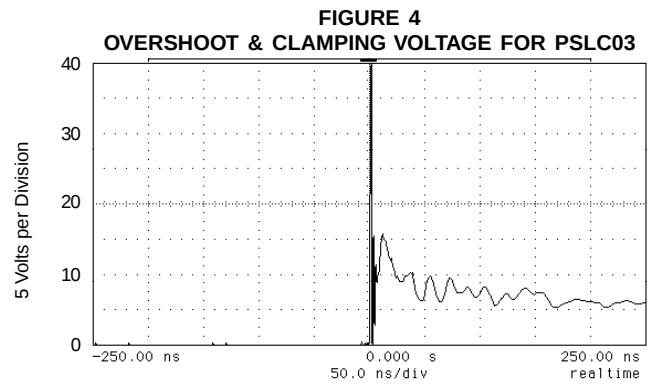
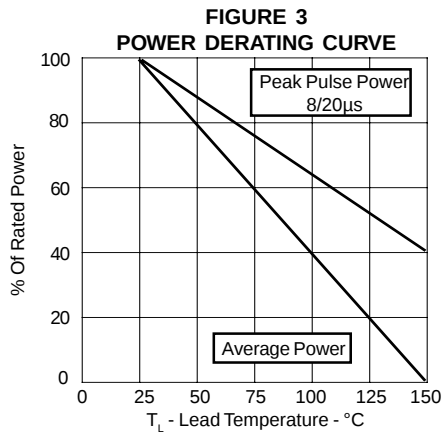
Note 1: Part numbers with an additional "C" suffix are bidirectional devices, i.e., PSLC05C.

Note 2: *Unidirectional Only:* Positive potential is applied from pin 2 to 1 or pin 3 to 4.

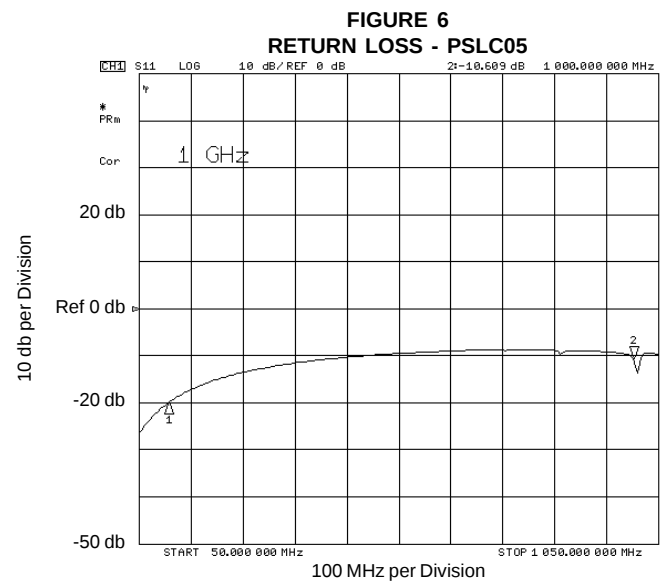
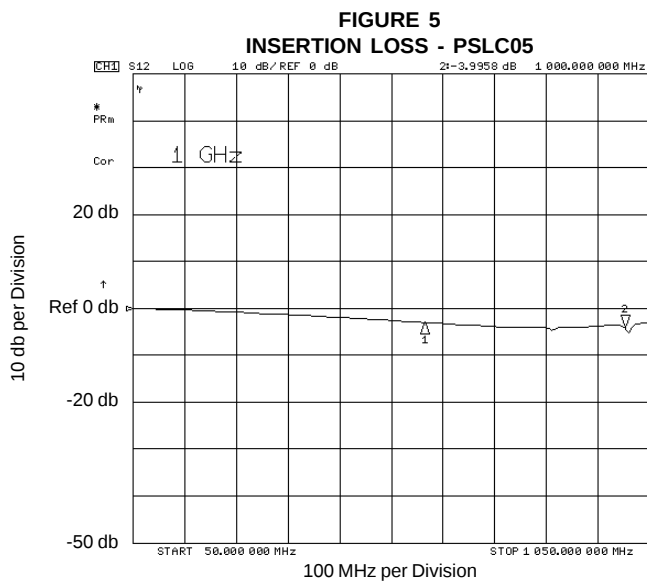
Note 3: Spice model and parameters for this series are available on the ProTek Devices web site: www.protekdevices.com.



GRAPHS



ESD Test Pulse: 5 kilovolt, 1/30ns (waveform)



APPLICATION NOTES

The PSLC Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD ($> 40\text{kV}$) or EFT. This product series provides both unidirectional and bidirectional protection, with a surge capability of 350 Watts P_{pp} per line for an $8/20\mu\text{s}$ waveform.

UNIDIRECTIONAL COMMON MODE CONFIGURATION (Figure 1)

The two PSLC Series devices provide protection in a common mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ TVS Device 1: Line 1(D+) is connected to Pins 2 & 3.
- ✓ TVS Device 2: Line 2(D-) is connected to Pins 2 & 3.
- ✓ Both TVS Devices: Pins 1 & 4 connected to ground.

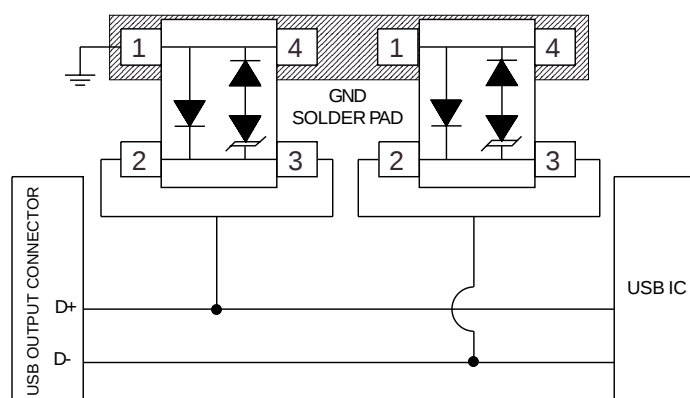


Figure 1 - Unidirectional Configuration (Two TVS Devices)
Common-Mode USB Protection

BIDIRECTIONAL DIFFERENTIAL MODE CONFIGURATION (Figure 2)

The PSLCxxC Series provides protection in a differential mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line 1(R_x) is connected to Pins 1 & 4.
- ✓ Line 2(T_x) is connected to Pins 2 & 3.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

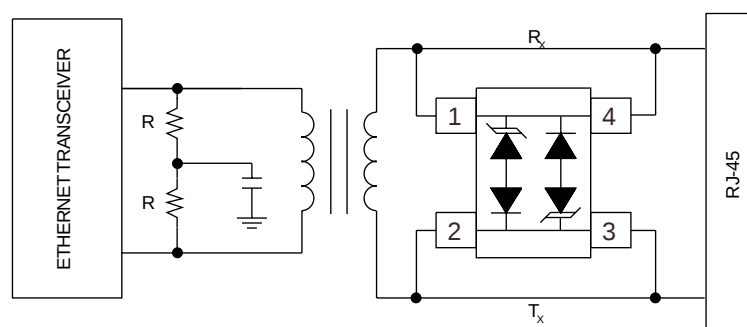
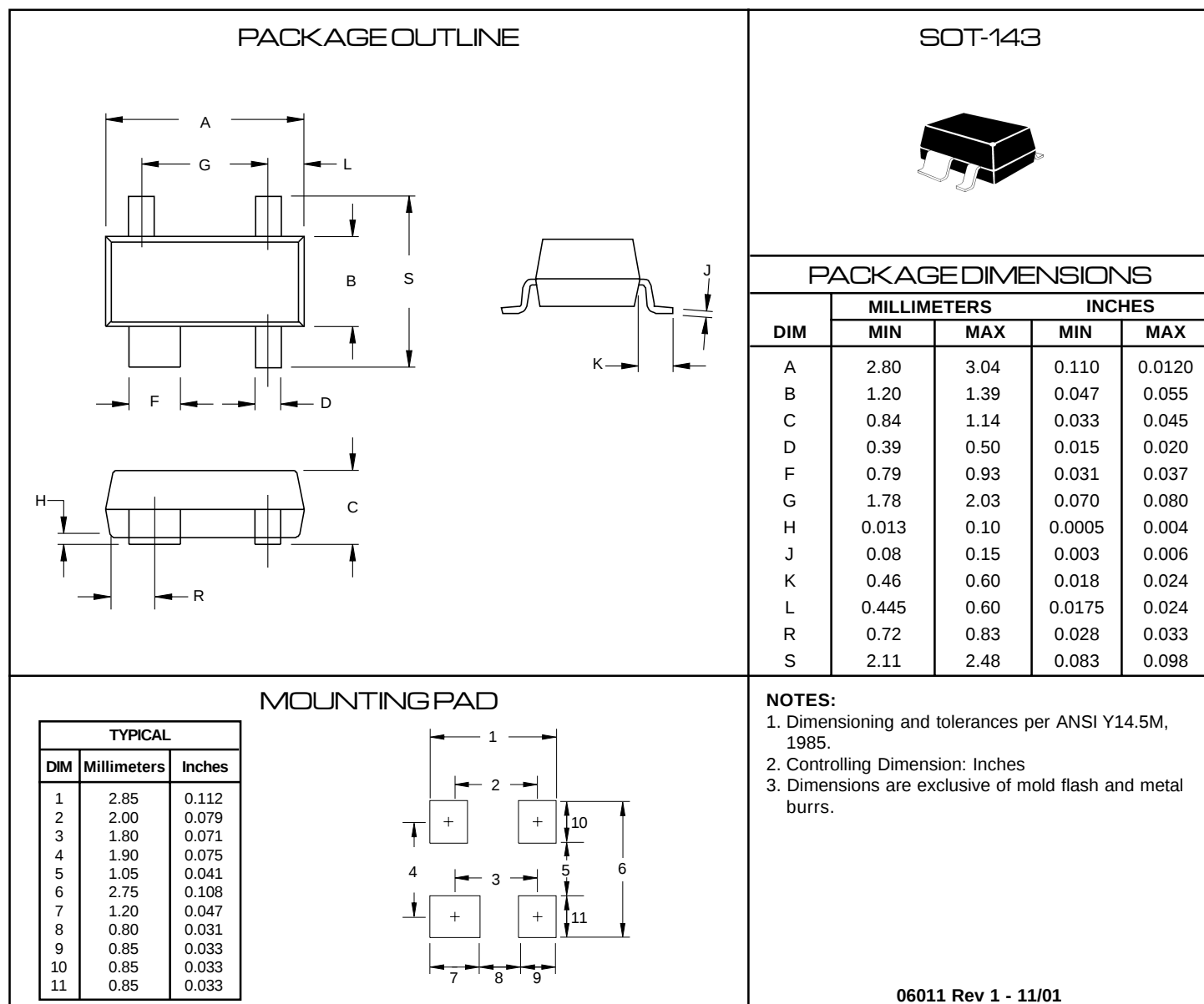


Figure 2 - Bidirectional Configuration
Differential-Mode Ethernet Protection

PACKAGE OUTLINE & DIMENSIONS



TAPE & REEL PACKAGING:

Surface mount product is taped and reeled in accordance with EIA-481, reel quantities and sizes are as follows:

7 Inch Reel - 3,000 pieces per reel; 13 Inch Reel - Not Available

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