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PB-1024
1-Inch CMOS Active-Pixel Digital Image Sensor

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May 2000 (Version 2.0)

Product Specification

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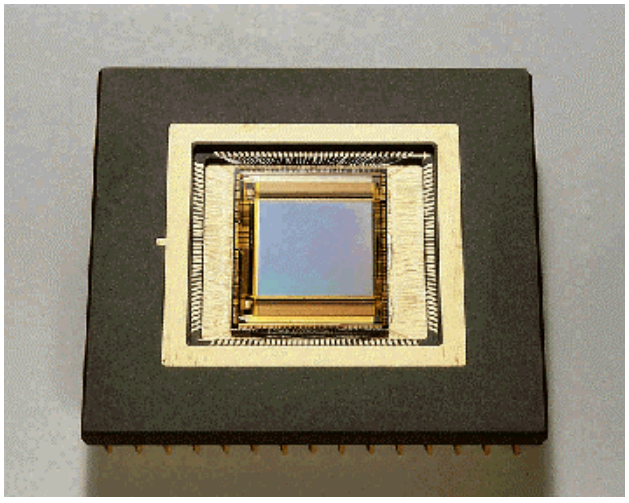


1.0 Introduction

- Photons-to-bits data stream
- 1024H x 1024V image resolution
- 10-micron-square active-pixel photodiodes
- 500 frames per second, progressive-scan
- 8-bit monochrome digital video
- Eight (8) parallel output ports
- 450 mW maximum power dissipation
- TrueBit® Noise Cancellation
- On-chip analog-to-digital converters
- 3.3-volt operation

1.1 Features

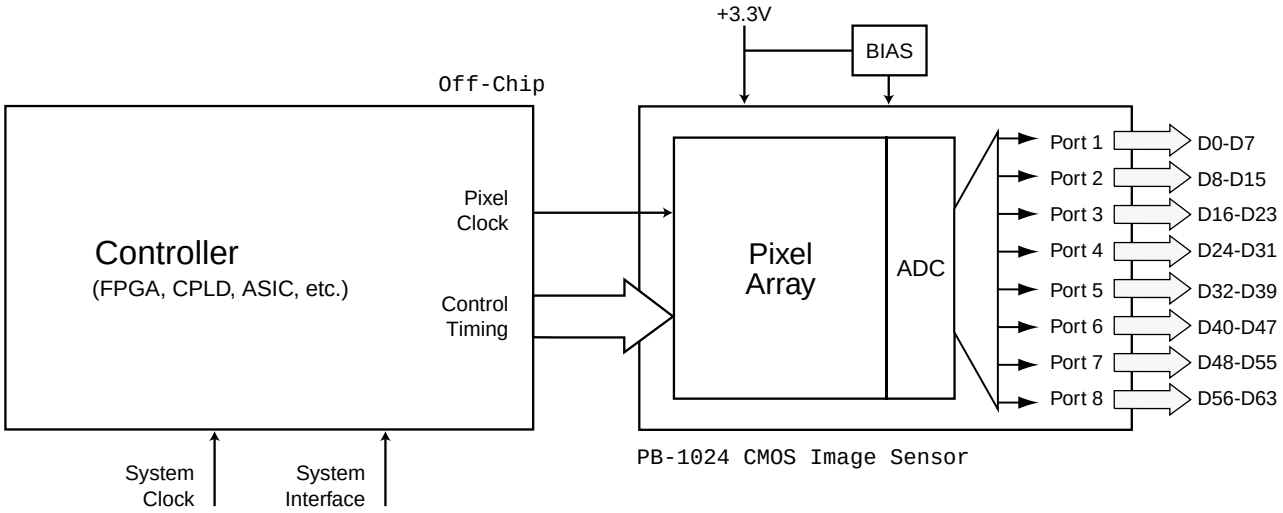
The PB-1024 is a 1024Hx1024V (megapixel) CMOS digital image sensor capable of 500 frames-per-second (fps) operation. It has on-chip 8-bit analog-to-digital converters (ADCs), which are self-calibrating, and a fully digital input interface. The chip's input clock rate is 66 MHz at 500 fps, for compatibility with many off-the-shelf interface components.

The sensor has eight (8) 8-bit-wide column-parallel digital output ports. Its design uses 0.5-micron technology and features an open architecture, to provide access to internal operations. ADC timing and pixel-read control are integrated on-chip. At 60 fps, the sensor dissipates less than 100 mW, and at 500 fps less than 450 mW; it operates on a 3.3V supply. Pixel size is 10 microns square and digital responsivity is about 500 bits per lux-second.

1.1 Features (continued)

The PB-1024 CMOS image sensor has an open architecture to provide access to its internal operations. A complete camera system can be built by using the chip in conjunction with the following external devices:

- An FPGA/CPLD/ASIC controller, to manage the timing signals needed for sensor operation.
- A 1-inch lens.
- Biasing resistors and bypass capacitors.

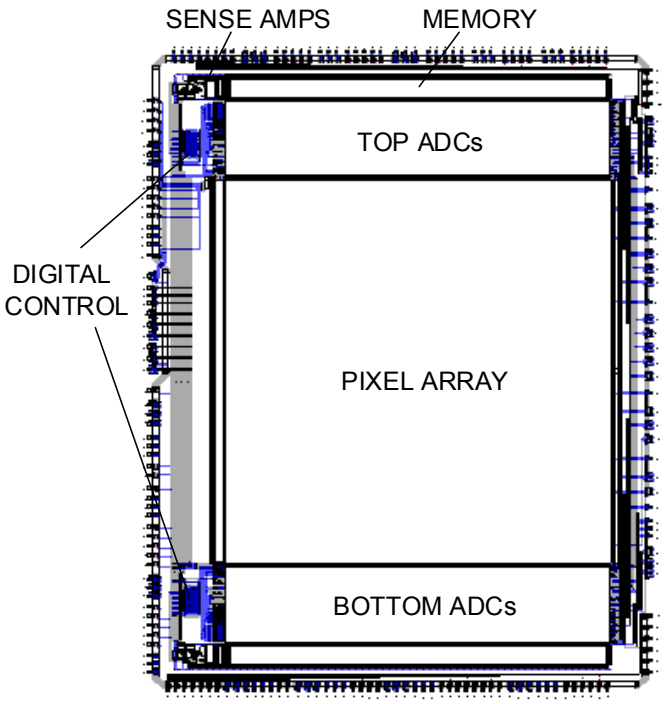


A Camera System Using the PB-1024 CMOS Image Sensor

1.2 Top-Level Specification

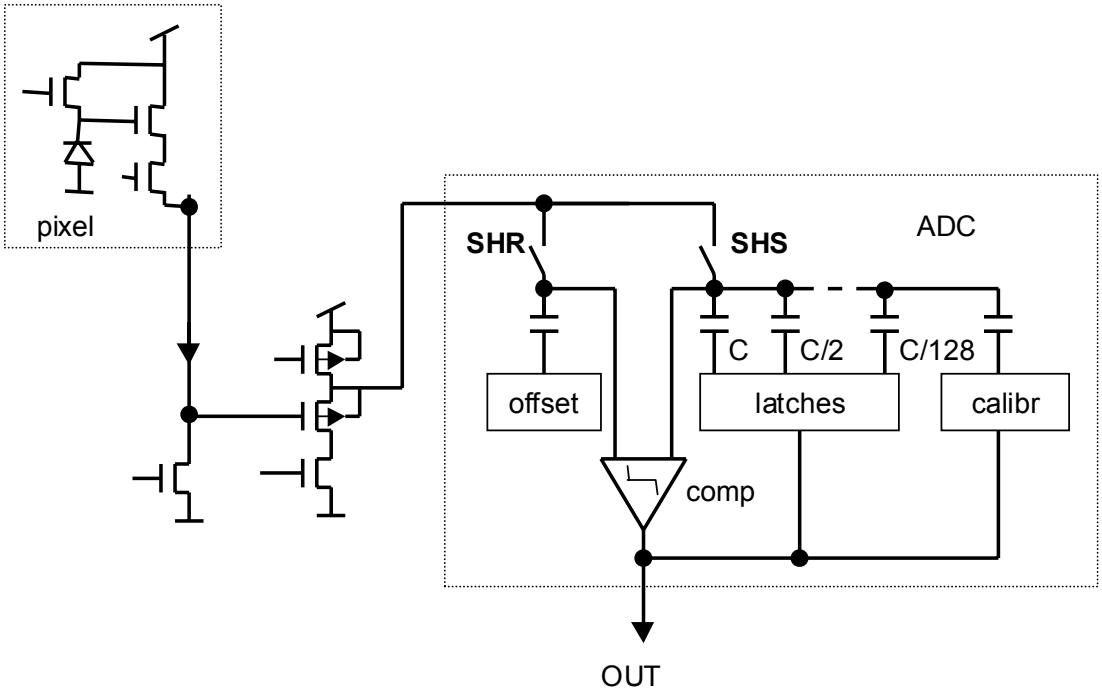
Array Format	1024H x 1024V 1:1 aspect ratio
Pixel Size and Type	10.0 µm x 10.0 µm active-pixel photodiode
Optical Format	1 inch
Frame Rate	0-500+ fps, progressive-scan (60, 120, 500 fps typical)
Output Data Rate	528 Mbytes/sec. (master clock 66 MHz, 500 fps)
Power Consumption	100 mW @ 60 fps 450 mW @ 500 fps
Digital Responsivity	500 bits per lux-second @ 550 nm ADC reference @ 1V
Internal Dynamic Range	64 dB
Supply Voltage	+3.3
Supply Current	140 mA nominal @ 500 fps
Operating Temperature	-5°C to +60°C
Output	8 ports
Shutter	Electronic rolling snap (ERS), up to 250 fps
ADC	On-chip 8-bit column-parallel (with >6.5 bit performance)
Package	145-pin ceramic PGA
Programmable Controls	Open architecture On-chip: • Basic ADC controls • Output multiplexing control • ADC calibration Off-chip: • Multiple windowing • Window size and location • Electronic pan and tilt • Frame rate and data rate • Integration time • ADC reference test mode

2.0 Electrical

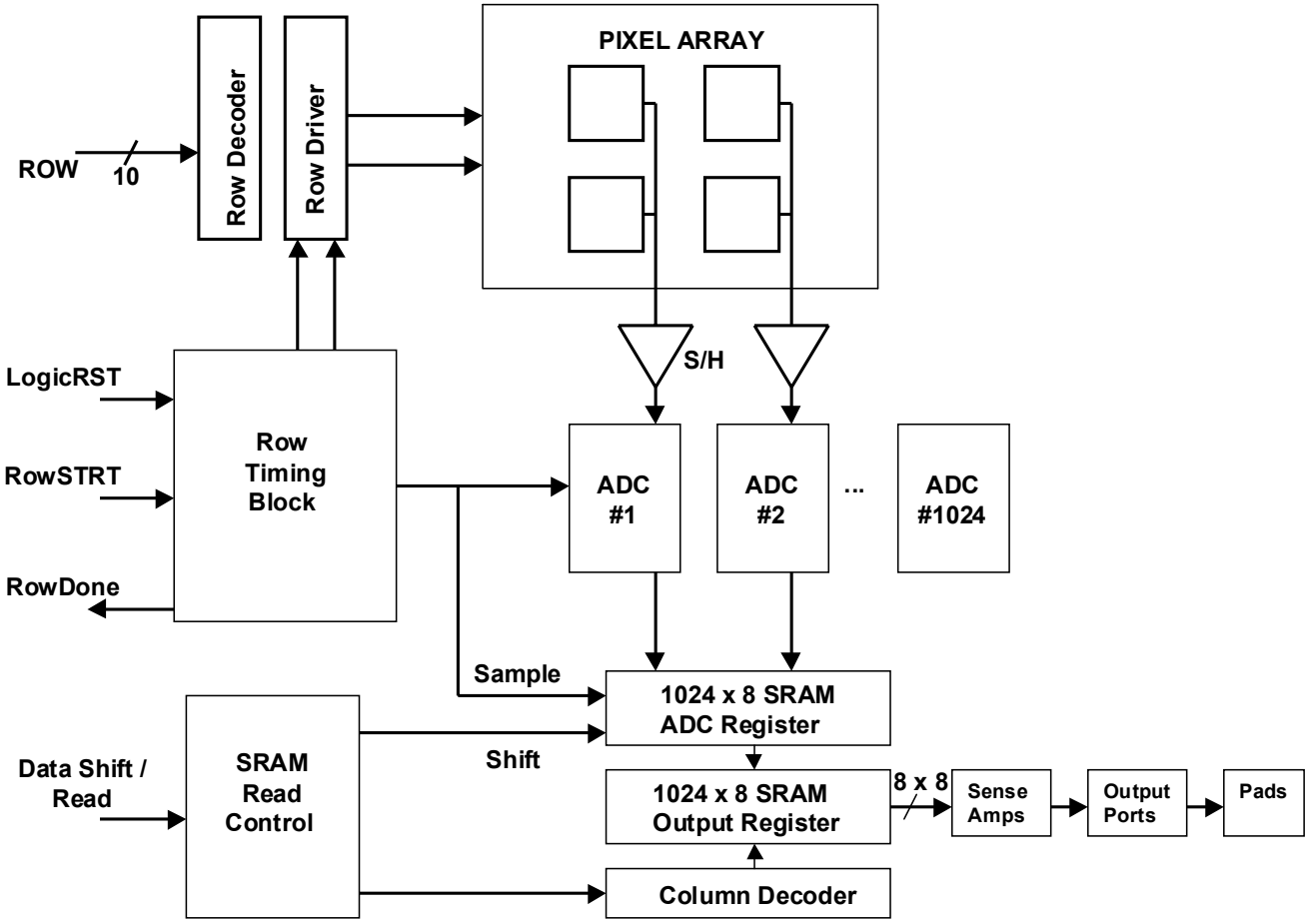


Sensor Architecture

2.1 Signal Path Diagram



2.2 Functional Block Layout



2.3 External Control Sequence

The PB-1024 includes on-chip timing and control circuitry to control most of the pixel, ADC, and output multiplexing operations. However, the sensor still requires a controller (FPGA, CPLD, ASIC, etc.) to guide it through the full sequence of its operation.

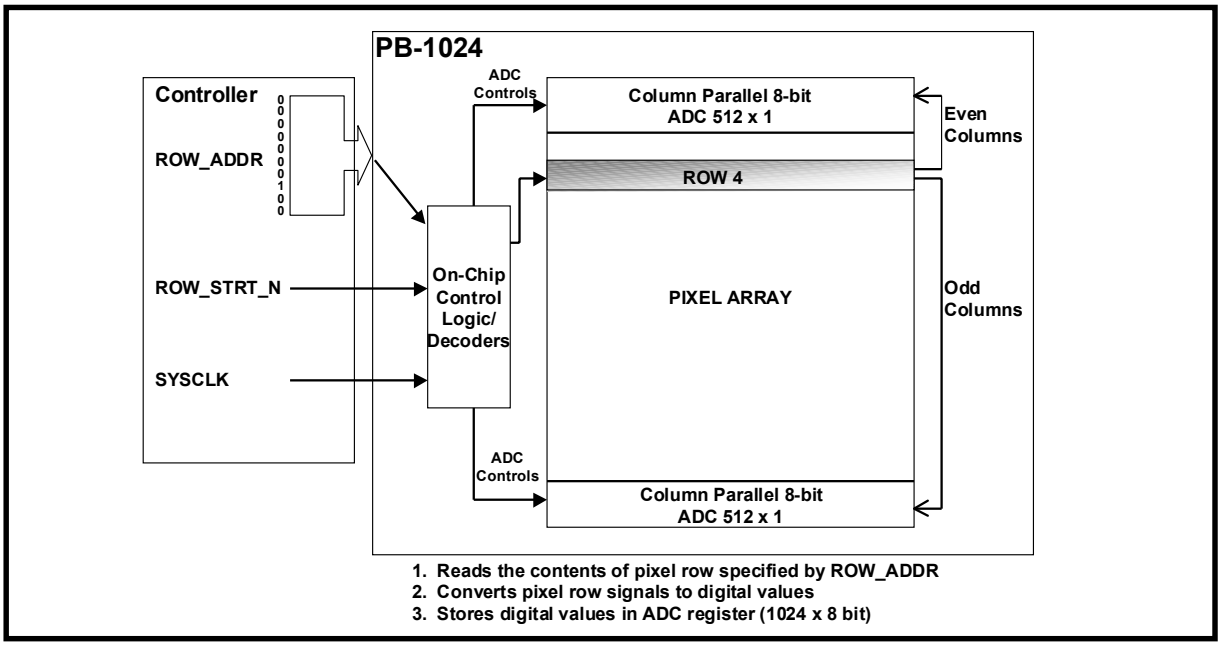
The sensor has a column-parallel ADC architecture that allows the array of 1,024 analog-to-digital converters on the chip to digitize simultaneously the analog data from an entire pixel row. The following input signals are utilized to control the conversion and readout process:

Signal Name	Description	Input Bus Width
ROW_ADDR	Row Address	10-bit
ROW_STRT_N	Row Start	1-bit
LD_SHFT_N	Load shift register	1-bit
DATA_READ_EN_N	Data read enable	1-bit

The 10-bit ROW_ADDR (row address) input bus selects the pixel row to be read for each readout cycle. The ROW_STRT_N signal starts the process of reading the analog data from the pixel row, the analog-to-digital conversion, and the storage of the digital values in the ADC registers. When these actions are completed, the sensor sends a response back to the system controller using the ROW_DONE_N. Row address must be valid for the first half of the row processing time (the period between ROW_START_N and ROW_DONE_N).

The PB-1024 contains a pipeline style memory array, which is used to store the data after digitization. This memory also allows the data from the previous row conversion cycle to be read while a new conversion is taking place.

The digital readout is controlled by lowering the LD_SHFT_N signal, followed by the DATA_READ_EN_N signal. LD_SHFT_N transfers the digitized data from the ADC register to the output register. DATA_READ_EN_N is used to enable the data output from the output register. A new pixel row readout and conversion cycle can be started two clock cycles after DATA_READ_EN_N is pulled low. The output register allows the reading of the digital data from the previous row to be performed at the same time as a new conversion (pipeline mode). This means that the total row time will be only that between when: (a) the ROW_STRT_N signal is applied and ROW_DONE_N is returned; and (b) LD_SHFT_N and DATA_READ_EN_N are applied plus two clock cycles. The pipelined operation means there will always be 1 row of latency at the start of sensor operation. The alternative to pipeline mode is sequential mode in which a new pixel row conversion is not initiated until after the output register is emptied (and LD_SHFT_N has been taken high). The ratio of line active and blanking times can be adjusted to easily match a variety of display and collection formats. **FOR ADDITIONAL INFORMATION AND EXPLANATION SEE SECTION 2.3.1.**



Example 1 - This example shows row 4 of the PB-1024 being digitized

2.3 External Control Sequence (continued)

ⓐ INTEGRATION TIME
This is not an input pin. It merely signifies that the particular row about to be read has been integrating light since it was previously selected. ♣ *This is only limited by the selection rate of the pixel row and the minimum row readout time (2 usec @ 66 MHz SYSCLK).*

ⓑ ROW_ADDR
The address for the pixel row to be read is input externally via this 10-bit input bus. *Must be valid for at least 68 SYSCLK cycles, must be valid when ROW_STRT_N is pulled low.*

ⓒ ROW_STRT_N
This signal:
i-Reads the contents of the pixel row specified by ROW_ADDR (ⓑ above)
ii-Converts pixel row signal to digital value
iii-Stores digital value in ADC register (1024 x 8-bit)
iv-Resets the pixel row
This process is completed in 132-133 SYSCLK cycles. Must be valid for a minimum of two clock cycles and a maximum of 100 clock cycles.*

ⓓ ROW_DONE_N
132-133* SYSCLK cycles after ROW_STRT_N has been pulled low (ⓒ above) the sensor acknowledges the completion of a row read operation/digitization by sending out a low going pulse on this pin. V*alid for two clock cycles.*

ⓔ LD_SHFT_N
This signal transfers the digitized data from the ADC register to the output register (1024 x 8-bit) and gates the power to the sense amplifiers. *May be enabled simultaneously with or after the rising edge of ROW_DONE_N. Must remain low the entire time the data is being read out.*

ⓕ DATA_READ_EN_N
This signal is used to enable the data output from the on-chip FIFO (1024 x 8-bit) to the eight, 8-bit output ports. *May be initiated simultaneously with or after LD_SHFT_N is selected. Minimum width is one clock cycle.*

ⓖ The pixel array of the PB-1024 image sensor is vertically partitioned into 128 groups of 8 columns that correspond to the sensor's eight (8) identical output ports.The first column of each 8-column set always goes to Port 1, while the last column of each set goes to Port 8, etc. The operator can access all pixels of the PB-1024 only by using all of its ports (see page 4).

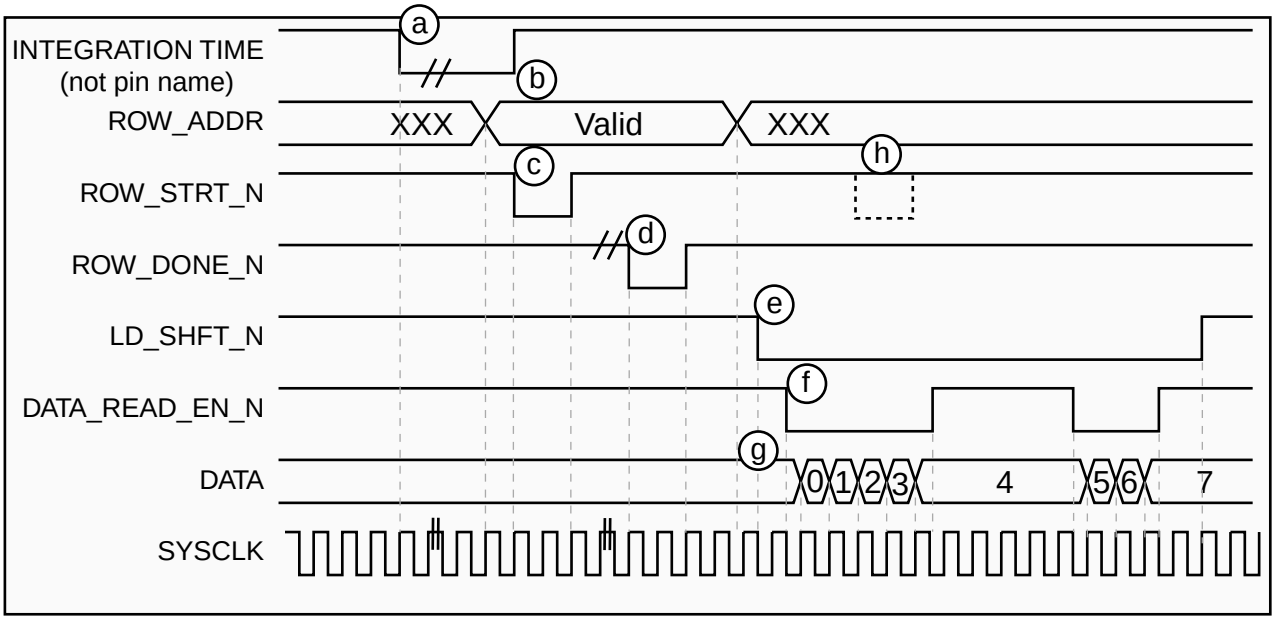
	CLK 1	CLK 2 ..... CLK128
Port 1	Col. 1	Col. 9 ..... Col. 1017
Port 2	Col. 2	Col. 10 ..... Col. 1018
Port 3	Col. 3	Col. 11 ..... Col. 1019
Port 4	Col. 4	Col. 12 ..... Col. 1020
Port 5	Col. 5	Col. 13 ..... Col. 1021
Port 6	Col. 6	Col. 14 ..... Col. 1022
Port 7	Col. 7	Col. 15 ..... Col. 1023
Port 8	Col. 8	Col. 16 ..... Col. 1024

ⓗ The use of an output register allows the processing of a row to be performed while the digital data from the previous operation is being read out of the sensor. A new pixel readout and conversion cycle can be started two clock cycles after DATA_READ_EN_N is pulled low.

***In order to minimize the sensor power consumption, the row processing circuitry operates at SYSCLK÷2. Therefore, depending on the user's implementation, there will be either 132 or 133 SYSCLK cycles between the start of ROW_STRT_N and ROW_DONE_N.**

♣In order to obtain the best performance from the initial image it is recommended that the user reset the entire pixel array to set the starting point of integration for this initial image. The timing for resetting the array should be identical to the frame time for the subsequent image.

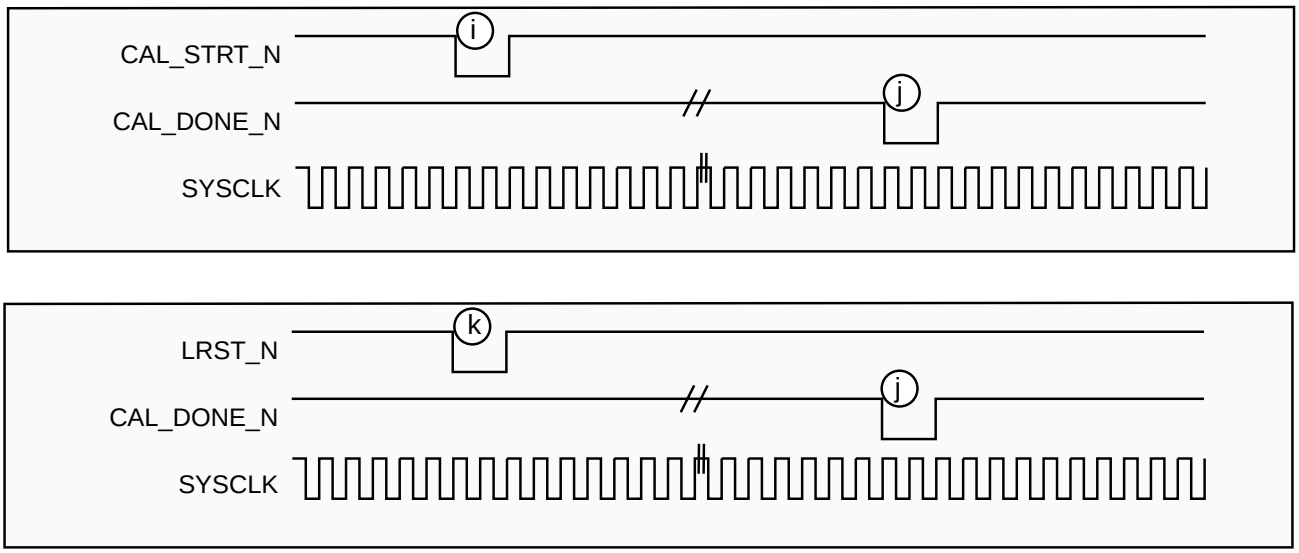
2.3 External Control Sequence (continued)



Typical I/O Signal Timing (Read Sequence)

2.3 External Control Sequence (continued)

The PB-1024 contains special self-calibrating circuitry that enables it to reduce its own fixed-pattern noise. This calibration process consists of connecting a calibration signal (VREF2) to each of the ADC inputs, and estimating and storing these offsets (5 bits) to subtract from subsequent samples. The Typical I/O Signal Timing (Initialization Sequence) diagram shows the timing sequence to calibrate the sensor. Calibration occurs automatically after logic reset (LRST_N) but it can also be started by the user, by pulling CAL_STRT_N low. When calibration is finished, the sensor generates the active low CAL_DONE_N.



Typical I/O Signal Timing (Initialization Sequence)

ⓘ CAL_STRT_N is a two-clock cycle-wide active-low pulse that initiates the ADC calibration sequence. The pulse must not be actuated for 1 microsecond after either power-up or removal of the sensor from a power-down state. Users may find it easiest to calibrate by means of the logic reset.

ⓙ CAL_DONE_N is a two-clock cycle-wide active-low output pulse that is asserted when the ADC calibration is complete. The device will automatically initiate a calibration sequence upon a logic reset. Completion of this sequence, in cases where it is initiated by a reset, is still with the CAL_DONE_N signal. This process is complete within 133 SYSCLK cycles of CAL_STRT_N. This process is complete within 133 SYSCLK cycles of LRST_N.

ⓚ LRST_N is a two-clock cycle-wide active-low pulse that resets the digital logic. It puts all logic into a known state (all flip-flops are reset). This signal also initiates an ADC calibration sequence.

2.3 External Control Sequence (continued)

2.3.1 Special Considerations

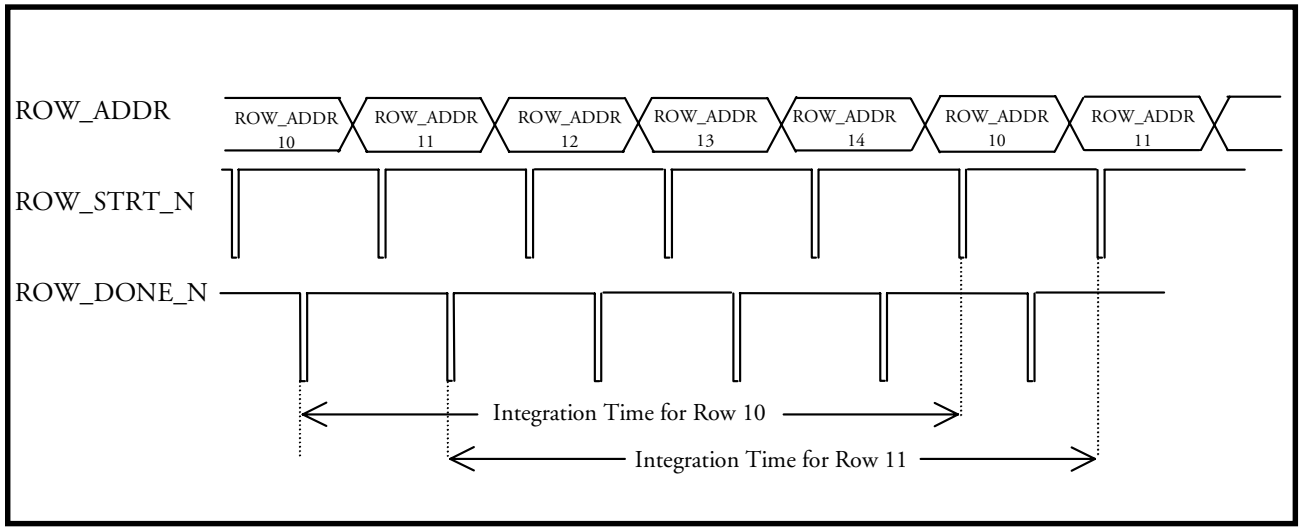
There are two synchronous 7-bit counters on the PB-1024 sensor which control the selection of SRAM columns. During full-speed operation, these counters increment on every rising clock edge, and 64 bits of new image data appear on the data pins. In the event that the device reading the sensor cannot keep up with the data stream, the ability to pause the data readout was included. The pause request is initiated by bringing the DATA_READ_EN_N line high prior to the next rising clock edge. This causes the output data to be latched while the counter is disabled from counting to the next block of columns.

The counter operates correctly during full-speed operation, when no attempt is made to disable the counter. However, due to an error in the next-state logic, the counter does not always operate correctly when it is disabled. The counter can be disabled correctly when the LSB of the current count is 0, i.e. when the current count value is even. However, when the LSB of the current count is 1 (odd), the rising edge of the clock will cause the counter to count by +2, to the next odd value. The counter will continue to count by 2's until the DATA_READ_EN_N line is brought low. The easiest work-around is to never disable the sensor readout on an odd column value.

2.4 Electronic Shutter

2.4.1 Non-ERS Mode

The PB-1024 can be operated in an electronic rolling shutter (ERS) mode to control the sensor integration time. In a normal, non-ERS read mode, a single address pointer is used to read data from (and reset) each row of pixels. This is done by changing the row address using ROW_ADDR to point to the appropriate row on the sensor. In a typical video application, a sequence of rows is read out repeatedly. The integration time of a row is set by the time elapsed between successive selection of a particular row (a row is selected using the ROW_ADDR and pulsing ROW_STRT_N). Please recall from Section 2.3 that ROW_STRT_N both reads and resets the row specified by ROW_ADDR. The integration time is simply the inverse of the frame rate (i.e. 60fps →16 msec integration time) in this mode.



Example 2 - Reading a window of 5 rows (starting with row 10 of the array) without ERS

2.4 Electronic Shutter (continued)

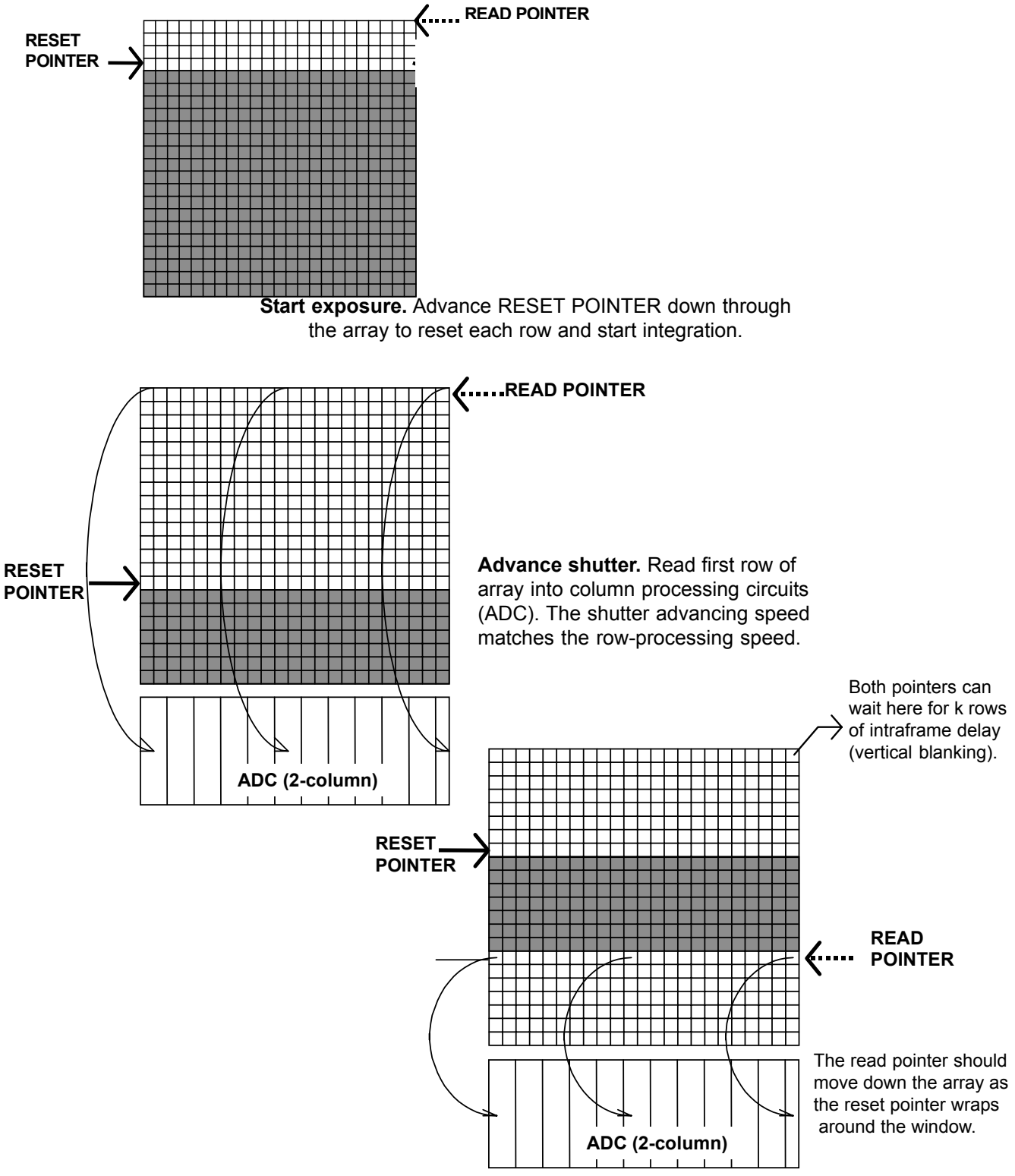
2.4.2 ERS Mode

In most applications, it is desirable to change the integration time (due to light intensity variation, etc.) while keeping the frame rate constant. For these applications, the PB-1024 can be operated in the ERS mode. The ERS operates up to 250 frames per second. In the ERS mode, two address pointers are used in each row read cycle. Both of these address pointers are controlled by the user-supplied ROW_ADDR input. Please recall from Section 2.3 that ROW_STRT_N both reads and resets the row specified by ROW_ADDR. In each row cycle, the first address (RESET POINTER♣) is used only to reset a row. This sets the starting point of integration for that row. The second address (READ POINTER♣) is used to read the data from another row. The row read by the READ POINTER had been reset by the RESET POINTER during a previous cycle. The difference between the value of the READ POINTER and the RESET POINTER sets the integration time. After system power-up, the user should move the RESET POINTER along the pixel array, row by row, while the READ POINTER stays in place. When the RESET POINTER reaches the desired row number and integration time, the READ POINTER should start moving along the pixel array. When the READ POINTER reaches the bottom (last row) of the pixel array, it should wrap around and go back to the top. The RESET POINTER should never catch up with the READ POINTER. In cases where integration time is longer than one full frame, the RESET POINTER should stop at the top of pixel array after it resets the whole array. Once the pixel array is wholly exposed to the desired integration time, the READ POINTER should start moving. The ERS illustration is shown in Example 3.

♣RESET POINTER and READ POINTER are not signals generated by the sensor but rather user-generated constructs utilized here to illustrate the ERS concept.

2.4 Electronic Shutter (continued)

2.4.2 ERS Mode (continued)

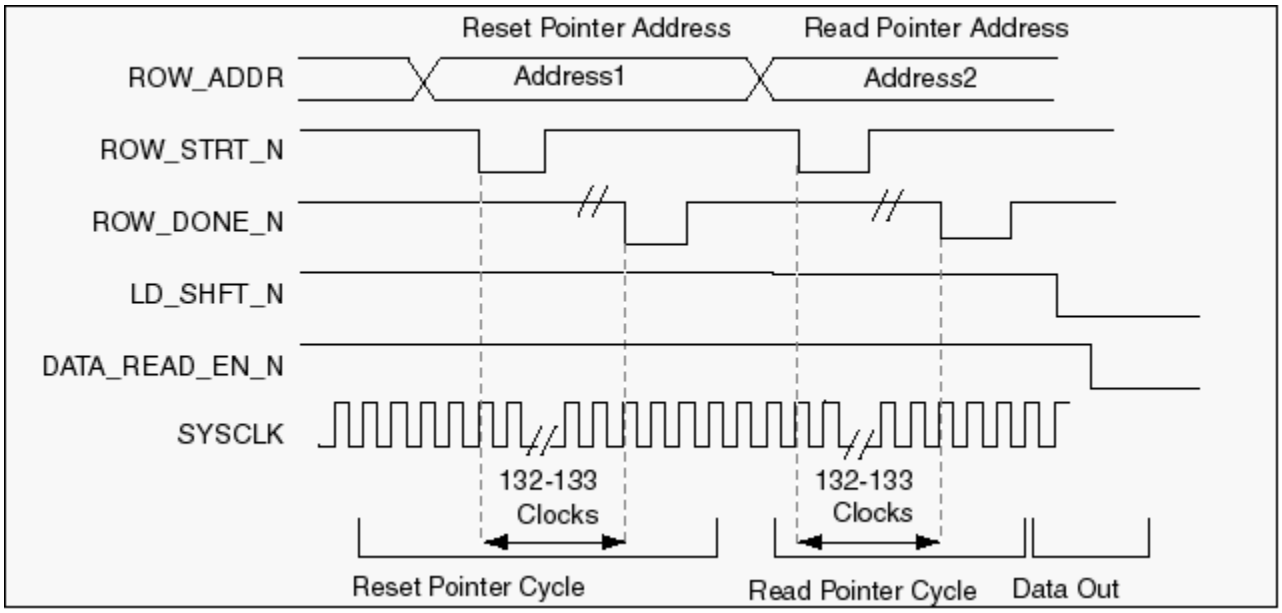


Example 3 - ERS Illustration

2.4 Electronic Shutter (continued)

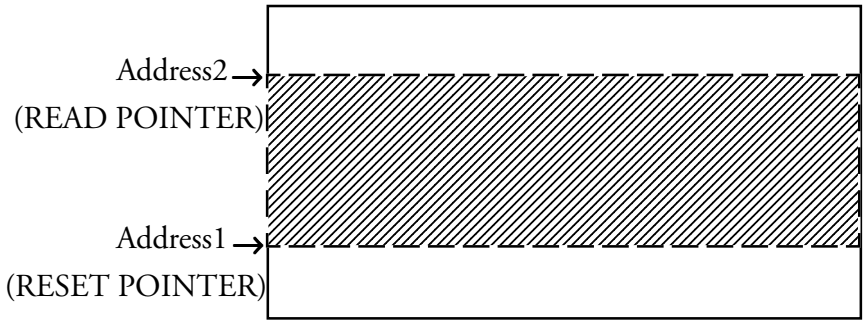
2.4.2 ERS Mode (continued)

The ERS Mode Row Read Cycle diagram indicates the signal relationships for ERS mode. Address1 is the reset pointer address. ROW_STRT_N is only used to reset this row. After the pixel row in Address1 is reset, jump to Address 2 (read pointer). ROW_STRT_N is used to read data from Address2.



ERS Mode Row Read Cycle

Example 4 illustrates the ERS pictorially. In this example, Integration time = (Address1 - Address2) * (Row Time). For example, if Row Time is set to 2 µsec (~66 MHz clock), and the user wants 1 msec integration time, set Address1 = Address2 + 500. The minimum integration time is one row time.



Example 4 - The ERS

2.5 Pin Descriptions

Signal Name	Function	Pin Number(s)
VAA	Power supply for pixel array, analog processing circuitry (column buffers, ADC, and support).	C15, F13, H14 J14, D14, L15, H1
AGND	Ground for analog signal processing circuitry.	D15, F14, H15, J13
AGND_SHIELD	Quiet analog ground for on-chip shielding. Can be connected to AGND.	E13, K14
CAL_DONE_N	A two-clock cycle-wide active-low pulse that indicates the ADC has completed its calibration operation.	K2
CAL_STRT_N	Starts the calibration process for the ADC. This is a two-clock cycle-wide active-low pulse.	L2
DARK_OFF_EN_N	A low input enables the dark offset cancellation function (VCLAMP3 and VREF3). Subtracts a fixed offset pre-ADC. Signal is pulled up on-chip.	N3
DATA_READ_EN_N	An active-low envelope signal that enables the column counter and causes the eight (8) 8-bit output ports to be updated with data on the rising edge of the system clock. Column counter is disabled when this input is high, and when counter is on an even column. Counter counts by 2 when this input is high, and when counter is on an odd column.	K1
SEE SECTION 2.3.1 FOR ADDITIONAL INFORMATION AND EXPLANATION.		
DATA [63:0]	Pixel data output bus that is eight pixels (64 bits) wide. Bit 0 is the LSB (least significant bit) of the lowest order pixel. In the group of eight pixels being output, bit 7 is the MSB (most significant bit).	
DATA0		L13
DATA1		M14
DATA2		P15
DATA3		N14
DATA4		M13
DATA5		P14
DATA6		N13
DATA7		N12
DATA8		C13
DATA9		B14
DATA10		A15
DATA11		B13
DATA12		A14
DATA13		B12
DATA14		C11
DATA15		A13
DATA16		R14
DATA17		P13
DATA18		N11
DATA19		R12
DATA20		P11

2.5 Pin Descriptions (continued)

Signal Name	Function	Pin Number(s)
DATA21		R11
DATA22		N10
DATA23		P10
DATA24		A12
DATA25		C10
DATA26		B10
DATA27		A11
DATA28		C9
DATA29		A10
DATA30		A9
DATA31		B8
DATA32		P9
DATA33		R10
DATA34		R9
DATA35		R8
DATA36		P8
DATA37		R7
DATA38		R6
DATA39		R5
DATA40		A8
DATA41		C7
DATA42		A7
DATA43		A6
DATA44		B7
DATA45		B6
DATA46		A5
DATA47		B5
DATA48		P6
DATA49		P5
DATA50		R3
DATA51		N5
DATA52		P4
DATA53		R2
DATA54		P3
DATA55		N4
DATA56		A4
DATA57		A3
DATA58		B4
DATA59		B3
DATA60		A2
DATA61		C4
DATA62		C3
DATA63		B2
VDD	Power supply for core digital circuitry.	B15, H2, M15

2.5 Pin Descriptions (continued)

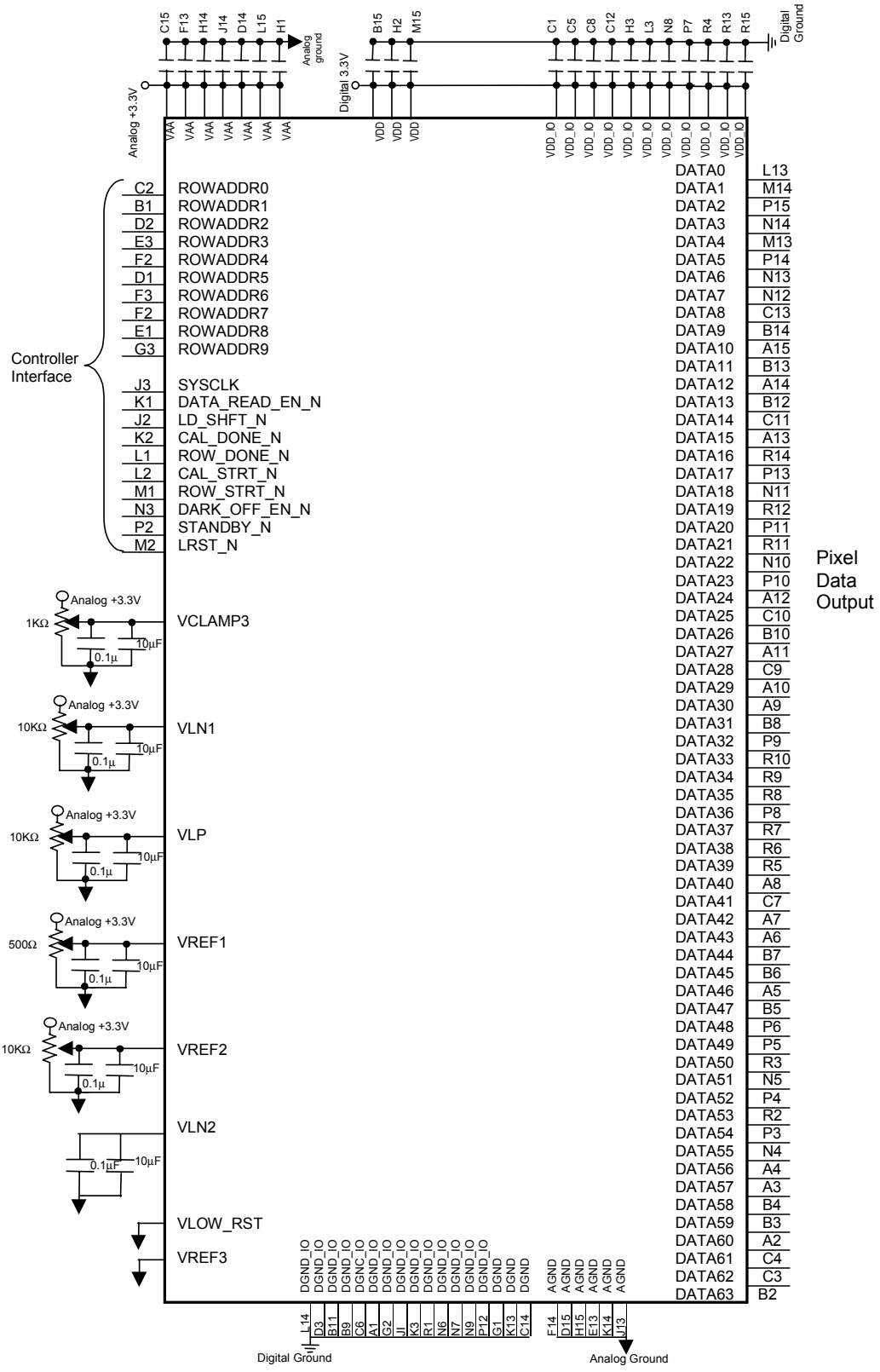
Signal Name	Function	Pin Number(s)
DGND	Ground for core digital circuitry.	C14, G1, K13
LD_SHFT_N	An active-low envelope signal that places the recently converted row of data into output register for output, enables the sense amps and resets the column counter.	J2
LRST_N	Global logic reset function (asynchronous). Active-low pulse.	M2
ROW_ADDR [9:0]	10-bit bus (0 to 1023, bottom to top) that controls which pixel row is being processed or read out. An asychronous (unclocked) digital input. Must be held valid for at least 70 SYSCLK cycles. Bit 9 is the MSB.	
ROW_ADDR0	.....	C2
ROW_ADDR1	.....	B1
ROW_ADDR2	.....	D2
ROW_ADDR3	.....	E3
ROW_ADDR4	.....	E2
ROW_ADDR5	.....	D1
ROW_ADDR6	.....	F3
ROW_ADDR7	.....	F2
ROW_ADDR8	.....	E1
ROW_ADDR9	.....	G3
ROW_DONE_N	A two-cycle-wide pulse that indicates that processing of the currently addressed row has been completed.	L1
ROW_STRT_N	Starts ADC conversion of the pixel row (defined by the row address) content. A two-clock cycle-wide active-low pulse.	M1
STANDBY_N	A low input sets the sensor in a low power mode. (Allow 1 microsecond before calibrating, after coming out of this mode). Signal is pulled up on-chip.	P2
SYSCLK	Clock input for entire chip. Maximum design frequency is 80 MHz (50%, ±5%, duty cycle).	J3
VCLAMP3	Dark offset cancellation negative input reference. Adjustable external voltage from 0 to 0.5V is recommended. User voltage source must supply a transient current of 40 mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND_SHIELD of ~0.1 µF to 1 µF is usually sufficient to filter out this required current transient.	E15
VDD_IO	Power supply for digital pad ring.	C1, C5, C8, C12, H3, L3, N8, P7, R4, R13, R15
VLN1	Bias setting for pixel source follower operating current. Adjustable external voltage from 0.5 to 1.5V is recommended. Impedance: 10kOhm, 10pF. Decoupling capacitors recommended.	G15

2.5 Pin Descriptions (continued)

Signal Name	Function	Pin Number(s)
VLN2	Bias setting voltage for ADC. Leave open circuit since this current is set on-chip. Impedance: 10kOhm, 10pF.	F15
VLOW_RST	Pixel reset reference voltage. Should be connected to AGND.	F1
VLP	Bias setting voltage for the column source follower operating current. Adjustable external voltage from 1.5 to 2.5 V is recommended. Impedance: 10kOhm, 10pF. Decoupling capacitors recommended.	G14
VREF1	ADC reference input voltage that sets the maximum input signal level (defines the level where the FF code occurs). This signal has two pin connections to minimize internal losses during high-speed operation. Adjustable external voltage from 0.5 to 1.25 V is recommended. User voltage source must supply a transient current of 100 mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND_SHIELD of ~0.1 µF to 1 µF is usually sufficient to filter out this required current transient.	E14, J15
VREF2	ADC reference used for the calibration operation. Adjustable external voltage from 0.5 to 1.0 V is recommended. User voltage source must supply a transient current of 20 mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND_SHIELD of ~0.1 µF to 1 µF is usually sufficient to filter out this required current transient.	H13
VREF3	Dark offset cancellation positive input reference, tied to the pedastal voltage to be added to the signal. Shound be connected to AGND.	G13
DGND_IO	Digital ground for pad ring.	A1, B9, B11, C6, D3, G2, J1, K3, L14, N6, N7, N9, P12, R1
—	No connect.	D13, K15, M3, N1, N2, N15, P1

NOTE: The analog voltages VCLAMP3, VLN1, VLN2, VLOW_RST, VLP, and VREF3 are generated on-chip and the user supplied voltages override the internal biases.

2.6 Board Connections



2.7 Electrical Specification

AC Electrical Characteristics (Vsupply = 3.3V ± 0.3V)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
Tplh	Data output propagation delay for low to high trans.			3		ns
Tphl	Data output propogation delay for high to low trans.			3		ns
Tsetup	Setup time for input to CLK	Vin = Vpwr or Vgnd		3		ns
Thold	Hold time for input to CLK	Vpwr=Min,VOH min		4		ns
PSRR_VDD	Power supply rejection ratio for digital supply	100 mV ripple at 9.7 kHz on supply		TBD		dB
PSRR_VDD_IO	Power supply rejection ratio for digital supply	100 mV ripple at 9.7 kHz on supply		TBD		dB
PSRR_VAA	Power supply rejection ratio for analog supply	100 mV ripple at 9.7 kHz on supply		TBD		dB

DC Electrical Characteristics (Vsupply = 3.3V ± 0.3V)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
VLP	Bias for Column Buffers			1.9		V
VREF1	Reference for ADC			1.0		V
VREF2	Reference for ADC Calibration			0.8		V
VREF3	Dark offset			0		V
VLN1	Bias for pixel source follower			1.0		V
VLN2	Bias for ADC			Open		
VLOW_RST	Reference for pixel reset			0		V
VCLAMP3	Dark offset			0.2		V
VIH	Input High Voltage		2.0		Vpwr+0.3	V
VIL	Input Low Voltage		-0.3		0.8	V
IIN	Input Leakage Current, No Pullup Resistor	Vin = Vpwr or Vgnd	-5		5	□A
VOH	Output High Voltage	Vpwr=Min, IOH=-100□A	Vpwr-0.2			V
VOL	Output Low Voltage	Vpwr=Min, IOL=100□A			0.2	V
Ipwr[1]	Maximum Quiescent Supply Current	66 MHz clock, 5pF load on outputs		140		mA

[1]Ipwr = I (VDD_IO) + I (VDD) + I (VAA)

2.7 Electrical Specification (continued)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vpwr	DC Supply Voltage	-0.5 to 5.5	V
Vin	DC Input Voltage	-0.5 to VDD + 0.5	V
Vout	DC Output Voltage	-0.5 to VDD + 0.5	V
I	DC Current Drain per Pin (Any I/O)	±50	mA
I	DC Current Drain, Vpwr and Vgnd	±100	mA

Maximum Ratings are those values beyond which damage to the device may occur. Vpwr=VDD=VAA=VDD_IO (VDD is supply to digital circuit, VAA to analog circuit). Vgnd=DGND=AGND=AGND_SHIELD (DGND is the ground to the digital circuit, AGND to the analog circuit). Chip can operate in mode when VDD_IO and logic levels are 3.3V, but VDD and VAA are 5V to increase dynamic range.

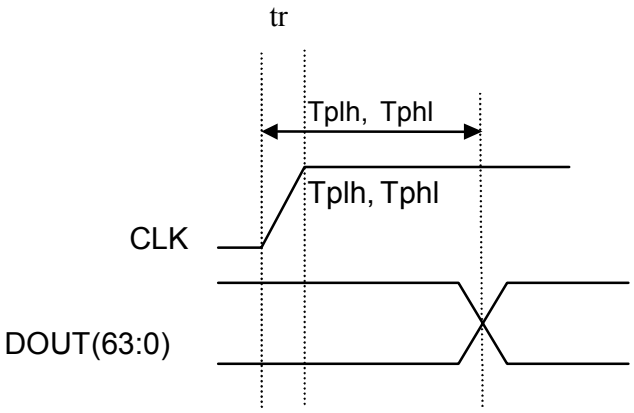
Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
Vpower	DC Supply Voltage	3.00	3.6	V
T_A	Commercial Operating Temperature	-5	60	C
T_J	Junction Temperature	0	85	C

This device contains circuitry to protect the inputs against damage from high static voltages or electric fields, but the user is advised to take precautions to avoid the application of any voltage higher than the maximum rated.

Power Dissipation (Vpwr = 3.3V; T_A = 25°C)

Symbol	Parameter	Typical	Unit
Pavg	Average Power	450	mW



Clock to Data Propagation Delay

3.0 Optical

3.1 Optical Specification

Image Sensor Characteristics (T_A = 25°C)

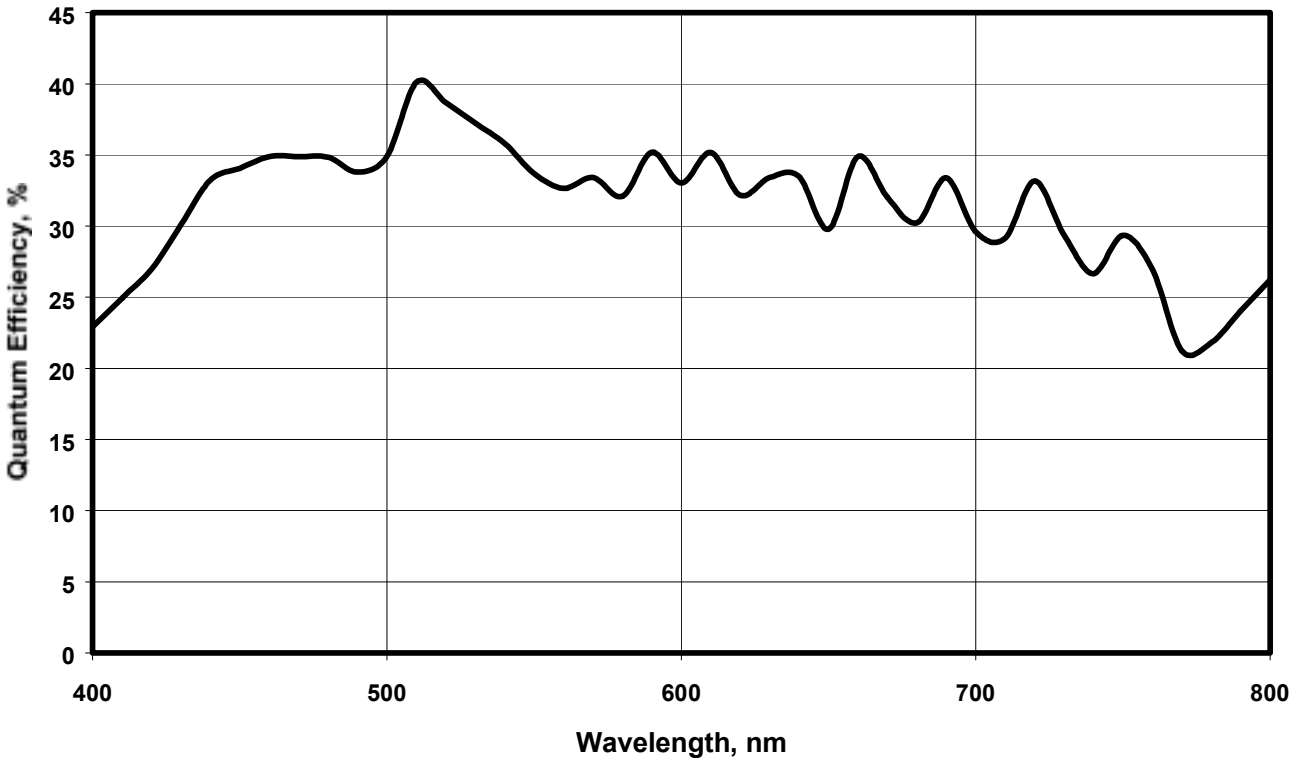
Symbol	Parameter	Min.	Typ.	Max.	Unit
R_I	Responsivity (ADC VREF=1V)		500		LSB/lux-sec.
SIG_NU[1]	Responsivity non-uniformity*		1		%
Nsat	Pixel saturation level		80,000		electrons
Idrk	Photodiode dark current		1		nA/cm^2
Vdrk	Output referred dark signal		60		mV/sec
NE	Input referred noise:				
	Overlapped conversion and digital readout (500 fps)		160		electrons
	Non-overlapped conversion and digital readout (60 fps)		50		electrons
Dyn_I	Internal dynamic range		64		dB
DRK_NU	Dark signal non-uniformity*		50		%
Kdrk	Dark current temperature coefficient		100		%/8°C

[1]Sensor non-uniformity measures at 30% saturation level.
*For additional details regarding the defect specifications please contact Photobit.

Pixel Array

Symbol	Parameter	Typical	Unit
Resolution	Number of pixels in active image	1024 x 1024	pixels
Pixel size	X-Y dimensions	10 x 10	µm
Pixel pitch	Center-to-center pixel spacing	10	µm
Pixel fill factor	Area of drawn active area	60	%

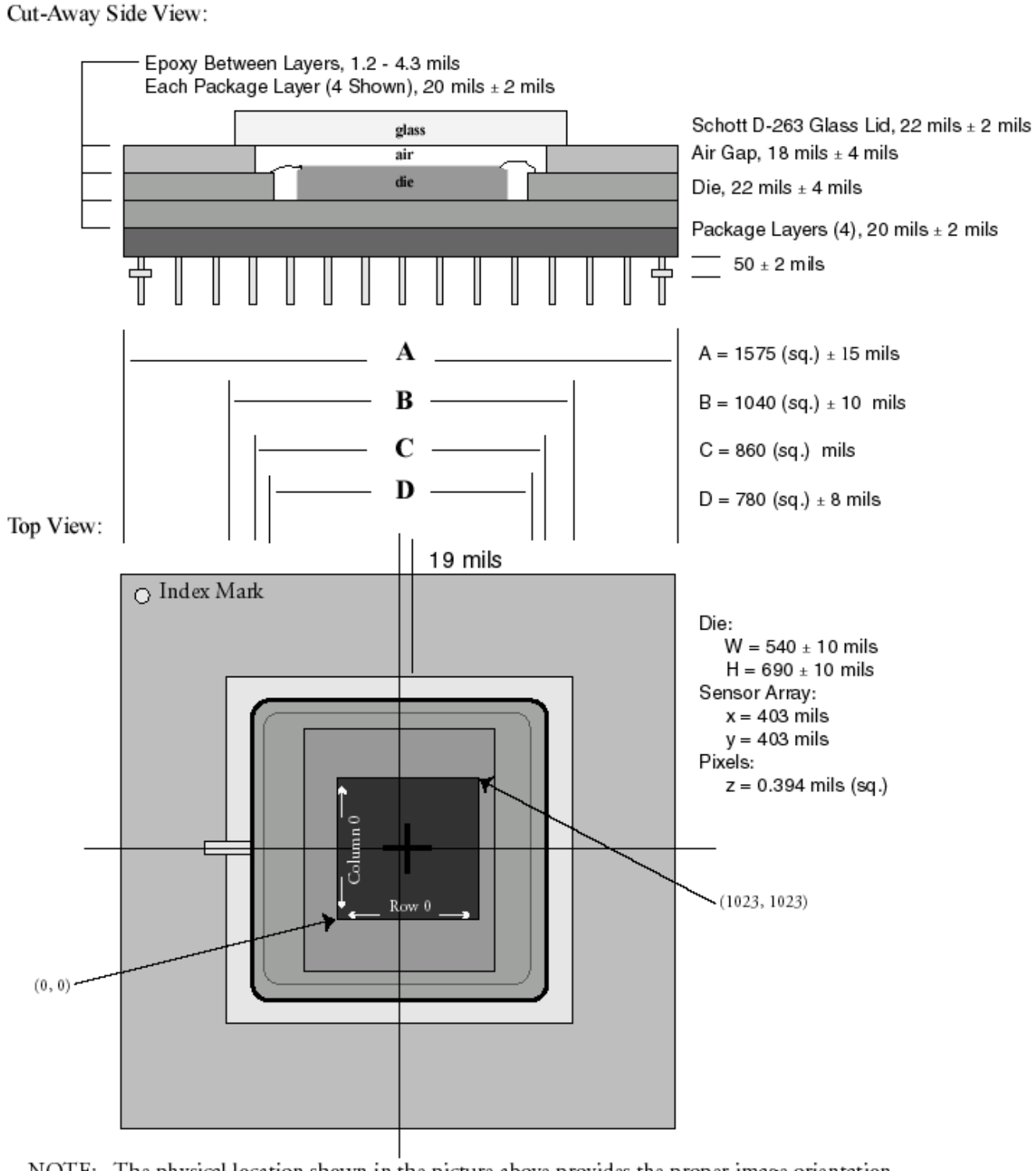
3.2 Quantum Efficiency



3.3 Pixel Array Offset Drawing

145-Pin Ceramic PGA (Pin Grid Array)

Sensor is centered on package, pixel array is off-center



NOTE: The physical location shown in the picture above provides the proper image orientation.

3.4 Lens Selection

Much of the specific information in this section is explained in detail in the Technology section on the Photobit website. The following information applies specifically to the Photobit PB-1024 megapixel image sensor.

Format

The PB-1024 megapixel image sensor is fabricated within the parameters of a 1-inch optical format. The diagonal of the image sensor array, 14.5 mm, fits most closely within the optical format corresponding to the 1-inch specification. Therefore, any imaging lens chosen should also satisfy this optical format criterion. For example, a lens with a 1-inch format will form an image that covers comfortably, but not excessively, an image sensor with a 1-inch format. Alternatively, a lens with less than a 1-inch format will form an image too small to adequately cover an image sensor with a 1-inch format, leaving the edges of the captured image cut off and under-utilizing the performance of the image sensor. Furthermore, a lens with greater than a 1-inch format will form an image that exceeds the area of an image sensor with a 1-inch format, thereby under-utilizing the performance of the lens.

Mounting

Several lens mounting standards exist that specify the threading of the lens' barrel as well as the distance the back flange of the lens should be from the image sensor for the lens to properly form an image. Typical lens mounting standards for the PB-1024 are:

Mount Name	Mounting Threads	Back-Flange-to-Image-Sensor
C	1 - 32	17.526 mm
CS	1 - 32	12.5 mm

Field of View and Focal Length

The field of view of an imaging system will depend on both the focal length of the imaging lens and the width of the image sensor. As most of the image information humans pay attention to generally falls within a 45-degree horizontal field of view, many camera systems attempt to imitate this field of view. However, in some cases a telephoto system (with a narrow field of view, say less than 20 degrees), or a wide angle system (with a wide field of view, say more than 60 degrees) may be desired. The approximate field of view that an imaging system can achieve is shown in the following equation:

$$\theta \approx 2\tan^{-1}\left(\frac{w}{2f}\right)$$

where θ is the field of view, $\tan^{-1}$ is the trigonometric function arc-tangent, w is the width of the image sensor, and f is the focal length of the imaging lens. For example, the imaging system's diagonal field of view can be determined by using the diagonal of the image sensor (14.5 mm) for w and a particular lens' focal length for f. Alternatively, the imaging system's horizontal field of view can be determined by using the horizontal of the image sensor (10.2 mm) for w and a particular lens' focal length for f. A lens with an approximately 12.4 mm focal length will provide a 45-degree horizontal field of view with a PB-1024 (keep in mind that the above equation is a simplified approximation).

F-Number

The f-number, or f/#, of an imaging lens is the ratio of the lens' focal length to its open aperture diameter. Every doubling in f-number reduces the light to the sensor by a factor of four. For example, a lens set at f/1.4 lets in four times more light than that same lens when it is set at f/2.8. Low f-number lenses capture a lot of light for delivery to the image sensor, but also require careful focus. Higher f-number lenses capture less light for delivery to the image sensor, and do not require as much effort to bring the imaging system to focus. Low f-number lenses generally cost more than high f-number lenses of similar overall performance. Typical f-numbers for various imaging systems are:

F-#	Imaging application
1.4	Low-light level imaging, manual focus systems
2.0	Typical for PC and other small form cameras
2.8	Common in digital still cameras
4.0+	Often used in machine vision applications

Typical f-numbers will range from 1.8 to 2.8. For example, most S-mount lenses come with a fixed f-number of f/2.0.

3.4 Lens Selection (continued)

MTF

Modulation Transfer Function (MTF) is a technical term that quantifies how well a particular system propagates information. For cameras, the "system" is the lens and the sensor, and the "information" is the picture they are capturing. MTF ranges from zero (no information gets through) to 100 (all information gets through), and is always specified in terms of information density. In most imaging systems, the MTF is limited by the performance of the imaging lens. A lens must be able to transfer enough information to the image sensor to be able to resolve details in the image that are as small as the pixels in the image sensor. The pixels are set on a 10-micron pitch (the center of one pixel is 10 microns from the center of its neighboring pixel). Thus, a lens used should be able to resolve image features as small as 10 microns. Typically, a lens' MTF is plotted as a function of the number of line pairs per millimeter the lens is attempting to resolve (more line pairs per millimeter mean higher information densities). For an electronic imaging system, one line pair will correspond to two image sensor pixels (each pixel can resolve one line). This is equated as:

$$LP/mm = \frac{1}{2z}$$

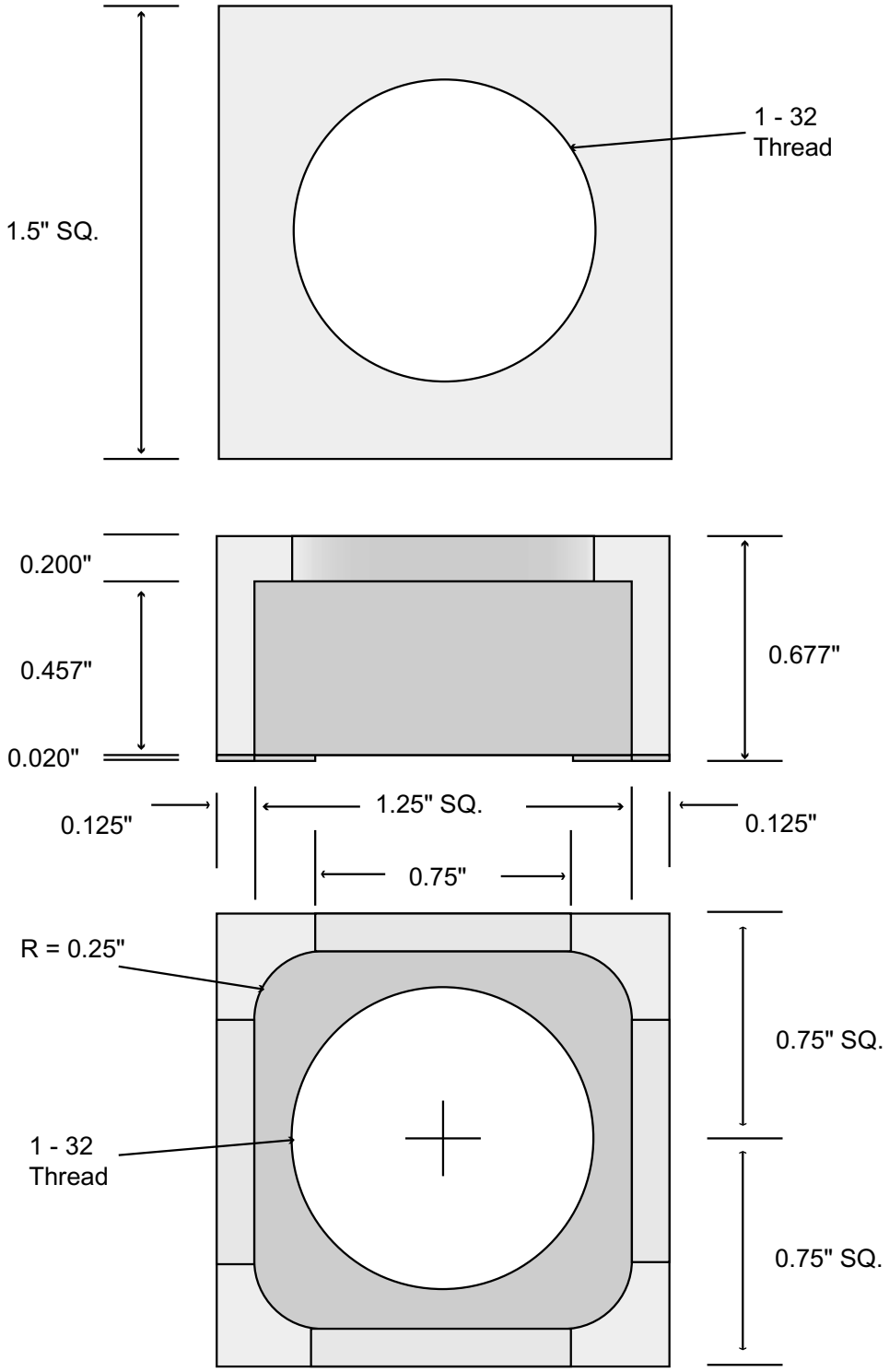
where LP/mm means line pairs per millimeter and z is the image sensor's pixel pitch, in millimeters. For the PB-1024, z = 0.010 mm, such that the PB-1024 has 50 LP/mm. Thus, a lens should provide an acceptable level of MTF all the way out to 50 LP/mm. For most lenses, the MTF will be highest in the center of the images they form, and gradually drop off toward the edges of the images they form. As well, MTFs at low values of LP/mm will generally be larger than MTFs at high values of LP/mm. One of the many trade-offs that must be decided by the end user is how high the MTF needs to be for a particular imaging situation. Generally, near an image sensor's LP/mm good MTFs are higher than 40, moderate MTFs are from 20 to 40, and poor MTFs are less than 20.

Infrared Cut-Off Filters

In most visible imaging situations it is necessary to include a filter in the imaging path that blocks infrared (IR) light from reaching the image sensor. This filter is called an IR cut-off filter. Various forms of IR cut-off filters are available, some absorptive (like Hoya's CM500 or Schott's BG18) and some reflective (i.e., dielectric stacks). Infrared light poses a problem to visible imaging because its presence blurs and decreases the MTF in the images formed by a lens. Since human vision only extends across a narrow range of the electromagnetic spectrum, camera systems hoping to capture images that look like the images our eyes capture must not capture light outside of our vision range. Silicon-based light detectors (like the ones in the PB-1024's pixels) detect light from the very deep blue to the near infrared. Thus, a filter must exist in the light's path that keeps the infrared from reaching the image sensor's pixels. In most cases, it is important that such a filter begin blocking light around 650 nm (in the deep red) and continue blocking it until at least 1100 nm (in the near IR). In most camera systems, the IR cut-off filter is included in the imaging lens.However, this point must be verified by a lens vendor when a particular lens is chosen for use with an image sensor.

3.4 Lens Selection (continued)

C-Mount Lens Shroud

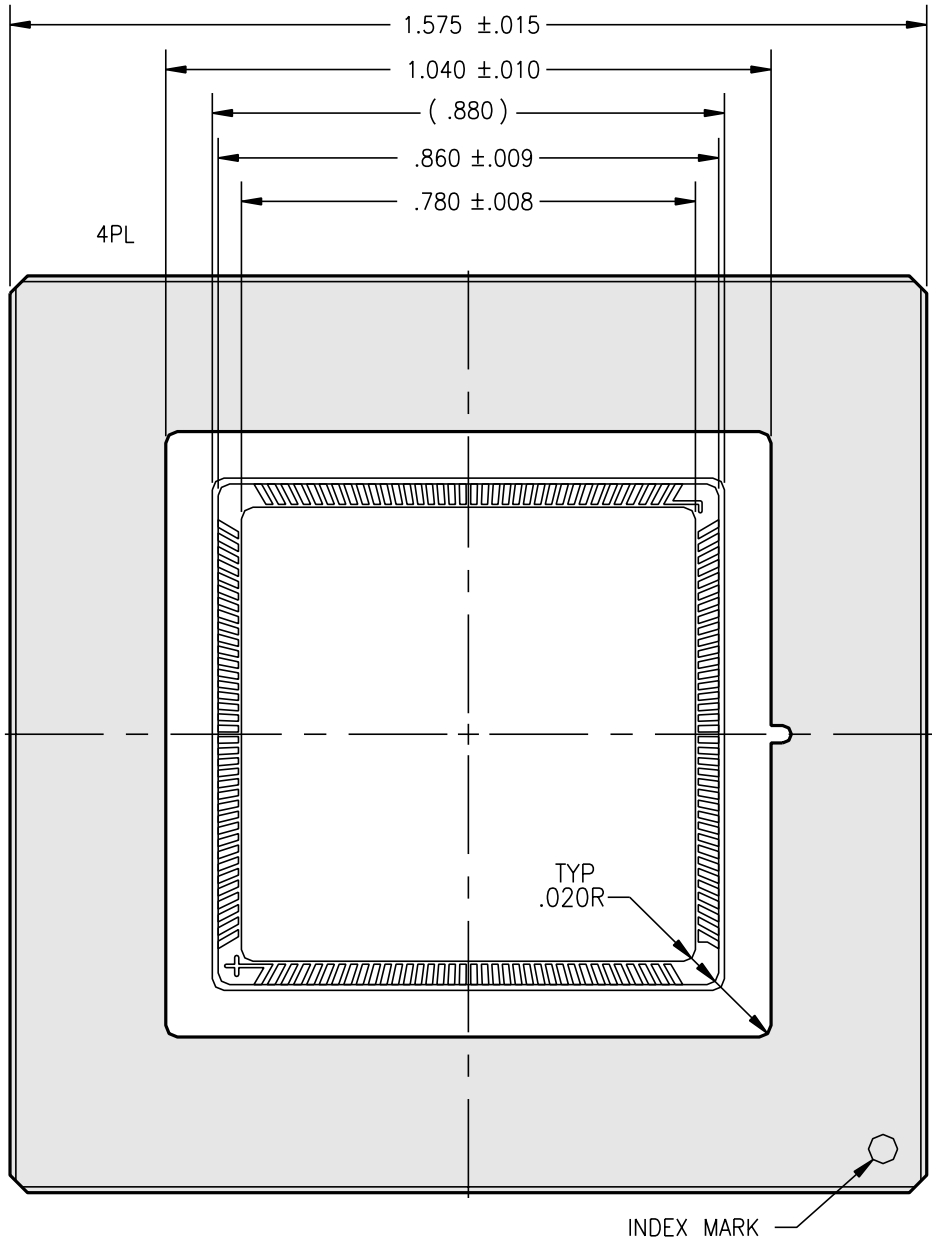


4.0 Mechanical

4.1 Package (145-Pin Ceramic PGA)

The PB-1024 CMOS image sensor has a window-filled package. During manufacture the die is placed into the 145-pin ceramic PGA (pin grid array), filled with a low-viscosity epoxy, covered with a window of appropriate thickness (for the focal length), and cured. This results in a physically robust module for board installation.

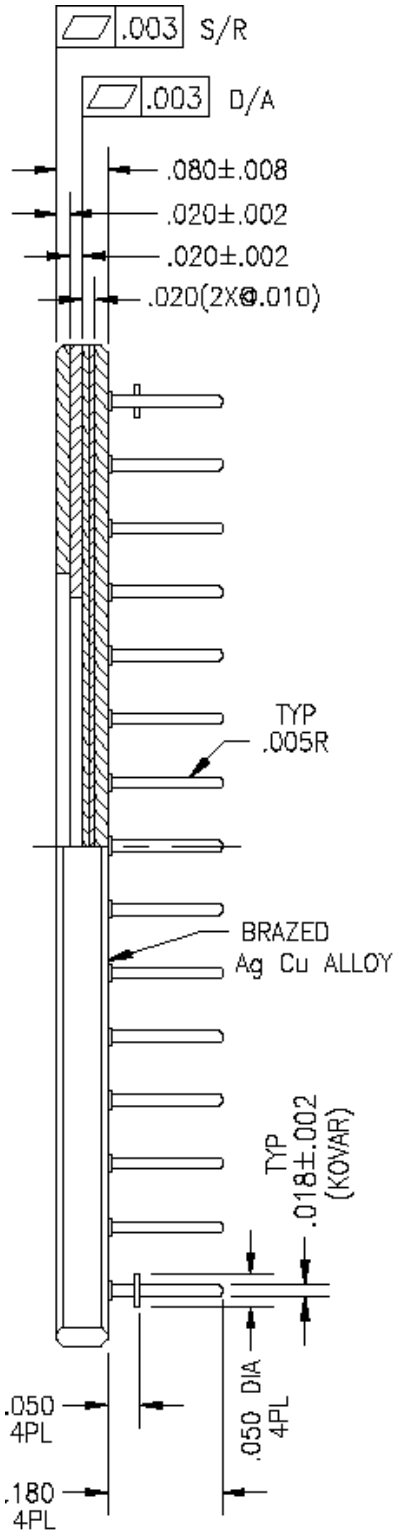
Top View



Metallization/plating: Tungsten + nickel 50~350µ “under gold 60~225µ” measurements in inches.

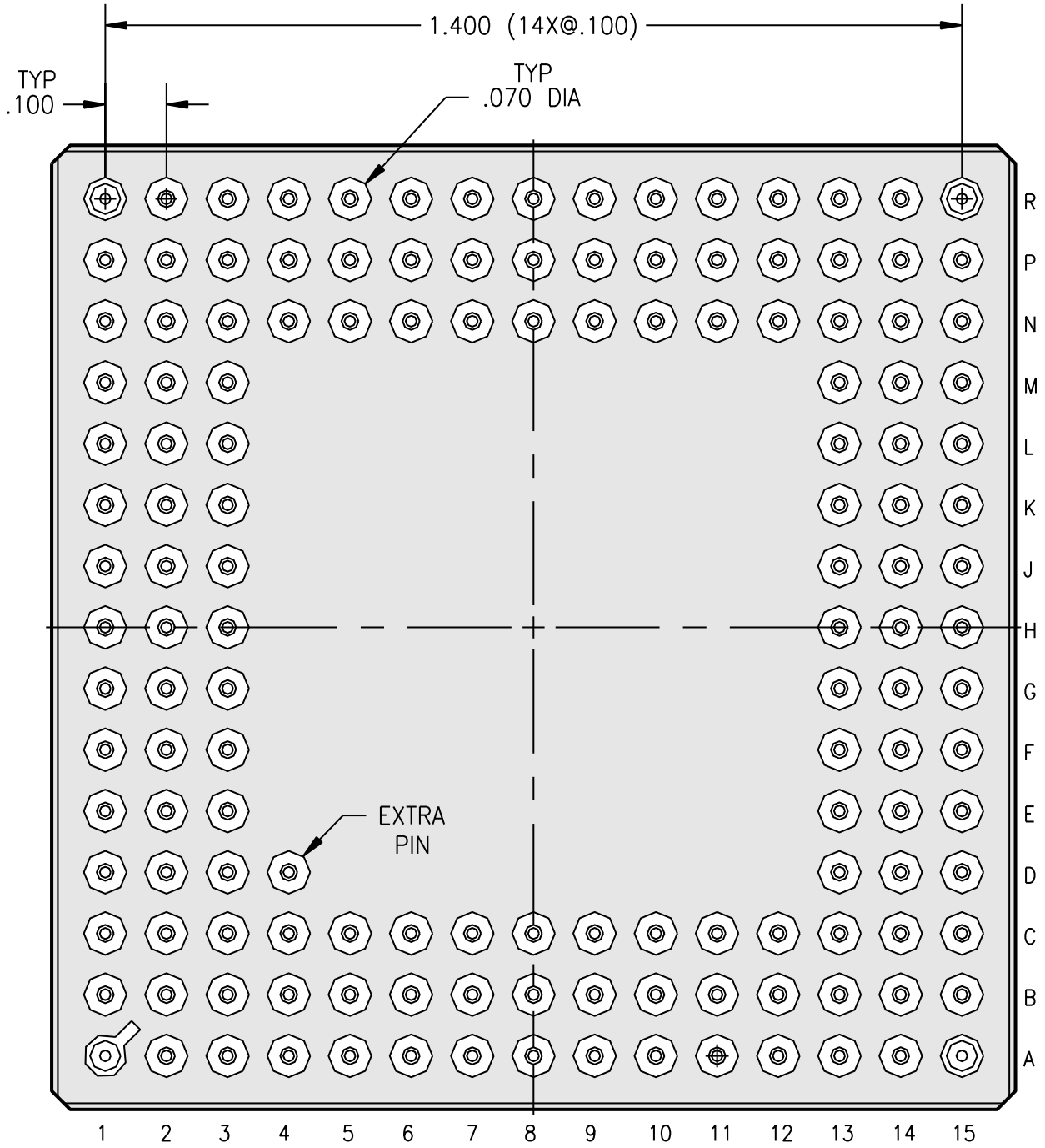
4.1 Package (continued)

Side View



4.1 Package (continued)

Bottom View



Seal ring and die attach to be floating from any pins.

5.0 Environmental

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Tstorage	Storage Temperature Range	-40 to 125	C
Tlead	Lead Temperature (10 second soldering)	235 Max.	C
Humidity	Maximum humidity exposure (@ 85C and 100 hours)	85% RH	%