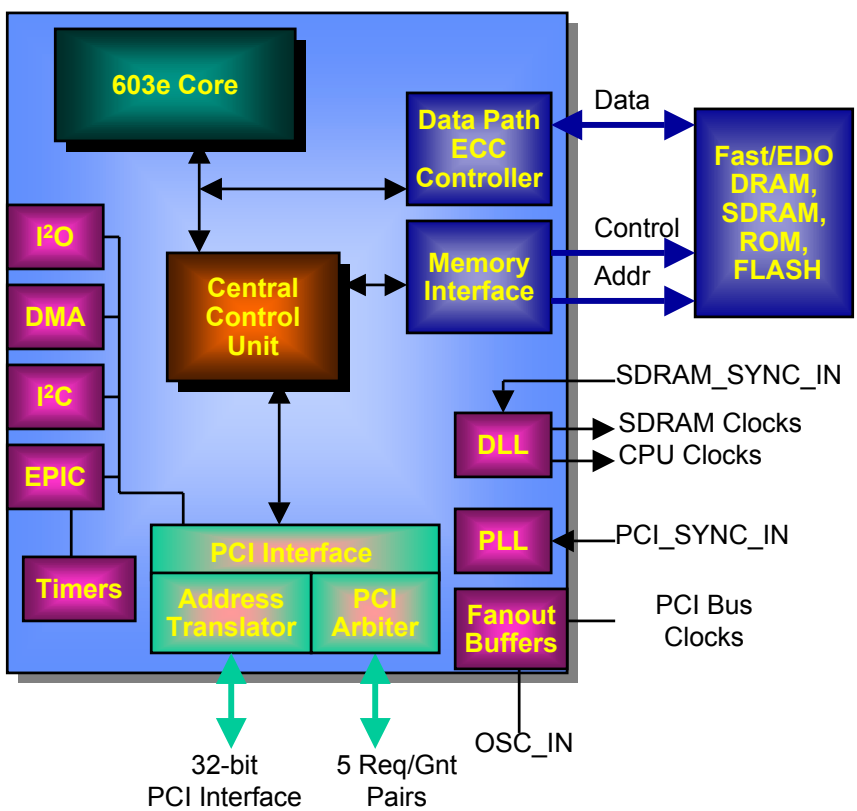
PC8240 Integrated PowerPC™ Processor Fact Sheet

The PC8240 Integrated PowerPC™ processor fits applications where cost, space, power consumption and performance are critical requirements. This device provides a high level of integration, reducing chip count from five discrete chips to one, thereby significantly reducing system component cost. High integration results is a simplified board design, less power consumption and faster time-to-market solution. This general purpose integrated processor targets systems using PCI interfaces in networking infrastructures, telecommunications, and other embedded markets. It can be used for control processing in applications such as routers, switches, network storage applications and image display systems.

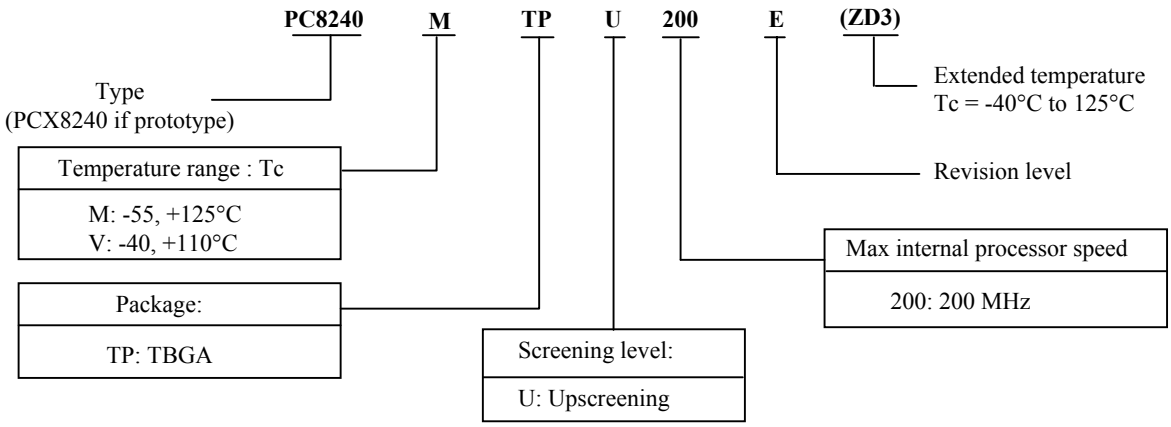
PC8240 Main Features

- 100-200 MHz PowerPC 603e™ core
- 32-bit PCI interface operating up to 66 MHz
- Memory controller offering SDRAM support up to 100 MHz operation
- General Purpose I/O and ROM interface support
- Two-channel DMA controller that supports chaining
- Messaging unit with I_2O messaging support capability
- Industry-standard I^2C interface
- Programmable Interrupts Controller (EPIC) with multiple timers and counters



PC8240 Technical Specifications

- **PowerPC 603e core**
  - High-performance, superscalar processor core
  - Floating-point unit (selectable), integer, load/store, system register and branch processing unit
  - 16KB instruction cache and 16KB data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - JTAG/COP for in-circuit hardware debugging
- **PCI Interface**
  - Compliant with PCI specification, revision 2.1
  - 32-bit PCI interface operates up to 66 MHz
  - PCI 5.0V tolerant
  - Support for accesses to all PCI address spaces
  - Store gathering of processor-to-PCI writes and PCI-to-memory writes
  - Selectable big or little endian operation
  - PCI interface can be configured as host or agent, allowing multiple PC107 chips on same PCI bus
  - Arbiter supports up to 5 other PCI devices
  - Parity support (selectable)
- **Memory Interface**
  - High bandwidth (32/64-bit) data bus up to 100 MHz
  - Programmable timing supporting either DRAM (FPM, EDO) or SDRAM
  - Support 1 to 8 banks - 4MB, 16MB, 64MB, and 128MB DRAMs or SDRAMs
  - 1GB of RAM space, 16MB of ROM space
  - 8-bit, 32-bit, or 64-bit ROM
  - PortX: 8-, 32-, or 64-bit general-purpose I/O port uses ROM controller interface with address strobe
  - Supports parity, read-modify-write, or error correcting code (ECC)
- **Other Embedded Features**
  - Two-Channel integrated DMA controller
  - I_2O Message Unit and I^2C controller
  - Embedded Programmable Interrupt Controller (EPIC)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI and memory bus drivers
- **Packaging**
  - 352 TBGA package
- **Screening**
  - TBGA upscreening based upon ATMEL-Grenoble standards
  - Full military temperature range (Tj = -55°C, + 125°C)
  - Industrial temperature range (Tj = -40°C, +110°C)



For additional information and product availability:
contact your local ATMEL-Grenoble representative
or visit our web site at http://www.atmel.com

You may also contact the PowerPC technical hotline at std.hotline@gfo.atmel.com

BP123 - 38521 Saint-Egrève Cedex - France - Tel: +33 (0)4 76 58 30 00 - Fax: +33 (0)4 76 58 34 80