# PT4820 Series

**35-W Triple Output Isolated DC/DC Converter for Logic Applications**

EXCALIBUR

**SLTS165A**

***(Revised 3/19/2002)***

## Features

- Triple Outputs (Independantly Regulated)
- Input Voltage Range: 36V to 75V
- 1500VDC Isolation
- Dual Logic On/Off Control
- Short Circuit Protection (All Outputs)
- Fixed Frequency Operation
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Space Saving Package: 1.3 sq. in. PCB Area (suffix N)
- Solderable Copper Case
- Safety Approvals Pending: UL60950 CSA 22.2 950 VDE EN60950

## Description

The PT4820 Excalibur™ power modules are a series of isolated triple-output DC/DC converters that operate from a standard (–48V) central office supply. Rated for up to 35W, these regulators are ideal for powering many mixed logic applications. The triple-output voltage combination allows for a compact multiple-output power supply in a single low-profile DC/DC module.

The available output voltage options include a low-voltage power bus for a DSP or ASIC core, and two additional standard logic supply voltages.

The PT4820 series incorporates many features to simplify system integration. These include a flexible On/Off enable control, an input under-voltage lock-out, and over-temperature protection. All outputs are short-circuit protected, and are internally sequenced to meet the power-up and power-down requirements of popular DSP ICs.

The PT4820 series is housed in a space-saving solderable case. The module requires no external heat sink and can occupy as little as 1.3 in² of PCB area.

## Ordering Information

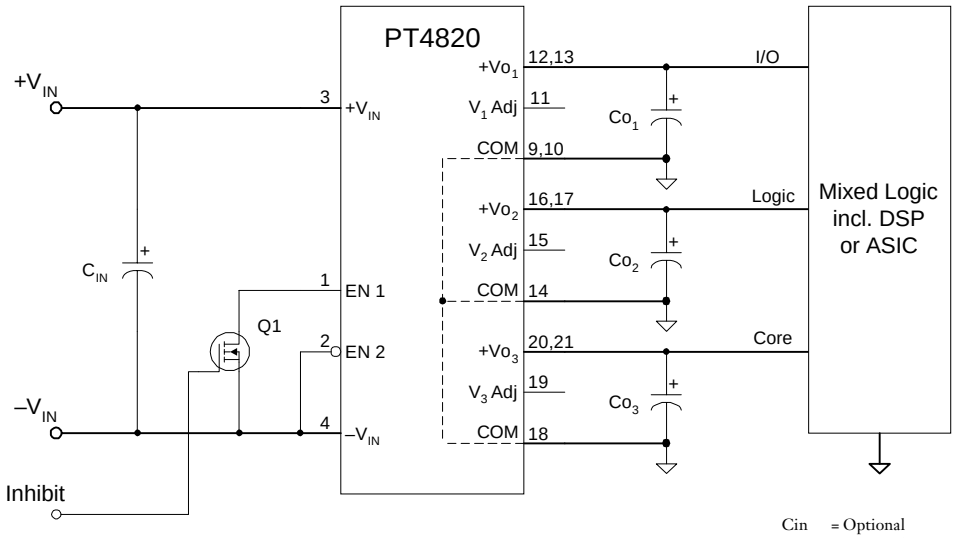
**PT4821❑** = +3.3/+2.5/+1.5V
**PT4822❑** = +3.3/+1.8/+1.5V
**PT4823❑** = +3.3/+2.5/+1.2V
**PT4824❑** = +3.3/+1.8/+1.2V
**PT4825❑** = +3.3/+1.5/+1.2V
**PT4826❑** = +5.0/+3.3/+1.8V
**PT4827❑** = +3.3/+2.5/+1.8V
**PT4828❑** = +5.0/+2.5/+1.5V
**PT4829❑** = +5.0/+1.8/+1.5V

## PT Series Suffix (PT1234x)

| Case/Pin Configuration | Order Suffix | Package Code |
|---|---|---|
| Vertical | **N** | (ENM) |
| Horizontal | **A** | (ENN) |
| SMD | **C** | (ENP) |

*(Reference the applicable package code drawing for the dimensions and PC layout)*

## Typical Application




Cin = Optional
Co1, Co2, Co3 = Optional; See specifications
EN1 & EN2 pins: See On/Off Enable Logic

## Environmental Specifications

| Characteristics | Symbols | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Maximum Operating Temperature Range | $T_a$ | Over $V_{in}$ Range | | –40 | — | +85 (i) | °C |
| Storage Temperature | $T_s$ | — | | –40 | — | +125 | °C |
| Mechanical Shock | | Per Mil-STD-883D, Method 2002.3<br>1 msec, ½ Sine, mounted | | — | TBD | — | G's |
| Mechanical Vibration | | Mil-STD-883D, Method 2007.2<br>20-2000 Hz | Suffix N<br>Suffix A, C | —<br>— | TBD (ii)<br>TBD (ii) | —<br>— | G's |
| Weight | — | Vertical/Horizontal | | — | 50 | — | grams |
| Shutdown Temperature | OTP | | | | 115 | 125 | °C |
| Flammability | — | Meets UL 94V-O | | | | | |

**Notes:** *(i) See SOA curves or consult factory for appropriate derating.*
*(ii) Only the case pins on through-hole pin configurations (N & A) must be soldered. For more information see the applicable package outline drawing.*

## Pin Configuration

| Pin | Function |
|---|---|
| 1 | EN 1 |
| 2 | EN 2 |
| 3 | +Vin |
| 4 | –Vin |
| 5 | Do Not Connect |
| 6 | Pin Not Present |
| 7 | Pin Not Present |
| 8 | Pin Not Present |
| 9 | COM |
| 10 | COM |
| 11 | $Vo_1$ Adjust |

| Pin | Function |
|---|---|
| 12 | $Vo_1$ |
| 13 | $Vo_1$ |
| 14 | COM |
| 15 | $Vo_2$ adjust |
| 16 | $+Vo_2$ |
| 17 | $+Vo_2$ |
| 18 | COM |
| 19 | $Vo_3$ adjust |
| 20 | $+Vo_3$ |
| 21 | $+Vo_3$ |

*Note: Shaded functions indicate those pins that are at primary-side potential.*

## On/Off Enable Logic

| Pin 1 | Pin 2 | Output Status |
|---|---|---|
| × | 1 | Off |
| 1 | 0 | On |
| 0 | × | Off |

**Notes:**
*Logic 1 =Open collector*
*Logic 0 = –Vin (pin 2) potential*

*For positive Enable function, connect pin 2 to pin 4 and use pin 1.*

*For negative Enable function, leave pin 1 open and use pin 2.*

## Pin Descriptions

**+Vin:** The positive input supply for the module with respect to –Vin. When powering the module from a –48V telecom central office supply, this input is connected to the primary system ground.

**–Vin:** The negative input supply for the module, and the 0VDC reference for the EN 1, and EN 2 inputs. When powering the module from a +48V supply, this input is connected to the 48V(Return).

**EN 1:** The positive logic input that activates the module output. If not used, this pin should be left open circuit. Connecting this input to –Vin disables the module's outputs.

**EN 2:** The negative logic input that activates the module output. This pin must be connected to –Vin to enable the module's outputs. A high impedance disables the module's outputs.

**Vo 1:** The highest regulated output voltage, which is referenced to the COM node.

**Vo 2:** The regulated output that is designed to power logic circuitry. It is referenced to the COM node.

**Vo 3:** The low-voltage regulated output that provides power for a µ-processor or DSP core, and is referenced to the COM node.

**COM:** The secondary return reference for the module's three regulated output voltages. It is DC isolated from the input supply pins.

**$Vo_1$ Adjust:** Using a single resistor, this pin allows $Vo_1$ to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

**$Vo_2$ Adjust:** Using a single resistor, this pin allows $Vo_2$ to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

**$Vo_3$ Adjust:** Using a single resistor, this pin allows $Vo_3$ to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

## PT4821 Electrical Specifications

(Unless otherwise stated, the operating conditions are:- $T_a$ =25°C, $V_{in}$ =48V, and $I_o$ =0.5$I_o$max)

| Characteristics | Symbols | Conditions | | PT4821 Min | PT4821 Typ | PT4821 Max | Units |
|---|---|---|---|---|---|---|---|
| Output Power | $P_o$ | Total (all three outputs) | | — | — | 35 (1) | W |
| Output Current | $I_o$ | Each output | $Io_1$ (3.3V) | 0 | — | 8 (2) | A |
| | | | $Io_2$ (2.5V) | 0 | — | 6 (2) | |
| | | | $Io_3$ (1.5V) | 0 | — | 6 (2) | |
| | | Total ($Io_1$ + $Io_2$ + $Io_3$) | | — | — | 12 (2) | A |
| Input Voltage Range | $V_{in}$ | Continuous | | 36 | — | 75 | V |
| | | Surge (1 minute) | | — | — | 80 | |
| Set-Point Voltage | $V_o$ | | $Vo_1$ | 3.24 | 3.3 | 3.36 | V |
| | | | $Vo_2$ | 2.45 | 2.5 | 2.55 | |
| | | | $Vo_3$ | 1.47 | 1.5 | 1.53 | |
| Temperature Variation | $Reg_{temp}$ | –40°C ≤$T_a$ ≤+85°C, $I_o$ =$I_o$min | $Vo_1$ | — | ±0.5 | — | %$V_o$ |
| | | | $Vo_2$/$Vo_3$ | — | ±0.5 | — | |
| Line Regulation | $Reg_{line}$ | All outputs, Over $V_{in}$ range | | — | ±0.1 | ±0.5 | %$V_o$ |
| Load Regulation | $Reg_{load}$ | All outputs, 0≤$I_o$≤$I_o$max | | — | ±0.1 | ±0.5 | %$V_o$ |
| Total Output Voltage Variation | $\Delta V_o$ tol | Includes set-point, line, load, | $Vo_1$ | — | — | ±3 (3) | %$V_o$ |
| | | –40°C≤$T_a$ ≤+85°C | $Vo_2$/$Vo_3$ | — | — | ±3 (3) | |
| Efficiency | η | $Io_1$ =6A, $Io_2$ =2A, $Io_3$ =2A | | — | 87 | — | % |
| $V_o$ Ripple/Noise (0 to 20MHz bandwidth) | $V_n$ | | $Vo_1$ | — | 50 | — | $mV_{pp}$ |
| | | | $Vo_2$ | — | 50 | — | |
| | | | $Vo_3$ | — | 25 | — | |
| Transient Response | $t_{tr}$ | 0.1A/µs load step, 50% to 75% $I_o$max | | — | 200 | — | µSec |
| | $V_{os}$ | $V_o$ over/undershoot | | — | 3 | — | %$V_o$ |
| Output Adjust Range | $V_o$adj | | $Vo_1$/$Vo_2$/$Vo_3$ | — | ±10 | — | %$V_o$ |
| Current Limit Threshold | $I_{LIM}$ | Total, all outputs | | — | 14 | — | A |
| Switching Frequency | $f_s$ | Over $V_{in}$ and $I_o$ ranges | | 350 | 400 | 450 | kHz |
| Under Voltage Lockout | $V_{on}$ | $V_{in}$ increasing | | — | 35.5 | — | V |
| | $V_{off}$ | $V_{in}$ decreasing | | — | 34 | — | |
| Enable Control (pins 1 & 2) | | Referenced to –$V_{in}$ (pin 4) | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | | 4 | — | 15 (4) | V |
| Low-Level Input Voltage | $V_{IL}$ | | | –0.2 | — | 0.8 (4) | |
| Low-Level Input Current | $I_{IL}$ | | | — | 1 | 2 | mA |
| Standby Input Current | $I_{in}$ standby | pins 1 & 2 open circuit | | — | 1 | 5 (3) | mA |
| Internal Input Capacitance | $C_{int}$ | | | — | 1.14 | — | µF |
| External Output Capacitance | $Co_1$ | | | 0 | — | 1,000 (5) | µF |
| | $Co_2$ | | | 0 | — | 1,000 (5) | |
| | $Co_3$ | | | 0 | — | 1,000 (5) | |
| Primary/Secondary Isolation | $V_{iso}$ | | | 1500 | — | — | V |
| | $C_{iso}$ | | | — | 2,200 | — | pF |
| | $R_{iso}$ | | | 10 | — | — | MΩ |

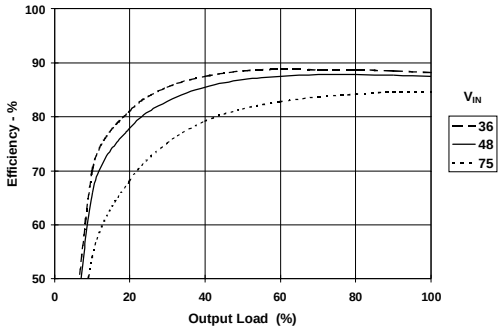
***Notes:*** *(1) The sum total power delivered from all three regulated outputs, $Vo_1$, $Vo_2$, and $Vo_3$, cannot exceed 35 watts.*
*(2) The sum-total current from outputs $Vo_1$, $Vo_2$, and $Vo_3$ cannot exceed 10ADC.*
*(3) Limits are guranteed by design.*
*(4) The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –$V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
*(5) Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

# Typical Characteristics

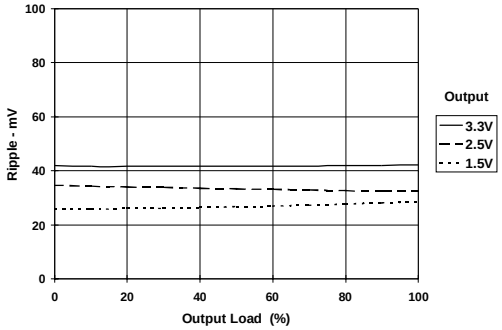
## PT4821 Performance Characteristics (See Note A)

***($Io_1$ =6A, $Io_2$ =2A, $Io_3$ =2A represents 100% Load)***

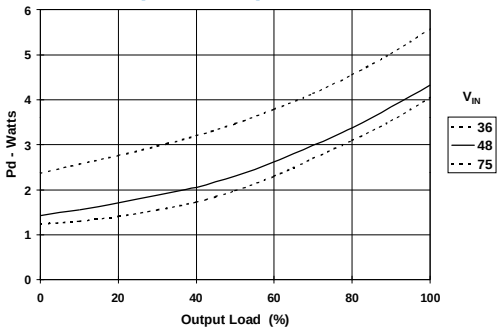
### Efficiency vs Output Power




### Output Ripple vs Output Power



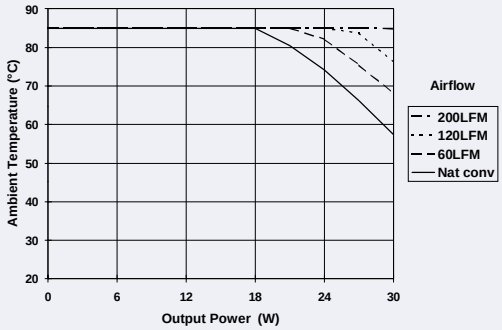

### Power Dissipation vs Output Power




## PT4821 Safe Operating Areas (See Note B)

***($Io_1$ =6A, $Io_2$ =2A, $Io_3$ =2A represents 100% Load)***

### SOA vs Output Load @$V_{in}$ =48V




**Note A:** *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
**Note B:** *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

## PT4826 Electrical Specifications

(Unless otherwise stated, the operating conditions are:- $T_a$ =25°C, $V_{in}$ =48V, and $I_o$ =0.5$I_o$max)

| Characteristics | Symbols | Conditions | | PT4826 Min | PT4826 Typ | PT4826 Max | Units |
|---|---|---|---|---|---|---|---|
| Output Power | $P_o$ | Total (all three outputs) | | — | — | 35 (1) | W |
| Output Current | $I_o$ | Each output | $Io_1$ (5.0V)<br>$Io_2$ (3.3V)<br>$Io_3$ (1.8V) | 0<br>0<br>0 | —<br>—<br>— | 5.0 (2)<br>5.5 (2)<br>5.5 (2) | A |
| | | Total ($Io_1$ + $Io_2$ + $Io_3$) | | — | — | 9 (2) | A |
| Input Voltage Range | $V_{in}$ | Continuous<br>Surge (1 minute) | | 36<br>— | —<br>— | 75<br>80 | V |
| Set-Point Voltage | $V_o$ | | $Vo_1$<br>$Vo_2$<br>$Vo_3$ | 4.9<br>3.24<br>1.76 | 5.0<br>3.3<br>1.8 | 5.1<br>3.36<br>1.84 | V |
| Temperature Variation | $Reg_{temp}$ | –40°C ≤$T_a$ ≤+85°C, $I_o$ =$I_o$min | $Vo_1$<br>$Vo_2$/$Vo_3$ | —<br>— | ±0.5<br>±0.5 | —<br>— | %$V_o$ |
| Line Regulation | $Reg_{line}$ | All outputs, Over $V_{in}$ range | | — | ±0.1 | ±0.5 | %$V_o$ |
| Load Regulation | $Reg_{load}$ | All outputs, 0≤$I_o$≤$I_o$max | | — | ±0.1 | ±0.5 | %$V_o$ |
| Total Output Voltage Variation | $\Delta V_o$ tol | Includes set-point, line, load,<br>–40°C≤$T_a$ ≤+85°C | $Vo_1$<br>$Vo_2$/$Vo_3$ | —<br>— | —<br>— | ±3 (3)<br>±3 (3) | %$V_o$ |
| Efficiency | η | $Io_1$ =5A, $Io_2$ =2A, $Io_3$ =2A | | — | 87 | — | % |
| $V_o$ Ripple/Noise<br>(0 to 20MHz bandwidth) | $V_n$ | | $Vo_1$<br>$Vo_2$<br>$Vo_3$ | —<br>—<br>— | 50<br>50<br>25 | —<br>—<br>— | $mV_{pp}$ |
| Transient Response<br>Overshoot | $t_{tr}$<br>$V_{os}$ | 0.1A/µs load step, 50% to 75% $I_o$max<br>$V_o$ over/undershoot | | —<br>— | 200<br>5 | —<br>— | µSec<br>%$V_o$ |
| Output Adjust Range | $V_o$adj | | $Vo_1$/$Vo_2$/$Vo_3$ | — | ±10 | — | %$V_o$ |
| Current Limit Threshold | $I_{LIM}$ | Total, all outputs | | — | 11 | — | A |
| Switching Frequency | $f_s$ | Over $V_{in}$ and $I_o$ ranges | | 350 | 400 | 450 | kHz |
| Under Voltage Lockout | $V_{on}$<br>$V_{off}$ | $V_{in}$ increasing<br>$V_{in}$ decreasing | | —<br>— | 35.5<br>34 | —<br>— | V |
| Enable Control (pins 1 & 2)<br>High-Level Input Voltage<br>Low-Level Input Voltage | <br>$V_{IH}$<br>$V_{IL}$ | Referenced to –$V_{in}$ (pin 4) | | <br>4<br>–0.2 | <br>—<br>— | <br>15 (4)<br>0.8 (4) | V |
| Low-Level Input Current | $I_{IL}$ | | | — | 1 | 2 | mA |
| Standby Input Current | $I_{in}$ standby | pins 1 & 2 open circuit | | — | 1 | 5 (3) | mA |
| Internal Input Capacitance | $C_{int}$ | | | — | 1.14 | — | µF |
| External Output Capacitance | $Co_1$<br>$Co_2$<br>$Co_3$ | | | 0<br>0<br>0 | —<br>—<br>— | 1,000 (5)<br>1,000 (5)<br>1,000 (5) | µF |
| Primary/Secondary Isolation | $V_{iso}$<br>$C_{iso}$<br>$R_{iso}$ | | | 1500<br>—<br>10 | —<br>2,200<br>— | —<br>—<br>— | V<br>pF<br>MΩ |

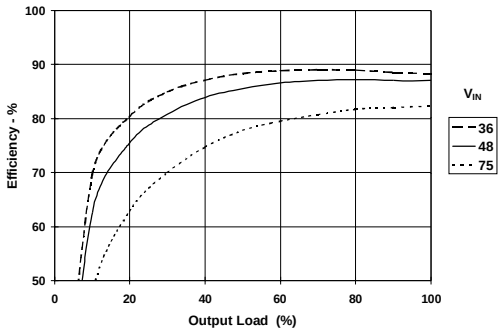
***Notes:*** *(1) The sum total power delivered from all three regulated outputs, $Vo_1$, $Vo_2$, and $Vo_3$, cannot exceed 35 watts.*
*(2) The sum-total current from outputs $Vo_1$, $Vo_2$, and $Vo_3$ cannot exceed 9ADC.*
*(3) Limits are guranteed by design.*
*(4) The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –$V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
*(5) Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

# Typical Characteristics

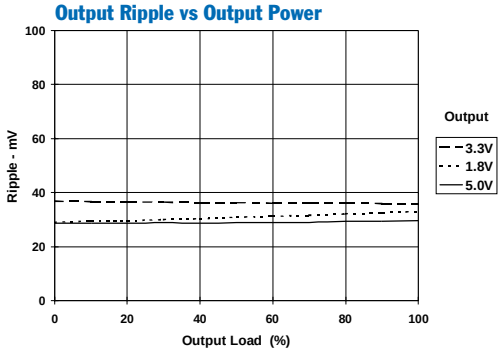
## PT4826 Performance Characteristics (See Note A)

***($Io_1$ =5A, $Io_2$ =2A, $Io_3$ =2A represents 100% Load)***

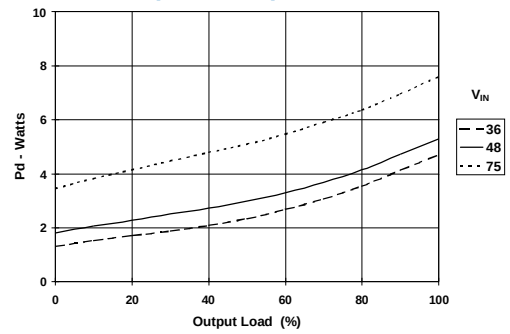
### Efficiency vs Output Power




### Output Ripple vs Output Power




### Power Dissipation vs Output Power




## PT4826 Safe Operating Areas (See Note B)

***($Io_1$ =5A, $Io_2$ =2A, $Io_3$ =2A represents 100% Load)***

### SOA vs Output Load @$V_{in}$ =48V

**Note A:** *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
**Note B:** *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

## PT4828 Electrical Specifications

(Unless otherwise stated, the operating conditions are:- $T_a$ =25°C, $V_{in}$ =48V, and $I_o$ =0.5$I_o$max)

| Characteristics | Symbols | Conditions | | PT4828 Min | PT4828 Typ | PT4828 Max | Units |
|---|---|---|---|---|---|---|---|
| Output Power | $P_o$ | Total (all three outputs) | | — | — | 35 (1) | W |
| Output Current | $I_o$ | Each output | $Io_1$ (5.0V)<br>$Io_2$ (2.5V)<br>$Io_3$ (1.5V) | 0<br>0<br>0 | —<br>—<br>— | 5.0 (2)<br>5.5 (2)<br>5.5 (2) | A |
| | | Total ($Io_1$ + $Io_2$ + $Io_3$) | | — | — | 9 (2) | A |
| Input Voltage Range | $V_{in}$ | Continuous<br>Surge (1 minute) | | 36<br>— | —<br>— | 75<br>80 | V |
| Set-Point Voltage | $V_o$ | | $Vo_1$<br>$Vo_2$<br>$Vo_3$ | 4.9<br>2.45<br>1.47 | 5.0<br>2.5<br>1.5 | 5.1<br>2.55<br>1.53 | V |
| Temperature Variation | $Reg_{temp}$ | –40°C ≤$T_a$ ≤+85°C, $I_o$ =$I_o$min | $Vo_1$<br>$Vo_2$/$Vo_3$ | —<br>— | ±0.5<br>±0.5 | —<br>— | %$V_o$ |
| Line Regulation | $Reg_{line}$ | All outputs, Over $V_{in}$ range | | — | ±0.1 | ±0.5 | %$V_o$ |
| Load Regulation | $Reg_{load}$ | All outputs, 0≤$I_o$≤$I_o$max | | — | ±0.1 | ±0.5 | %$V_o$ |
| Total Output Voltage Variation | $\Delta V_o$ tol | Includes set-point, line, load,<br>–40°C≤$T_a$ ≤+85°C | $Vo_1$<br>$Vo_2$/$Vo_3$ | —<br>— | —<br>— | ±3 (3)<br>±3 (3) | %$V_o$ |
| Efficiency | η | $Io_1$ =5A, $Io_2$ =2A, $Io_3$ =2A | | — | 86.5 | — | % |
| $V_o$ Ripple/Noise<br>(0 to 20MHz bandwidth) | $V_n$ | | $Vo_1$<br>$Vo_2$<br>$Vo_3$ | —<br>—<br>— | 50<br>50<br>25 | —<br>—<br>— | $mV_{pp}$ |
| Transient Response<br>Output Voltage Deviation | $t_{tr}$<br>$V_{os}$ | 0.1A/µs load step, 50% to 75% $I_o$max<br>$V_o$ over/undershoot | | —<br>— | 200<br>5 | —<br>— | µSec<br>%$V_o$ |
| Output Adjust Range | $V_o$adj | | $Vo_1$/$Vo_2$/$Vo_3$ | — | ±10 | — | %$V_o$ |
| Current Limit Threshold | $I_{LIM}$ | Total, all outputs | | — | 11 | — | A |
| Switching Frequency | $f_s$ | Over $V_{in}$ and $I_o$ ranges | | 350 | 400 | 450 | kHz |
| Under Voltage Lockout | $V_{on}$<br>$V_{off}$ | $V_{in}$ increasing<br>$V_{in}$ decreasing | | —<br>— | 35.5<br>34 | —<br>— | V |
| Enable Control (pins 1 & 2)<br>High-Level Input Voltage<br>Low-Level Input Voltage | <br>$V_{IH}$<br>$V_{IL}$ | Referenced to –$V_{in}$ (pin 4) | | <br>4<br>–0.2 | <br>—<br>— | <br>15 (4)<br>0.8 (4) | V |
| Low-Level Input Current | $I_{IL}$ | | | — | 1 | 2 | mA |
| Standby Input Current | $I_{in}$ standby | pins 1 & 2 open circuit | | — | 1 | 5 (3) | mA |
| Internal Input Capacitance | $C_{int}$ | | | — | 1.14 | — | µF |
| External Output Capacitance | $Co_1$<br>$Co_2$<br>$Co_3$ | | | 0<br>0<br>0 | —<br>—<br>— | 1,000 (5)<br>1,000 (5)<br>1,000 (5) | µF |
| Primary/Secondary Isolation | $V_{iso}$<br>$C_{iso}$<br>$R_{iso}$ | | | 1500<br>—<br>10 | —<br>2,200<br>— | —<br>—<br>— | V<br>pF<br>MΩ |

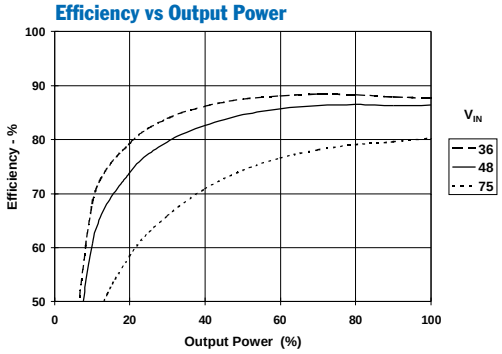
***Notes:*** *(1) The sum total power delivered from all three regulated outputs, $Vo_1$, $Vo_2$, and $Vo_3$, cannot exceed 35 watts.*
*(2) The sum-total current from outputs $Vo_2$, and $Vo_3$ cannot exceed 9ADC.*
*(3) Limits are guranteed by design.*
*(4) The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –$V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
*(5) Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

# Typical Characteristics

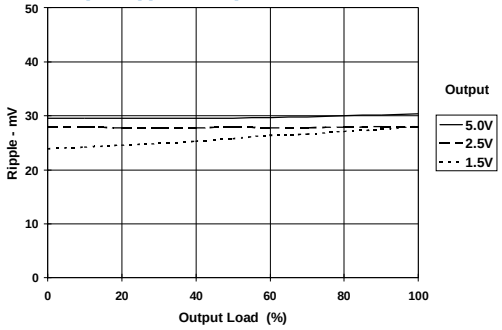
## PT4828 Performance Characteristics (See Note A)

***($Io_1$ =5A, $Io_2$ =2A, $Io_3$ =2A represents 100% Load)***

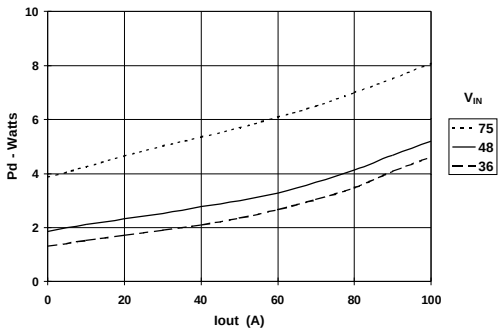
### Efficiency vs Output Power




### Output Ripple vs Output Power




### Power Dissipation vs Output Power




## PT4828 Safe Operating Areas (See Note B)

***($Io_1$ =5A, $Io_2$ =2A, $Io_3$ =2A represents 100% Load)***

### SOA vs Output Load @$V_{in}$ =48V

**Note A:** *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
**Note B:** *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

## Operating Features of the PT4820 Triple-Output DC/DC Converters

### Short-Circuit Protection

To protect against load faults all three outputs from the PT4820 series of triple-output DC/DC converters incorporate output short-circuit protection. When the combined output current from all three outputs exceeds the current limit threshold (see data sheet specifications), the PT4820 shuts down after a short period of typically 15ms. This forces the output voltage at all three regulated outputs to simultaneously fall to zero. Following shutdown, the module periodically attempts to recover by executing a soft start power-up. This occurs at intervals of approximately 65ms. If the load fault persists, the module will continually cycle through successive over-current trips, shutdowns, and restarts.

### Over-Temperature Protection

The PT4820 DC/DC converter series have an internal temperature sensor, which monitors the temperature of the module's metal case. If the case temperature exceeds a nominal 115°C the converter will shut down. The converter will automatically restart when the sensed temperature returns to about 100°C.

### Under-Voltage Lock-Out

The Under-Voltage Lock-Out (UVLO) circuit prevents operation of the converter whenever the input voltage to the module is insufficient to maintain output regulation. The UVLO has approximately 2V of hysterisis. This is to prevent oscillation with a slowly changing input voltage. Below the UVLO threshold the module is off and the enable control inputs, EN1 and EN2 are inoperative.

### Primary-Secondary Isolation

The PT4820 series of DC/DC converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500VDC. The isolation complies with UL60950 and EN60950, and the requirements for operational isolation. This allows the converter to be configured for either a positive or negative input voltage source.

The regulation control circuitry for these modules is located on the secondary (output) side of the isolation barrier. Control signals are passed between the primary and secondary sides of the converter. The data sheet 'Pin Descriptions' and 'Pin-Out Information' provides guidance as to which reference (primary or secondary) that must be used for each of the external control signals.

### Fuse Recommendations

If desired an input fuse may be added to protect against the application of a reverse input voltage.

## Using the On/Off Enable Controls on the PT4820 Series of Triple Output DC/DC Converters

The PT4820 (48V input) series of triple-output DC/DC converters incorporate two output enable controls. EN1 (pin 2) is the *Negative Enable* input, and EN2 (pin 1) is the *Positive Enable* input. Both inputs are electrically referenced to $-V_{in}$ (pin 4) on the primary or input side of the converter. The *Enable* pins are ideally controlled with an open-collector (or open-drain) discrete transistor. A pull-up resistor is not required. If added, the pull-up voltage must be limited to 15V.

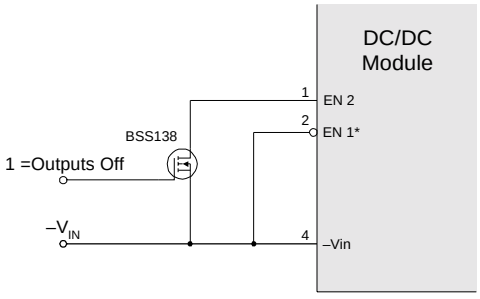
### Automatic (UVLO) Power-Up

Connecting EN1 (pin 2) to $-V_{in}$ (pin 4) and leaving EN2 (pin 1) open-circuit configures the converter for automatic power up. (See data sheet "Typical Application"). The converter control circuitry incorporates an "Under Voltage Lockout" (UVLO) function, which disables the converter until the minimum specified input voltage is present at $\pm V_{in}$. (See data sheet Specifications). The UVLO circuitry ensures a clean transition during power-up and power-down, allowing the converter to tolerate a slow-rising input voltage. For most applications EN1 and EN2, can be configured for automatic power-up.

### Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect EN1 (pin 2) to $-V_{in}$ (pin 4), and apply the system On/Off control signal to EN2 (pin 1). In this configuration, a low-level input voltage ($-V_{in}$ potential) applied to pin 4 disables the converter outputs. Figure 1 is an example of this configuration.

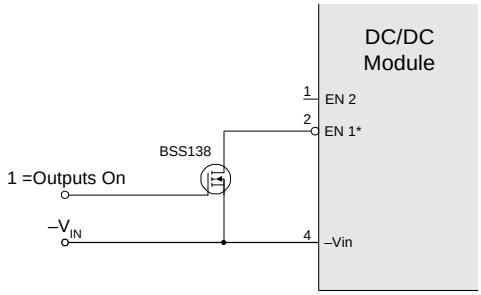
***Figure 1; Positive Enable Configuration***




### Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, EN2 (pin 1) is left open circuit, and the system On/Off control signal is applied to EN1 (pin 2). A low-level input voltage ($-V_{in}$ potential) must then be applied to pin 2 in order to enable the outputs of the converter. An example of this configuration is detailed in Figure 2. *Note: The converter will only produce and output voltage if a valid input voltage is applied to $\pm V_{in}$.*

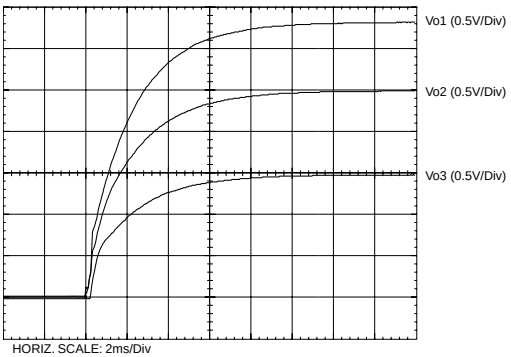
***Figure 2; Negative Enable Configuration***




### On/Off Output Voltage Sequencing

The power-up characteristic of the PT4820 series of DC/DC converters meets the requirements of microprocessor and DSP chipsets. All three outputs from the converter are internally sequenced to power up in unison. Figure 3 shows the waveforms from a PT4821 after power is applied to the input of the converter. During power-up, $Vo_1$ initially rises to approximately 0.8V. This is followed by $Vo_2$ and $Vo_3$, which promptly rise to the same voltage as $Vo_1$. All three output voltages then rise together until each reaches their respective output voltage. The waveforms of Figure 3 were measured with loads of approximately 50% on each output, with an input source of 48VDC. The converter typically produces a fully regulated output within 60ms of applying $V_{in}$.

***Figure 3; $Vo_1$, $Vo_2$, $Vo_3$ Power-Up Sequence***




During turn-off, all outputs drop rapidly due to the discharging effect of actively switched rectifiers. The discharge time is typically 100µs, but will vary with the amount of external load capacitance.

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