



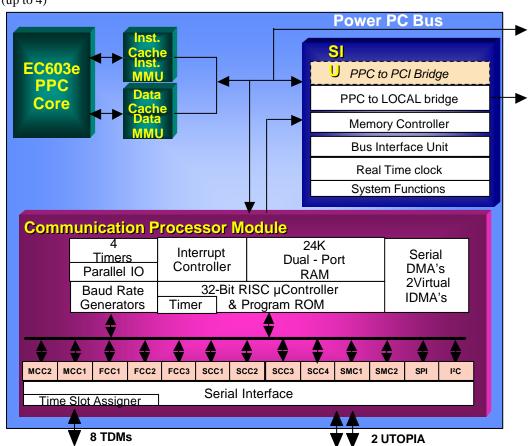
# PC8260 PowerQUICCII™ Microprocessor Fact Sheet

The PC8260 PowerQUICCII is the most advanced integrated communication microprocessor ever designed for the telecommunications and networking markets. The PC8260 can be described as the next generation PowerQUICC providing higher performance in all areas of device operation, including greater flexibility, extended capabilities, and higher integration. Like the PC860, the PC8260 integrated two main components, the embedded PowerPC<sup>™</sup> core and the Communication Processor Module (CPM). The CPM simultaneously supports three fast serial communications controllers (FCCs), two multichannel controllers (MCCs, four serial communications controllers (SCCs), two serial management controllers (SMCs), one serial peripheral interface (SPI) and one I²C interface. The combination of the PowerPC core and the CPM, along with the versatility and performance of the PC8260, provides customers with enormous potential in developing networking and communications products while significantly reducing time-to-market development stages.

#### PC8260 Main Features

- 32-bit embedded PowerPC core up to 200 MHz
- System Interface Unit
- **■** Communication Processor Module (CPM)
  - Enhanced 32-bit RISC communication controller
  - 3 FCCs, 2 MCCs, 4 SCCs, 2 SMCs, 1 SPI and 1 I<sup>2</sup>C
  - Multi-port 10/100 Mbps Ethernet (up to 3)
  - 155 Mbps ATM-SAR (up to 2)
  - 256 HDLC channels (each channel 64 Kbps, full-duplex)
  - 10 Mbps Ethernet (up to 4)











## **PC8260 Technical Specifications**

#### ■ EC603e<sup>TM</sup> microprocessor (embedded PowerPC core) up to 200 MHz

- 280.0 MIPS at 200 MHz (Dhrystone 2.1)
- Low-power core with 16KB data and 16KB instruction cache, 4-way set associative
- Disable CPU mode
- Memory management unit
- Floating point unit (FPU)
- Common on-chip processor (COP)

#### ■ System Interface Unit (SIU)

- Memory controller, including two dedicated SDRAM machines
- Hardware bus monitor and software watchdog timer
- IEEE 1149.1 JTAG test access port (TAP)

### ■ High-Performance Communication Processor Module (CPM) up to 166 MHz

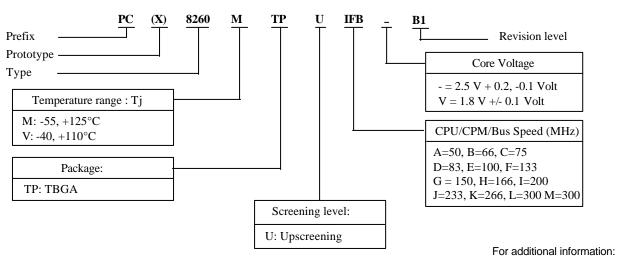
- PowerPC core and CPM may run at different frequencies
- Supports serial bit rate up to 710 Mbps at 133 MHz
- Parallel I/O registers
- On-board 24KB of dual-port RAM
- 2 multi-channel controllers (MCCs), each supporting 128 full-duplex, 64 Kbps, HDLC lines
- Virtual DMA functionality
- 3 FCCs supporting:
  - Full 155 Mbps ATM SAR (up to 2) (AAL0, AAL1, AAL5)
  - 10/100 Mbps Ethernet (up to 3) (IEEE 802.3x with flow Control)
  - 45 Mbps HDLC / Transparent (up to 3)
- 2 bus architectures: one 64-bit PowerPC bus and one 32-bit local bus
- 2 UTOPIA Level II master/slave ports, both with multi-PHY support
- 3 MII interfaces
- 8 TDM interfaces (T1/E1), 2 TDM ports can be interfaced with (T3/E3)

### Packaging

- 480 TBGA package (37.5 x 37.5 mm)

#### Screening

- TBGA upscreening based upon ATMEL-Grenoble standards
- Full military temperature range ( $Tc = -55^{\circ}C$ , +  $125^{\circ}C$ )
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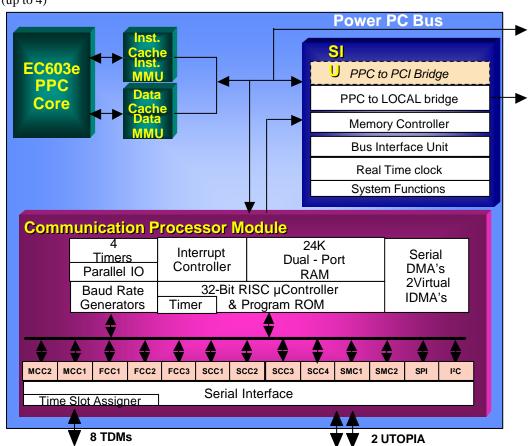
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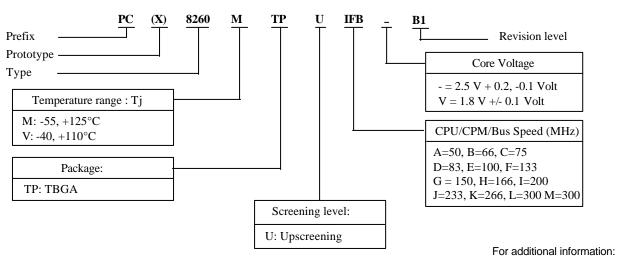
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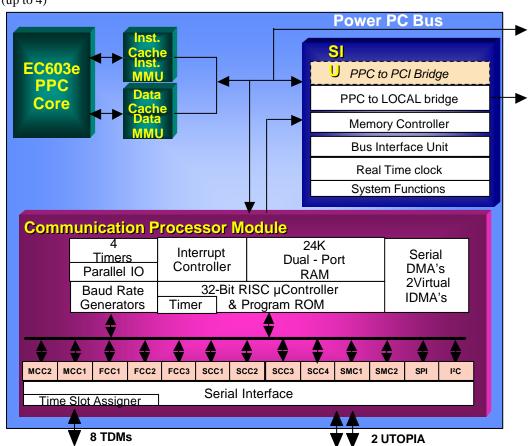
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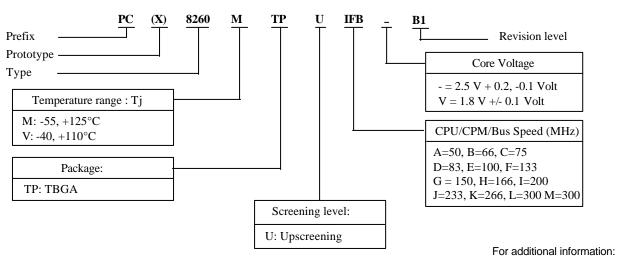
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