

PC740A and 750A PowerPC™ Microprocessors

Fact Sheet

The PowerPC 750 and PowerPC740 microprocessors are low-power 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture. The PowerPC 750 and the PowerPC 740 micro-processors differ only in that the PowerPC 750 features a dedicated L2 cache interface with on-chip L2 tags.

Both are software-compatible and bus-compatible with the PowerPC603e™ micro-processor families, and the PowerPC 740 is pin-compatible as well. PowerPC 750/740 micro-processors are fully JTAG-compliant.

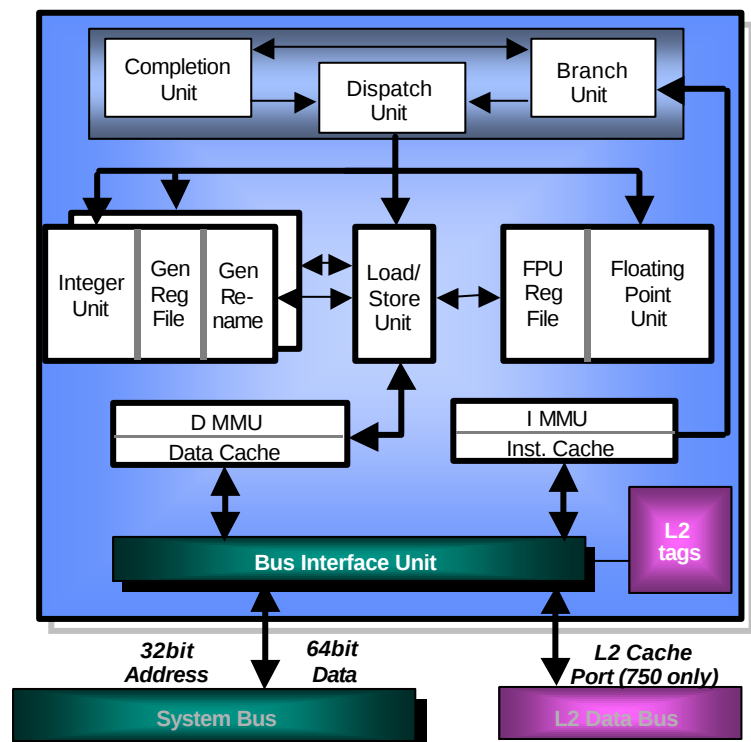
PC740/750 Main Features

■ Six independent execution units :

- Two integer units
- Floating-point unit
- Branch processing unit
- Load/store unit
- System register unit

■ Cache and MMU Support

- 32-Kbytes, physically-addressed instruction and data cache
- 8-way set-associative
- Dedicated L2 cache interface with on-chip L2 tags (PC750, only)
- Separate Instruction and Data MMUs
- Virtual memory support up to 4 Petabytes (2^{52})
- Real memory support up to 4 Gigabytes (2^{32})
- 128-entry instruction and data TLBs



■ Bus Interface

- Compatible with 60x processor interface
- 32 bit address bus
- 64-bit data bus
- 11 Bus -to- Core frequency multipliers

■ Power Management

- Low-power design
- 3 static power saving modes : doze, nap and sleep
- Dynamic power management
- Integrated thermal management unit

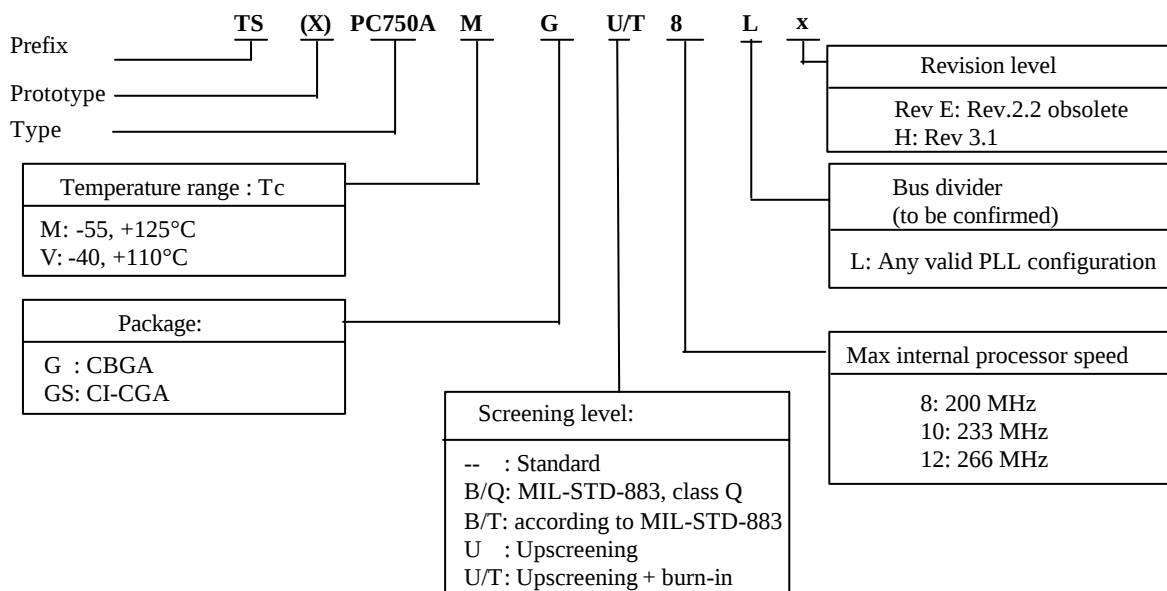
■ Packaging

- PC740 : 255 pin CBGA and CI-CGA
- PC750 : 360 pin CBGA and CI-CGA

■ Screening

- CBGA upscreening upon Atmel-Grenoble standards
- CI-CGA up to QML class Q
- Full military range (Tj = -55°C +125°C)
- Industrial temperature range (Tj = -40°C +85°C)

	PC740A 200 - 266 MHz	PC750A 200 - 266 MHz
Motorola Name	MPC740PID8t	MPC750PID8t
Die Revision	3.1 = H	3.1 = H
CPU Speeds - Internal	200 MHz	200 MHz
	233 MHz	233 MHz
	266 MHz	266 MHz
CPU Bus Dividers	3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x	3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x
Bus Interface	32-bit address, 64-bit data	32-bit address, 64-bit data
Instructions per Clock	3 (2+Branch)	3 (2+Branch)
L1 Cache	32-KB Instruction and Data	32-KB Instruction and Data
L2 Cache	-	256KB, 512KB, 1MB
Core-to-L2 Frequency Divisions	-	1:1, 1.5:1, 2:1, 2.5:1, 3:1
Tvp/Max Power Dissipation	5.7W/7.9W @ 266 MHz	5.7W/7.9W @ 266 MHz
Die Size	67 mm ²	67 mm ²
Package	255-pin Flip-Chip CBGA	360-pin Flip-Chip CBGA
	255-pin Flip-Chip CI-CGA	360-pin Flip-Chip CI-CGA
Process	0.29µ CMOS, 5LM	0.29µ CMOS, 5LM
Voltage	3.3V I/O	3.3V I/O
	2.6V internal	2.6V internal
SPECint95 (estimated)	11.5 @ 266 MHz	12.0 @ 266 MHz
SPECfp95 (estimated)	6.9 @ 266 MHz	7.4 @ 266 MHz
Other Performance	488 MIPS @ 266 MHz	488 MIPS @ 266 MHz
Status	Active	Active
Samples	Now	Now
Production	Now	Now
Execution Units	Integer (2)	Integer (2)
	Floating Point Unit	Floating Point Unit
	Branch Unit	Branch Unit
	Load/Store Unit	Load/Store Unit
	System Register	System Register



For additional information:
 contact your local ATMEL-Grenoble representative
 or visit our web site at <http://www.atmel-grenoble.com>



You may also contact the PowerPC technical hotline at std.hotline@atmel-grenoble.com

The PowerPC and PowerPC603e names and the PowerPC logotype are trademarks of International Business Machines Corporation, used under license therefrom.