6 CHANNEL ESD PROTECTION ARRAY

Features

- Six channels of ESD protection
- 15KV ESD protection (HBM)
- 8KV contact, 15KV air ESD protection per IEC 1000-4-2
- Low loading capacitance, 3 pF typ.
- Miniature 8-pin MSOP or SOIC package

Applications

- I/O port protection for cellular phones, notebook computers, PDAs, etc.
- ESD protection for VGA (Video) port in PC's or Notebook computers
- ESD protection for sensitive electronic equipment.

Product Description

The PAC DN006™ is a diode array designed to provide 6 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers the ESD current pulse either to the positive (V_P) or negative (V_N) supply. The PAC DN006 will protect against ESD pulses up to 15 KV Human Body Model (100 pF capacitor discharging through a 1.5KΩ resistor) and 8KV contact discharge per International Standard IEC1000-4-2.

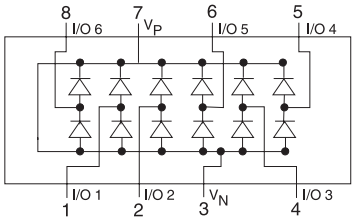
This device is particularly well-suited for portable electronics (e.g. cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripheral equipment.

ABSOLUTE MAXIMUM RATINGS

Diode Forward DC Current (Note 1)	20mA
Storage Temperature	-65°C to 150°C
Operating Temperature Range	0°C to 70°C
DC Voltage at any Channel Input	V_N-0.5V to V_P+0.5V

Note 1: Only one diode conducting at a time.

SCHEMATIC CONFIGURATION

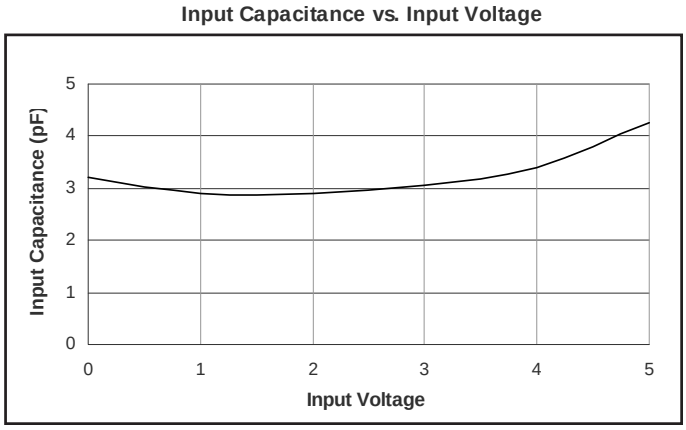


STANDARD SPECIFICATIONS

Parameter	Min.	Typ.	Max.
Operating Supply Voltage (V_P-V_N)			5.5 V
Diode Forward Voltage, I_F = 20mA, T = 25°C	0.65 V		0.95 V
Diode reverse breakdown voltage, T = 25°C	17.0 V		
ESD Protection Peak Discharge Voltage at any Channel Input, in-system (Note 2) Human Body Model, Method 3015 (Note 3, 4) Contact Discharge per IEC 1000-4-2 (Note 5) Air Discharge per IEC 1000-4-2 (Note 5)	 ±15 KV ±8KV ±15KV		
Channel Clamp Voltage @ 15KV ESD HBM, T = 25°C (Notes 3, 4) Positive transients Negative transients			 V_P+13.0 V V_N-13.0 V
Channel Leakage Current, T = 25°C		0.1 μA	1.0 μA
Channel Input Capacitance (Measured @ 1 MHz) V_P = 5V, V_N = 0V, V_{INPUT}= 2.5V		3pF	6pF
Package Power Rating SOIC Package MSOP Package			 350mW 200mW

Note 2: From I/O pins to V_P or V_N only. V_P bypassed to V_N with 0.2 μF ceramic capacitor.
Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$=100pF, $R_{Discharge}$=1.5KΩ, V_P=5.0V, V_N=GND.
Note 4: This parameter is guaranteed by design and characterization.
Note 5: Standard IEC1000-4-2 with $C_{Discharge}$=150pF, and $R_{Discharge}$=330Ω, V_P=5V, V_N=GND.

© 1999 California Micro Devices Corp. All rights reserved.
PAC DN006™ is a trademark of California Micro Devices Corp.



Typical variation of C_{IN} with V_{IN}. (V_P=5V, V_N=0V)

STANDARD PART ORDERING INFORMATION				
Package		Ordering Part Number		
Pins	Style	Tubes	Tape & Reel	Part Marking
8	SOIC	PACDN006S/T	PACDN006S/R	PDN006S
8	MSOP	PACDN006M/T	PACDN006M/R	D006

Application Information

See also California Micro Devices Application Note AP 209, " Design Considerations for ESD Protection."

In order to realize the maximum protection against ESD pulses with the PAC DN006, care must be taken in the PCB layout to minimize the parasitic series inductance to the Supply and Ground rails. Refer to Figure 1, which illustrates the case of a positive ESD pulse applied between an input channel and Chassis Ground. The parasitic series inductance back to the power supply is represented by L_1. The voltage V_Z on the line being protected is:

$$V_Z = \text{Forward voltage drop of } D_1 + L_1 \times d(I_{esd})/dt + V_{Supply}$$

where I_{esd} is the ESD current pulse, and V_{Supply} is the positive supply voltage.

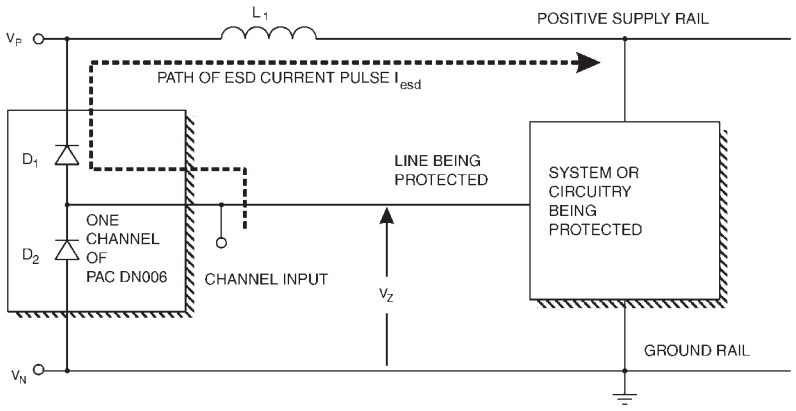


Figure 1

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, consider the case of an ESD pulse that rises from zero to 10 Amps in 1nS. Here $d(I_{esd})/dt$ can be approximated by $\Delta I_{esd}/\Delta t$, or $10/(1 \times 10^{-9})$. So each nano Henry of series inductance (L_1) will lead to a 10V increment in V_Z.

©1999 California Micro Devices Corp. All rights reserved.

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_Z equation above, the V_{Supply} term, in reality, is given by ($V_{DC} + I_{esd} \times R_{out}$), where V_{DC} and R_{out} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{out} of 1 ohm would result in a 10V increment in V_Z for a peak I_{esd} of 10A. To mitigate this effect, a high frequency bypass capacitor should be connected between the V_P pin of the PAC DN006 and the ground plane. The value of this bypass capacitor should be chosen such that it will absorb the charge transferred by the ESD pulse with minimal change in Vp. Typically a value in the 0.1 μF to 0.2 μF range is adequate for IEC-1000-4-2, level 4 contact discharge protection (8KV). Ceramic chip capacitors mounted with short printed circuit board traces are a good choice for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the PAC DN006 should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the PAC DN006 as possible, with minimum PCB trace lengths to the power supply and ground planes to minimize stray series inductance.

Implementation Examples

ESD events are very high speed pulses with rise times in the range of 1 nS or less. To effectively use the PAC DN006, the following design guidelines must be observed (as discussed in the application section):

1. The inductance from the V_N and V_P connections of the PAC DN006 to ground must be very low. This includes the path through the V_P decoupling capacitor to ground and the path to the power supply (as discussed above).

2. The inductance between the connector pin to be protected and the PAC DN006 channel input pin must be kept to a minimum. (If there is a large inductance here, the ESD event will find a lower impedance path which will more likely be through the device to be protected.) Figure 2 shows the implementation schematic and Figure 3 shows a possible layout for the PAC DN006. In Figure 3, notice the large V_{CC} and ground areas with multiple via connections to the underlying reference planes and the positioning of the bypass capacitor. Note how the signal lines to be protected flow from the connector to the PAC DN006 and then out to the device to be protected (Figures 3, 4, and 5). This daisy chaining provides a low impedance path from the connector to the PAC DN006 and a higher impedance path from the PAC DN006 to the protected device.

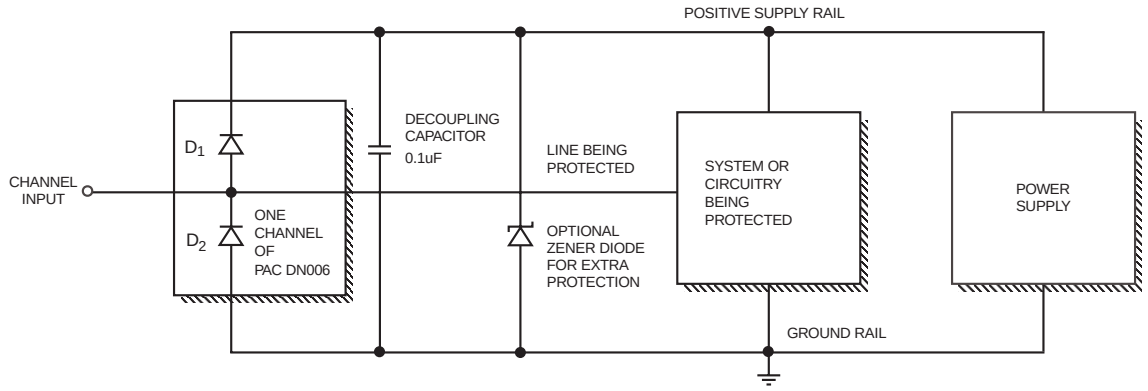


Figure 2

© 1999 Calirornia Micro Devices Corp. All rights reserved.

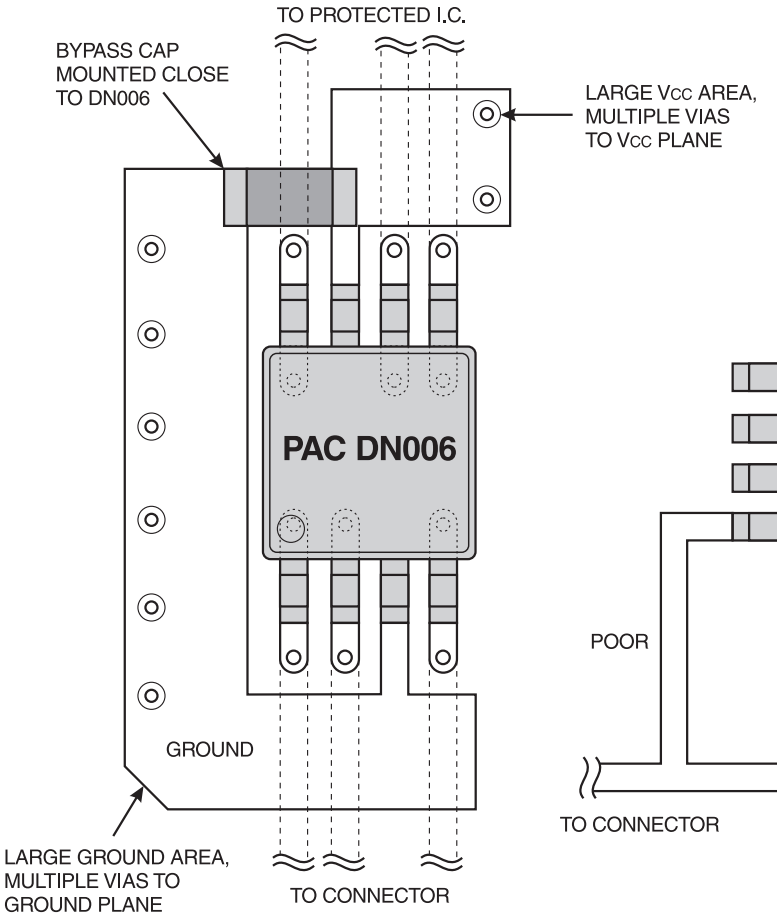


Figure 3

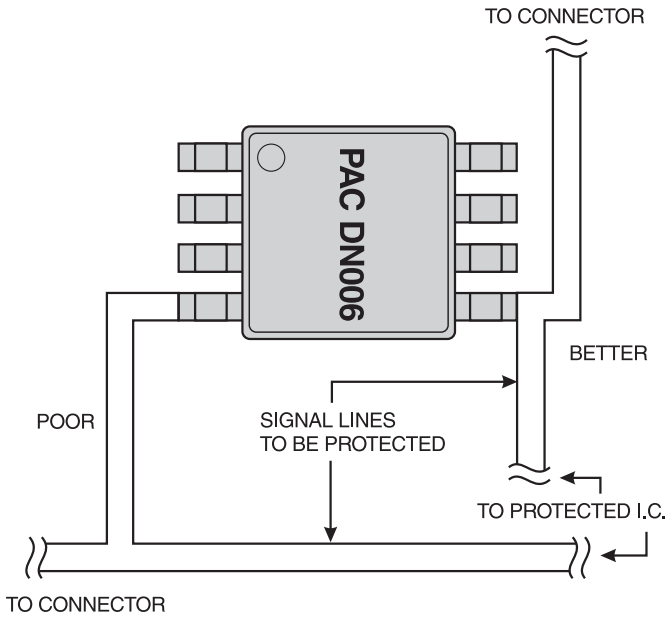


Figure 4

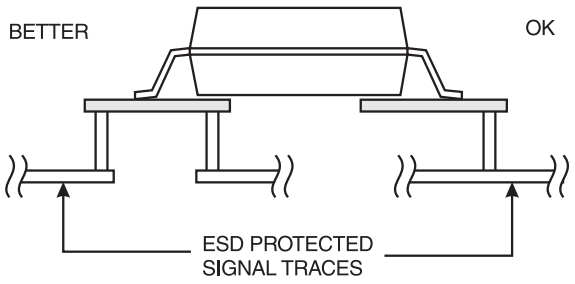
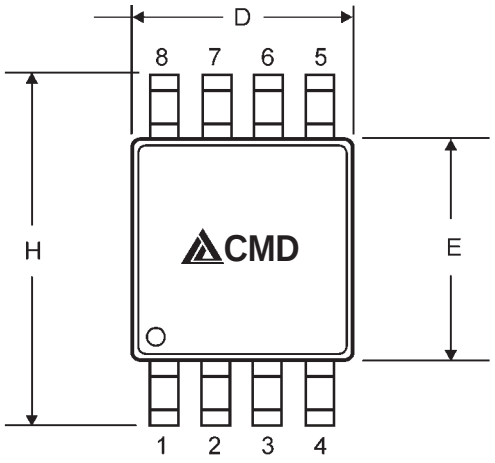
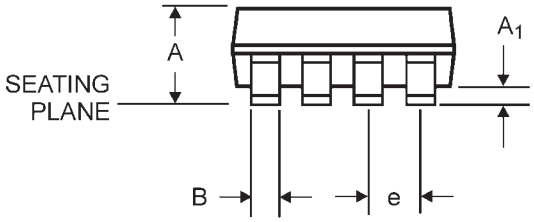


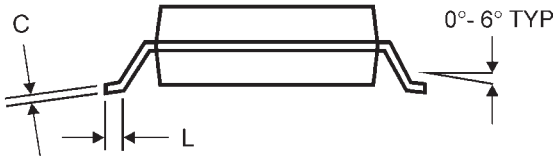
Figure 5

© 1999 Calirornia Micro Devices Corp. All rights reserved.

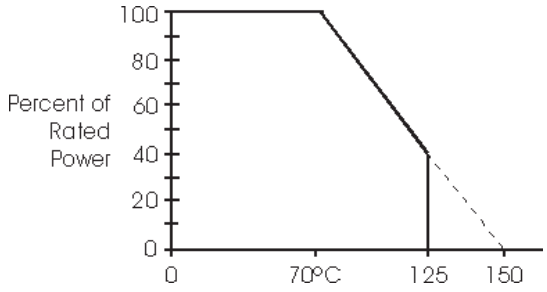
MSOP - TOP VIEW







Power Derating Curve

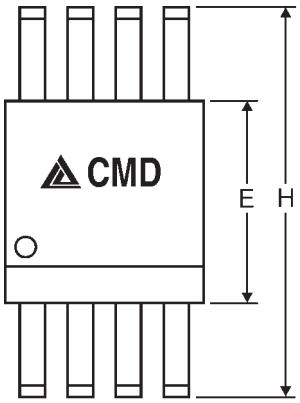


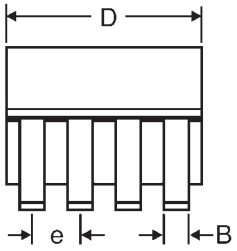
Mechanical Specifications	
Lead Plating	Tin-Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004" (0.102mm)
Substrate Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94V-0

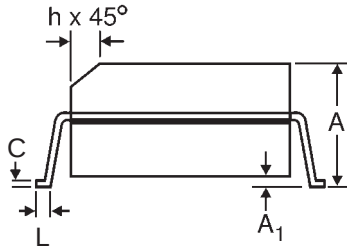
Package Dimensions, Power Dissipation & Information				
Package	**MSOP**			
Pins #	**8**			
JEDEC	**MO 187**			
	mm		**inches**	
	min	**max**	**min**	**max**
A	0.94	1.09	0.037	0.043
A_1	0.05	0.15	0.002	0.006
B	0.20	0.40	0.008	0.016
C	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.64 BSC		0.025 BSC	
H	4.78	4.98	0.188	0.196
L	0.40	0.69	0.016	0.027
P_D @ 70 C	**200mW**			
# / tube	**50 pcs**			
# / tape & reel	**2,500 pcs**			

©1999 California Micro Devices Corp. All rights reserved.

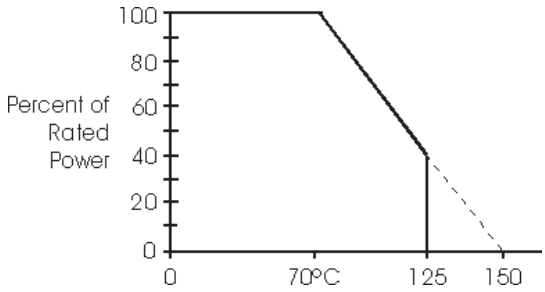
SOIC - TOP VIEW







Power Derating Curve



Mechanical Specifications	
Lead Plating	Tin-Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004" (0.102mm)
Substrate Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94V-0

Package Dimensions, Power Dissipation & Information

Package	SOIC			
Pins #	8			
JEDEC	MS 012			
	mm		inches	
	min	max	min	max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.500 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.099	0.0196
L	0.40	1.27	0.016	0.050
P_D @ 70 C	500mW			
# / tube	100 pcs			
# / tape & reel	2,500 pcs			

Printed on recycled Paper

©1999 California Micro Devices Corp. All rights reserved.

C0240298D

215 Topaz Street, Milpitas, California 95035 ▲ Tel: (408) 263-3214 ▲ Fax: (408) 263-7846 ▲ www.calmicro.com