2 CHANNEL ESD PROTECTION ARRAY

Features

- 2 channel ESD protection
- 15KV ESD protection (HBM)
- 8KV contact, 15KV air ESD protection per IEC 1000-4-2
- Low loading capacitance, 3 pF typ.
- Miniature 4-pin SOT-143 package

Applications

- I/O port: protection for cellular phones, notebooks computers, PDA, etc.
- ESD protection for sensitive electronic equipment.
- ESD protection for applications where low capacitive loading is required.

Product Description

The PAC DN004™ is a diode array designed to provide two channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers the ESD current pulse either to the positive (V_P) or negative (V_N) supply. The PAC DN004 will protect against ESD pulses up to 15 KV Human Body Model, and 8KV contact discharge per International Standard IEC1000-4-2.

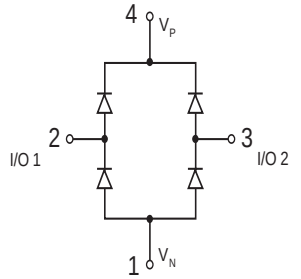
This device has identical characteristics as the PAC DN006 (6 channel array). They can be used together in order to provide a larger number of protected inputs if required. This device is particularly well-suited for portable electronics (e.g. cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripheral equipment.

ABSOLUTE MAXIMUM RATINGS

Diode Forward DC Current (Note 1)	20mA
Storage Temperature	-65°C to 150°C
Operating Temperature Range	0°C to 70°C
DC Voltage at any Channel Input	V_N-0.5V to V_P+0.5V

Note 1: Only one diode conducting at a time.

SCHEMATIC CONFIGURATION



STANDARD SPECIFICATIONS

Parameter	Min.	Typ.	Max.
Operating Supply Voltage (V_P-V_N)			5.5 V
Diode Forward Voltage, I_F = 20mA, T = 25°C	0.65 V		0.85 V
Diode reverse breakdown voltage, T = 25°C			
Top Diode (Cathode to V_P)	19.0 V		
Bottom Diode (Anode to V_N)	28.0 V		
ESD Protection			
Peak Discharge Voltage at any Channel Input, in-system (Note 2)			
Human Body Model, Method 3015 (Note 3, 4)	-15 KV		+15 KV
Contact per IEC 1000-4-2 (Note 5)	-8KV		+8KV
Air Discharge per IEC 1000-4-2 (Note 5)	-15KV		+15KV
Channel Clamp Voltage @ 15KV ESD HBM, T = 25°C (Notes 3, 4)			
Positive transients			V_P+13.0 V
Negative transients			V_N-13.0 V
Channel Leakage Current, T = 25°C		0.1 μA	1.0 μA
Channel Input Capacitance (Measured @ 1 MHz) V_P = 5V, V_N = 0V, V_{IN} = 2.5V		3pF	6pF
Package Power Rating			225mW

Note 2: From I/O pins to V_P or V_N only. V_P bypassed to V_N with 0.2 μF ceramic capacitor.
Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$=100pF, $R_{Discharge}$=1.5KΩ, V_P=5.0V, V_N=GND.
Note 4: This parameter is guaranteed by characterization only.
Note 5: Standard IEC1000-4-2 with $C_{Discharge}$=150pF, and $R_{Discharge}$=330Ω, V_P=5V, V_N=GND.

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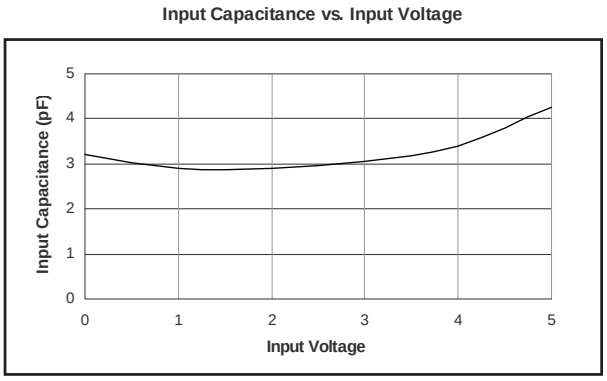


Typical variation of C_{IN} with V_{IN}. (V_P=5V, V_N=0V)

STANDARD PART ORDERING INFORMATION				
Package		Ordering Part Number		
Pins	Style	Bag	Tape & Reel	Part Marking
4	SOT-143	PACDN004M/B	PACDN004M/R	D004

Application Information

In order to realize the maximum protection against ESD pulses with the PAC DN004, care must be taken in the PCB layout to minimize the parasitic series inductance to the Supply and Ground rails. Refer to Figure 1, which illustrates the case of a positive ESD pulse applied between an input channel and Chassis Ground. The parasitic series inductance back to the power supply is represented by L_1. The voltage V_Z on the line being protected is:

V_Z = Forward voltage drop of D_1 + L_1 x $d(I_{esd})/dt$ + V_{Supply}

where I_{esd} is the ESD current pulse, and V_{Supply} is the positive supply voltage.

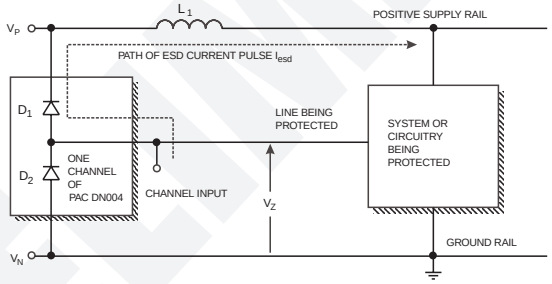


Figure 1

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, consider the case of an ESD pulse that rises from zero to 10 Amps in 1nS. Here $d(I_{esd})/dt$ can be approximated by $\Delta I_{esd}/\Delta t$, or $10/(1x10^{-9})$. So each nano Henry of series inductance (L_1) will lead to a 10V increment in V_Z.

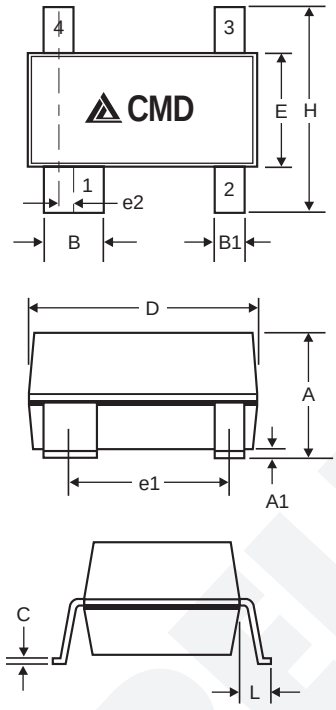
Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_Z equation above, the V_{Supply} term, in reality, is given by (V_{DC} + I_{esd} x R_{out}), where V_{DC} and R_{out} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{out} of 1 ohm would result in a 10V increment in V_Z for a peak I_{esd} of 10A. To mitigate this effect, a high frequency bypass capacitor should be connected between the V_P pin of

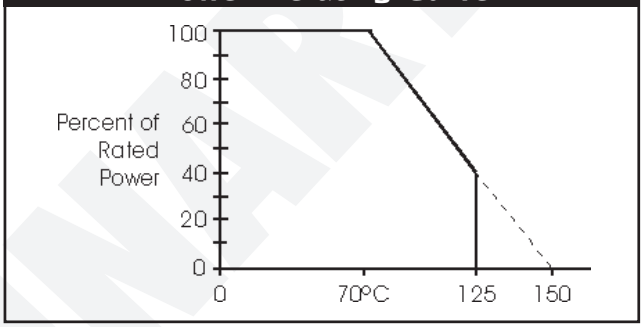
the PAC DN004 and the ground plane. The value of this bypass capacitor should be chosen such that it will absorb the charge transferred by the ESD pulse with minimal change in Vp. Typically a value in the 0.1 μF to 0.2 μF range is adequate for IEC-1000-4-2, level 4 contact discharge protection (8KV). Ceramic chip capacitors mounted with short printed circuit board traces are a good choice for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the PAC DN004 should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the PAC DN004 as possible, with minimum PCB trace lengths to the power supply and ground planes to minimize stray series inductance.

SOT-143 - TOP VIEW



Power Derating Curve



Mechanical Specifications

Lead Plating	Tin-Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004" (0.102mm)
Substrate Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94V-0

Package Dimensions, Power Dissipation & Information

Package	SOT-143			
Pins	4			
	mm		inches	
	min	max	min	max
A	0.890	1.120	0.035	0.044
A1	0.013	0.100	0.0005	0.004
B	0.760	0.940	0.030	0.037
B1	0.370	0.510	0.015	0.020
C	0.0850	0.180	0.0033	0.0071
D	2.800	3.040	0.110	0.120
E	1.200	1.400	0.047	0.055
e1	1.920 BSC		0.076 BSC	
e2	0.20 BSC		0.008 BSC	
H	2.100	2.640	0.083	0.104
L	0.55 ref		0.022 ref	
P_D @ 70 C	.225W			
# / bag	1000 pcs			
# / tape & reel	2,500 pcs			

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