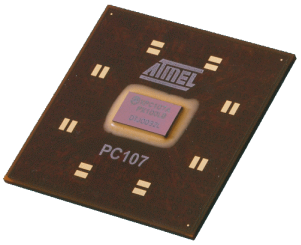
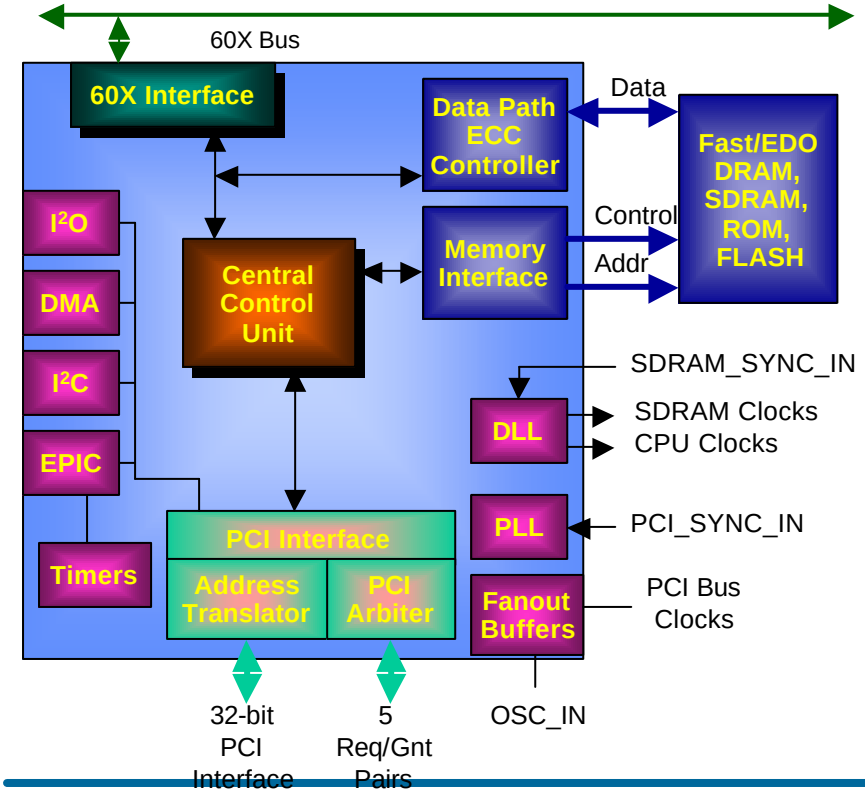
PC107 PCI Bridge & Memory Controller
Fact Sheet

The PC107 PCI Bridge & Memory Controller provides a PowerPC™ architecture compliant bridge between PowerPC microprocessors and the Peripheral Component Interconnect (PCI) bus. PCI support allows system designers to design systems quickly using peripherals already designed for PCI and other standard interfaces available in the personal computer hardware environment. The PC107 provides many of the other necessities for embedded applications including a high performance memory controller and dual processor support, 2-channel flexible DMA controller, an interrupt controller, and I²O-ready message unit, an I²C controller, and low skew clock drivers. The PC107 contains an Embedded Programmable Interrupt Controller (EPIC) featuring five hardware interrupts (IRQs) as well as 16 serial interrupts along with 4 timers. The PC107 uses an advanced, 2.5V HiP3 process technology and is fully compatible with TTL devices.

PC107 Main Features

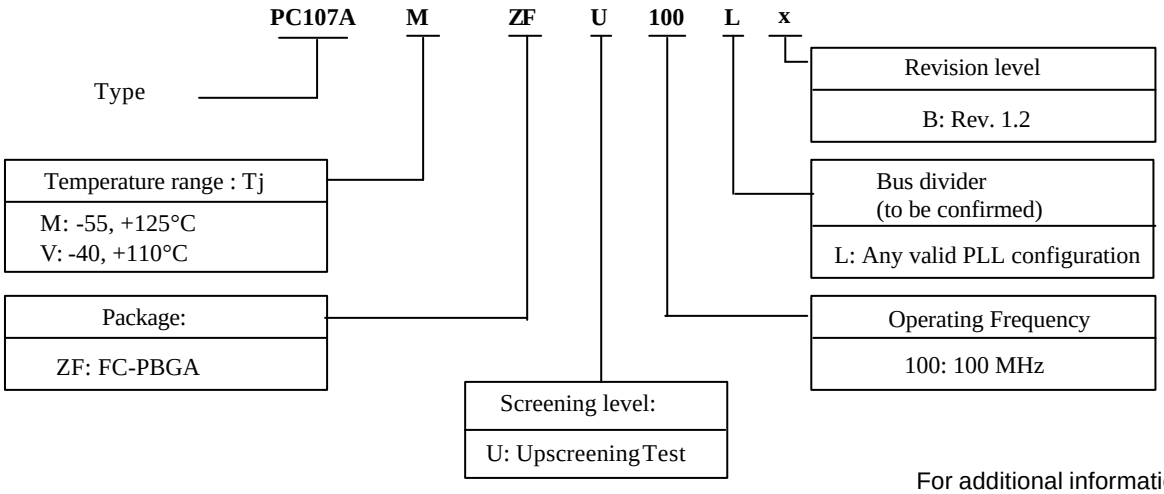


- **Multiprocessor and Local Bus Slave support**
  - Supports PowerPC 603e™, PowerPC 740™, PowerPC 750™ or PowerPC 7400™ microprocessors
  - Operating bus frequency up to 100 MHz
  - Supports either a second processor or a local bus slave
- **PCI Bus support**
- **Integrated memory controller**
  - Controls processor and PCI interactions to main memory
  - Supports a variety of DRAM (FPM, EDO), SDRAM, and ROM/Flash ROM up to 100 MHz
- **Power Management**
  - Provides hardware support for 4 level of power reduction: nap, doze, sleep and suspend
  - Fully static design preserving internal logic states during power saving modes



PC107 Technical Specifications

- **Processor Interface**
  - Processor bus frequency up to 100 MHz
  - 64-bit or 32-bit data bus and 32-bit address bus
  - SMP support for a second processor
  - Full memory coherency supported, integrated arbiter and slave peripheral support
  - JTAG/COP for in-circuit hardware debugging
  - IEEE 1149.1 compliant, JTAG boundary-scan interface
- **PCI Interface**
  - Compliant with PCI specification, revision 2.1
  - 32-bit PCI interface operates up to 66 MHz
  - PCI 5.0V tolerant
  - Read and write buffers to improve PCI performance
  - Selectable big or little endian operation
  - PCI interface can be configured as host or agent, allowing multiple PC107 chips on same PCI bus
  - Arbiter supports up to 5 other PCI devices
  - Parity support
- **Memory Interface**
  - High bandwidth (32/64-bit) data bus up to 100 MHz
  - Programmable timing supporting either DRAM (FPM, EDO) or SDRAM
  - Support 1 to 8 banks - 4MB, 16MB, 64MB, 128MB, and/or 256MB DRAMs or SDRAMs
  - 1GB of RAM space, 144MB of ROM space
  - 8-bit, 32-bit or 64-bit ROM/Flash ROM
  - PortX: 8-, 32-, or 64-bit general-purpose I/O port uses ROM controller interface with address strobe
  - Supports parity, read-modify-write, or error correcting code (ECC)
- **Other Embedded Features**
  - Two-Channel integrated DMA controller
  - Message Unit and I²C controller
  - Embedded Programmable Interrupt Controller (EPIC)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI and memory bus drivers
- **Packaging**
  - 503 Flip-Chip PBGA package
- **Screening**
  - FC-PBGA upscreening based upon ATMEL-Grenoble standards
  - Full military temperature range (Tj = -55°C, + 125°C)
  - Industrial temperature range (Tj = -40°C, +110°C)



For additional information:
contact your local ATMEL-Grenoble representative
or visit our web site at http://www.atmel-grenoble.com

You may also contact the PowerPC technical hotline at std.hotline@atmel-grenoble.com

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