High Performance Four Independent Programmable Clocks

FEATURES

- Four Independent clocks programmable from DC to 200MHZ Step as low as 7.8khz.
- Sleep Mode between DC, 250khz or arbitrary External Clock.
- Glitch free Switching time less than 32Microsecond.
- Outputs Rise and Fall times programmable.
- External clock multiplexing for easy expansion.
- Expandable to 2 chips per board without additional external decoder.
- Additional output clocks division from 1 to 128 by binary increment.
- Serial programming of 22 bit word.
- First output can be hardwired for 10MHZ at Power-On.
- All outputs can be disabled.
- Separate Analog and Digital Power Supplies.
- Low jitter noise (less than 150ps).
- Symmetrical duty cycle.
- Uses 10 Mhz crystal .
- Low power (less than 5 mA per VCO)
- Requires only few external capacitors.
- CMOS technology.

DESCRIPTIONS

The PhaseLink Labs PLL51C04 incorporates 4 independent outputs with associated VCO frequencies programmable from 0 to 200 Mhz with 1MHz step using Phase Locked Loop technique. In addition to 1 Mhz step, the outputs clocks is further divided down by output dividers programmable from 1 to 128 by binary increment.

The sleep mode of the chip is composed of 3 different modes : VCO frequencies, 250 Khz and External frequency. In addition to these sleep modes, all VCO, crystal oscillators and outputs can be disabled independently.

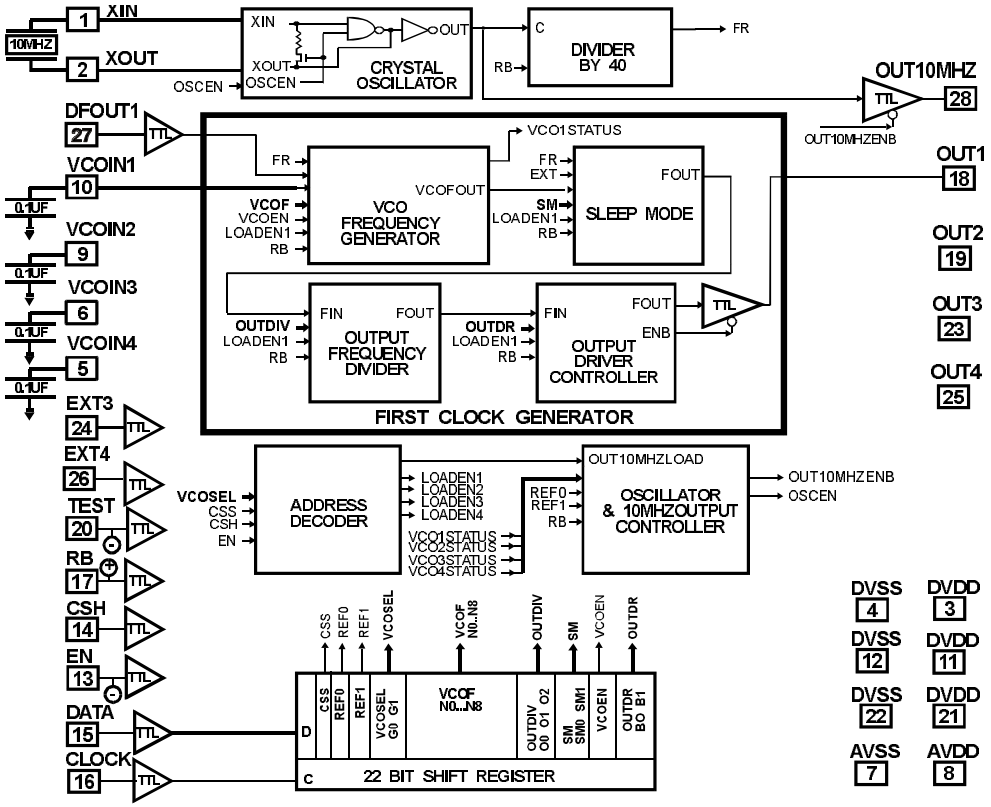
Each output has 3 independent programmable output buffers for customization of the rise and fall times.

APPLICATIONS

This high performance, low cost device offers significant advantage over crystal oscillators where multiple variable clock sources are needed such as :

- High performance disk drives
- High speed computers
- Test equipment.
- Tuning devices
- SCSI Host Adapter boards
- Graphics controllers

BLOCK SCHEMATICS



Notes :
DFOUTI applies only to First Clock Generator,
EXT signal for First and Second Clock Generator is FR
EXT for Third and Fourth Clock Generator is EXT3 and EXT4 respectively.

TABLE 1
PROGRAMMING DATA WORD STRUCTURE

BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSS	***REF0***	***REF1***	***VCOSEL***		***VCOF***									***OUTDIV***			***SM***		***VCOEN***	***OUTDR***	
CSS	REF0	REF1	G0	G1	N0	N1	N2	N3	N4	N5	N6	N7	N8	O0	O1	O2	SM0	SM1	VCOEN	B0	B1
Chip Select *TABLE 2*	Osc Enable *TABLE 3*	OUTPUT 10MHZ Enable *TABLE 4*	Select VCO for LOADING *TABLE 5*		VCO frequency selection *TABLE 6*									Output Divider *TABLE 7*			Sleep Mode *TABLE 8*		VCO Enable *TABLE 9*	Output Drivers Selection *TABLE 10*	

TABLE 2
CHIP SELECT FOR LOADING OF PROGRAMMING DATA WORD

CSS	***CHIP SELECT***
0	SELECT CHIP with CSH=0 for programming
1	SELECT CHIP with CSH=1 for programming

TABLE 3
CRYSTAL OSCILLATOR CONTROL

REF0	***10 MHZ OSCILLATOR***
0	OFF
1	ON

TABLE 4
10MHZ OUTPUT CONTROL

REF1	***OUT10MHZ***
0	TRISTATE
1	ON

TABLE 5
SELECTION OF VCO FOR LOADING OF DATA WORD

VCOSEL		***LOAD REGISTER for***
G0	***G1***	
0	0	CLOCK GENERATOR 1
1	0	CLOCK GENERATOR 2
0	1	CLOCK GENERATOR 3
1	1	CLOCK GENERATOR 4

TABLE 6
VCO FREQUENCY PROGRAMMING

VCOF									DECIMAL	***VCO FREQUENCY***
N0	***N1***	***N2***	***N3***	***N4***	***N5***	***N6***	***N7***	***N8***	VALUE	
0	0	0	0	0	0	0	0	0	0	UNDEFINED
1	0	0	0	0	0	0	0	0	1	1 MHZ
0	1	0	0	0	0	0	0	0	2	2 MHZ
.	.	.	.	.	.	.	.	.	3-199	3-199 MHZ
0	0	0	1	0	0	1	1	0	200	200 MHZ
									201-511	NOT TO BE USED

TABLE 7
SLEEP MODE

SM		***FREQUENCIES***
SM0	***SM1***	
0	0	NORMAL (FROM VCO)
1	0	NORNAL (FROM VCO)
0	1	INTERNAL REF (250KHZ)
1	1	EXTERNAL REF (EXT)

TABLE 8
OUTPUT DIVIDER

OUTDIV			***OUTPUT DIVIDER RATIO***
O0	***O1***	***O2***	
0	0	0	DIVIDE BY 1
1	0	0	DIVIDE BY 2
0	1	0	DIVIDE BY 4
1	1	0	DIVIDE BY 8
0	0	1	DIVIDE BY 16
1	0	1	DIVIDE BY 32
0	1	1	DIVIDE BY 64
1	1	1	DIVIDE BY 128

TABLE 9
VCO ENABLING

VCOEN	***VCO***
0	DISABLED
1	ENABLE

TABLE 10
OUTPUT DRIVERS CONTROL

OUTDR		***BUFFERS PRO-GRAMMED***
B0	***B1***	
0	0	TRISTATE
1	0	1 BUFFER
0	1	2 BUFFERS
1	1	3 BUFFERS

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CIRCUIT DESCRIPTION

Using a 250KHZ clock (**FR**) from a 10 Mhz crystal oscillator as stable reference frequency, the PLL51C04 synthesizes 4 independent clocks OUT1 OUT2 OUT3 OUT4, each with frequencies ranging from 0 Mhz to 200 Mhz.

Refering to Block Diagram on page 1, the device contains essentially 4 major blocks :

10 MHZ Crystal Oscillator (see Table 3 & Timing diagram Figure 5)

generates a 250 Khz reference frequency FR through a divider by 40. The oscillator can be disabled by bit REF0 from 22 BIT SHIFT REGISTER. It has a built-in feedback resistor.

10MHZ Oscillator & OUT10MHZ Controller :

(Table 3, 4 & Timing diagram figure 5 & 8)

enable / disable Oscillator and 10 Mhz output. The control bits REF0 and REF1 are for control of crystal Oscillator and 10 MHZ Output respectively. These bits are from 22 BIT SHIFT REGISTER.

22 BIT SHIFT REGISTER (Table 1)

for serial loading of Programming Data Word. The whole 22 bits are shifted into this register and 17 bits transfered into individual CLOCK GENERATOR latches by EN signal. Remaining bits are used for selection of the chip, clock generators or control of crystal oscillator.

ADDRESS DECODER (Table 5)

selection of 1 of 4 Clock Generators for programming. Inputs to this block are CSH, EN from external pins and CSS, VCOSEL bits from 22 BIT SHIFT REGISTER. If CSS=CSH the EN pulse will create a LOADEN signal for 1 of 4 internal 17 bits latch of 4 CLOCK GENERATORS, VCOSEL bits select which one of 4 CLOCK GENERATORs to be programmed.

4 CLOCK GENERATORS :

synthesize clock frequencies using reference FR (250Khz) and control word VCOF. FR from DIVIDER_BY_40, VCOF from 22 BIT SHIFT REGISTER.

Each of these 4 Clock Generators has 4 building blocks : 17 BITS REGISTER, VCO FREQUENCY GENERATOR, SLEEP MODE CONTROLLER, OUTPUT FREQUENCY DIVIDER and OUTPUT DRIVER CONTROLLER.

17 BITS REGISTER (Table 1)

this register contains all control signals for each individual CLOCK GENERATOR. It is composed of VCOF (9 bits), SM (2 bits), OUTDIV (3 bits), VCOEN (1 bit) and OUTDR (2 bits).

VCO FREQUENCY GENERATOR (Table 6)

synthesizes a VCO Frequency from FR and VCOF bits. FR (Reference Frequency) is a fixed 250 Khz from 10 Mhz crsytal. VCOF is a binary number from the 22 BIT SHIFT REGISTER.

The VCO Frequency is

$$F_{VCO} = VCOF*4*250Khz = VCOF \text{ in Mhz}$$

SLEEP MODE CONTROLLER (Table 7)

selects its Output Frequency from 3 different clock sources : VCO Frequency, internal Reference Frequency FR and External Frequency EXT. The selection is controlled by SM bits from 22 BIT SHIFT REGISTER.

OUTPUT FREQUENCY DIVIDER (Table 8)

the Output Clock from SLEEP MODE CONTROLLER is divided by a programmable divider inside this block, the Division Ratio is controlled by OUTDIV bits from 22 BIT SHIFT REGISTER.

OUTPUT DRIVER CONTROLLER (Table 10)

this block controls the drivers for the clock output. The control bits are OUTDR from 22 BIT SHIFT REGISTER.

FUNCTIONAL DESCRIPTION

- The chip will function only if signal TEST is *low*. TEST=*high* is reserved for Factory testing. This TEST pin has internal pull-down resistor.
- All the functions of PLL51C04 are completely controllable from the 22 BIT SHIFT REGISTER where all the control words are loaded in serially.

I. POWER UP

Master Reset : RB (pin 17)

The signal RB has a built-in Pull-up resistor of 50kohm. It can be used as master reset of the chip or as Power-On reset.

An external capacitor C_{PR} is needed for it to perform as Power-On reset signal.

RB=0 (at Power-On)

(see Timing diagram figure 1 & 2 on page 8)

- The 10 MHZ crystal oscillator is *enable* and stabilized 10ms after VDD reaches 3 V.
- Output OUT10Mhz (pin 28) is active and has 10 Mhz coming out after crystal oscillator is stable.
- All outputs OUT1 OUT2 OUT3 OUT4 are static at either High level or Tristate.

RB=0 (at any time except Power-On)

- The 10 Mhz crystal oscillator is *enable*. The time required for it to stabilized depends on its state before the reset. If it was disabled the oscillation will be stabilized 1ms after the reset.
- Output OUT10MHZ (pin 28) is active and has 10 Mhz output clock.
- All outputs OUT1 OUT2 OUT3 OUT4 are static at either *high* level or *tristate*. They will have a tristate output only if they were tristate before the reset.

RB=1 from 0

- after RB goes high for a TID time, all outputs OUT2, OUT3 and OUT4 assume a static high level from a previous high level or Tristate. These outputs will stay static until programmed to function differently (see Figure 1 & 2 on page 8).
- If DFOUT1 signal (pin 27) is *low*, OUT1 will assume a static High level from a previous High level or Tristate. If this signal is *high*, OUT1 will have 10 Mhz clock coming out after a Enable Period T_{EN}.

$$32.15\ \mu s \leq T_{EN} \leq 36.15\ \mu s$$

An important application for this DFOUT1 signal is to hardwired DFOUT1 to VDD so after Power-on the output OUT1 can have automatically 10 Mhz output clock without any need for programming. OUT1 can be programmed later on as all other outputs.

Note : it is imperative that when RB goes High, the EN signal (pin 13) be kept to LOW. This is to prevent erronous loading of undefined content of the 22 Bit Shift Register into internal registers of Clock Generators. It means that ***during the Power-On, care must be taken to insure that EN stays statically LOW.***

II. PROGRAMMING :

A. PROGRAMMING OF THE DATA WORD

The programming of the chip consists of 2 steps:

1. Shifting serially 22 bit data word into the 22 bit shift register by using signals DATA (pin15) and CLOCK (pin 16) (see TABLE 1 for definition of the Programming Data Word and Timing diagram figure 3 on page 9)
2. Tranfering the content of the shift register to individual register of 1 of 4 CLOCK GENERATORS by pulsing the signal EN *high* then *low*. When EN is *high*, it transfers the content of 22 Bit Shift Regiter into internal Register of 1 of 4 Clock generators. When *low*, it latches the DATA in the register (see Timing Diagram 3). The VCOSEL (bit 18 and bit 17) will determine which CLOCK GENERATOR to be programmed.

B. SEQUENCE OF EVENTS

(see Timing diagram figure 3 on page 9)

The sequence of events, in general, will be as described below, except when mentioned otherwise.

After the rising edge of EN the Clock Generator which is programmed will have its output OUTx (x=1,2,3,4)

- goes *high* at the next rising edge of the output OUTx (at current frequency).
- stay *high* for a Enable Period T_{EN} of

$$32\ \mu s + 1.5\ TN \leq T_{EN} \leq 36\ \mu s + 1.5\ TN$$

TN being the period of the New clock frequency.

- After this period the output will resume with the new mode of operation together with new frequency. The output OUTx will be active starting with the Falling edge of the new clock frequency.

C. DEFINITION OF DATA WORD

The DATA WORD consists of 22 bits from Bit0 to Bit21.

Bit21 : **CSS** (see TABLE 2)

This **C**hip **S**elect by **S**oftware is to be compared with signal CSH (pin 14) for DATA WORD transfer.

The CSH (Chip Select Hardware) allows 2 PLL51C04 to be used on same system without additional external decoding.

Only one PLL51C04 with CSH=CSS can be programmed at a time.

When CSS=CSH the EN pulse will create LOADEN1 or LOADEN2 or LOADEN3 or LOADEN4 pulse.

Which LOADEN is active will depend on value of VCOSEL.

This LOADEN pulse will transfer the bit VCOF OUTDIV SM VCOEN OUTDR (bits D16...to..D0) to 17 bit internal register of CLOCK GENERATOR.

At Power-On (RB=0) CSS is unknown.

Bit20: **REF0** (see TABLE 3)

This bit controls the 10 MHZ crystal oscillator. REF0=1 will enable the oscillator.

At Power-On (RB=0) REF0=1, Oscillator is enable.

REF0 =0 : (Timing diagram figure 5)

Crystal oscillator will be disabled after all outputs OUT1 OUT2 OUT3 OUT4 were set in idle state High.

After these outputs go in idle state High they will stay High until after REF0 is programmed to a 1.

All internal registers of CLOCK GENERATORS maintain their previous value (*no loading*) meaning that all bits from D16 to D0 are not loaded in any internal registers.

The idle state of crystal oscillator is *low*, the output OUT10Mhz is also *low*.

REF0=1 after it was 0 : (figure 6)

A *high* on EN will trigger the oscillator, it will oscillate after a Start-Up Time (see T_{STW} AC specifications).

The programming of this bit to value 1 always tranfers the 22 BIT Shift Register content to internal register of 1 of 4 clock generators. Therefore previous content of this register chosen by VCOSEL bits has to be shifted into the SHIFT REGISTER if one desires to keep previous output frequency.

OUT10MHZ output may have glitch but other Outputs will resume glitch-free.

Bit19 : **REF1** (see TABLE 1 & 4 & figure 8)

When CSS=CSH and REF1=0, a *high* on EN signal will disable OUT10MHZ output (*tristate*) immediately. A REF1=1 will enable this output in the same manner.

The programming of this bit always transfers Shift Register content into internal register of 1 of 4 Clock generators unless it is combined in the same loading with the bit REF0=0. In this case the register content of all 4 clock generators remain intact but their output will be affected as described above.

At Power-On (RB=0) REF1=1, OUT10MHZ is enable.

Bit18, Bit17 : **VCOSEL** (G0 G1) (Table 1 & 5)

These 2 bits determine which Clock Generator will be programmed. The one chosen by VCOSEL will latch the 17 bits of Data from 22 Bit Shift Register into its internal register.

At Power-On these bits are unknown.

Bit16...Bit8 : **VCOF** (Table 1 & 6)

These 9 bits control Frequency of VCO from VCO Frequency Generator. The frequency of VCO is programmable following the formula :

$$F_{VCO} = \text{VCOF Mhz}$$

The minimum increment step of VCO frequency is 1 Mhz.

- Valid VCOF number is from 1 to 200 (in binary). The device has programmability up to 511 but it is reserved for future use only. This version only supports up to 200 Mhz.
- VCOF=0 is not valid

At Power=On (RB=0) VCOF is unknown.

RB=1 after RB=0 VCOF has value of 10 (decimal)

Bit7, Bit6, Bit5 : **OUTDIV** (Table 1 & 8)

- These 3 bits control the division ratio of divider that slows down the frequency of the source selected by Sleep Mode Circuit.
- At Power-on (RB=0) OUTDIV is unknown

RB=1 after RB=0 OUTDIV=000, meaning no division.

Bit4 Bit3 : **SM** (Table 1 & 7)

This 2 bits select which sources of frequency will go to the Output OUTx. There are 3 sources : VCO frequency, Internal Reference Frequency FR (250 Khz) and External frequency EXTx from external pins.

The choice has following restrictions :

- Crystal Oscillator must be active when FR is selected. (Active means toggling).
- EXTx must be active when selected.
- First and second CLOCK GENERATOR (outputs OUT1 and OUT2) can not select External source.
- Selection of VCO source is permissible even when VCO is OFF.
- At Power=On (RB=0) SM is unknown.

  RB=1 after RB=0, SM has value of 00 (binary). It means that VCO source is selected.

Bit2 : **VCOEN** (Table 1 & 9)

(see Timing diagram Figure 1, 2, 3 & 4)

- This bit control internal VCO of Clock Generator. When VCOEN=0 the VCO is OFF independently of the number VCOF loaded in the register.
- This bit is maskable by signal DFOUT1 from pin 27 for First Clock Generator (OUT1). A *high* on this pin will keep VCO of this Output always *on*.
- At Power-On (RB=0) VCOEN is unknown.
- RB=1 after RB=0, VCOEN=0 meaning all internal VCOs are disable after Power-On. They will stay disabled until enabled by programming.
- For output OUT1, a DFOUT1=1 (pin 27) will override this VCOEN bit. It will enable the internal VCO of this Clock Generator always on even at Power-On reset.

Bit1 Bit0 : **OUTDR** (Table 1 & 10)

(see Timing diagram figure 7)

These 2 bits control the drivers of OUT1 OUT2 OUT3 OUT3. Each output has 3 independent drivers that can be enabled/disabled by OUTDR.

By controlling the drivers one can optimize the rise and fall times of each output depending on the system requirement.

- At Power-on (RB=0) OUTDR is unknown

  RB=1 after RB=0 OUTDR=1 (one buffer on)

PIN DESCRIPTION

XIN (pin 1) : crystal Oscillator input. An external reference frequency or an external crystal can be connected. The input frequency must be 10 Mhz. Some other frequencies centered around 10 Mhz can be used, in this case please consult our Marketing or Engineering Department for further details.

XOUT (pin 2) : crystal Oscillator output. This output is inverted from XIN. A feedback resistor of nominal 1 Megaohm is connected between XIN and XOUT. When the oscillator is disabled, Feedback resitor is disconnected; XIN goes *high* and XOUT goes to *low*.

VCOIN1,VCOIN2,VCOIN3,VCOIN4 (Pins 10,9,6,5) : these pins are inputs directly to internal VCOs. Normally they are connected to filter capacitors of 0.1 μF. Since these inputs directly control VCOs,one can apply an analog signal to control directly VCO frequencies from outside, bypassing altogether the internal Phase-locked loop. On PC board, one should isolate these inputs from any active signals, noise from these signals may affect the stability of VCOs output frequencies.

DFOUT1 (pin 27) : this pin control VCO of the first Clock Generator. A *high* on this pin will always enable the VCO, bypassing the bit VCOEN from programming word, even when master reset RB=0 or at Power-on.

EN (pin 13) : a positive pulse on this input will, at the same time, deactivate the affected output while loading its register. At Power-On it should be kept Low to avoid erronous programming of Clock Generators.This pin has a pull-down of 50 kohm.

CSH (pin 14) : this chip select signal allows the use of 2 PLL51C04 on the same board without any additional address decoder. One chip can be programmed at a time, only the one with CSH matches CSS bit in the 22 BIT SHIFT REGISTER will receive the loading of Programming Data.

DATA (pin 15) : data input of 22 BIT SHIFT REGISTER.

CLOCK (pin 16) : clock input of the 22 BIT SHIFT REGISTER.

RB (pin 17) : master reset. This signal resets the whole chip at the same time makes the crystal oscillator and OUT10MHZ (pin 28) active if they were not already. When reset is active OUT1 OUT2 OUT3 OUT4 go to *high* and stay *high* until reprogrammed after reset goes away. OUT1 will assume 10 Mhz clock frequency if DFOUT1 is *high*. This pin has 50Kohm pull-up resitor. It can be used as power-on reset.

TEST (pin 20) : to be tied to VSS or left open for the chip to function. It has built-in 50 Kohm pull-down resistor. TEST= *high* is reserved for factory testing.

EXT3 (pin 24) : the clock frequency applied to this pin can be selected by Sleep Mode Controller as a source of frequency . Then it can be divided down further as the case for VCO frequency before it goes out to OUT3.

EXT4 (pin 26) : as EXT3 but applied to OUT4.

OUT10MHZ (pin 28) : is a buffered output of XIN.

OUT1 (pin 18) : output of First Clock Generator. Its sources of frequency are VCO Frequency and internal reference frequency FR of 250 Khz. Its rise and fall times are controllable from programming. At Power-On, this pin is automatically programmed to 10 Mhz if DFOUT1 (pin 27) is tied to High level

OUT2 (pin 19) : output of Second Clock Generator. Its sources of frequencies are from VCO frequency and internal reference frequency of 250 Khz. Its rise and fall times are controllable from programming. At Power-On, it has a static *high* and its VCO clock Generator is *off* until programmed.

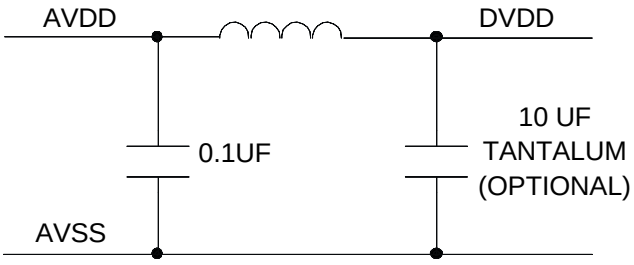
OUT3 (pin 23) : output of Third Clock Generator. Its sources of frequencies are from VCO frequency, internal reference frequency of 250 Khz and arbitrary external frequency EXT3. Its rise and fall times are controllable from programming. At Power-On, it has a static *high* and its VCO clock generator is *off* until programmed.

OUT4 (pin 25) : output of Fourth Clock Generator. Its sources of frequencies are from VCO frequency, internal reference frequency of 250 Khz and arbitrary external frequency EXT4. Its rise and fall times are controllable from programming. At Power-On, it has a static *high* and its VCO clock Generator is *off* until programmed.

POWER SUPPLY DECOUPLING

In order to minimize noise jitter on outputs, the following rules should be implemented :

- All VDD power supply pins must have decoupling capacitors.
- The distance between these capacitors and power pin should be minimized .
- These capacitors should have low lead inductance, so ceramic capacitors are recommended. A value of 0.1µF is sufficient.
- For critical applications, analog power supply pin AVDD should be isolated from digital power supply plane. A single ferrite bead between Digital power plane and Analog power pin is sufficient. (see schematics)



TIMING DIAGRAMS

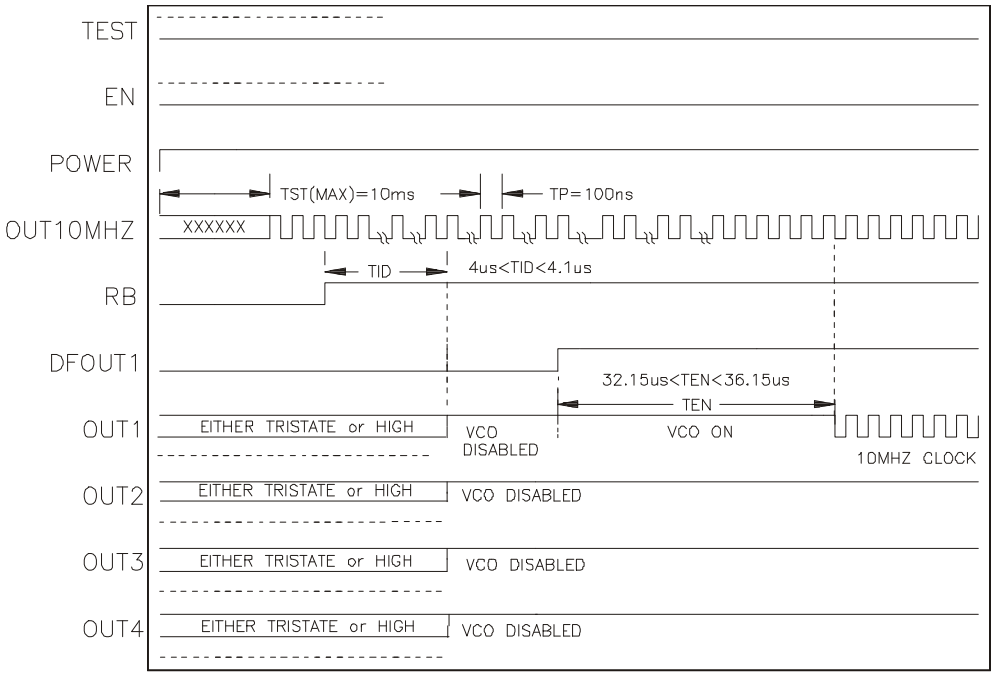


FIGURE 1 : POWER ON / RESET SEQUENCE
WITH DFOUT1 HIGH AFTER TID

All VCO are disabled by RB and stay so until programmed to different value.
After Reset, OUT1 assumes 10MHZ clock if DFOUT1 goes High.

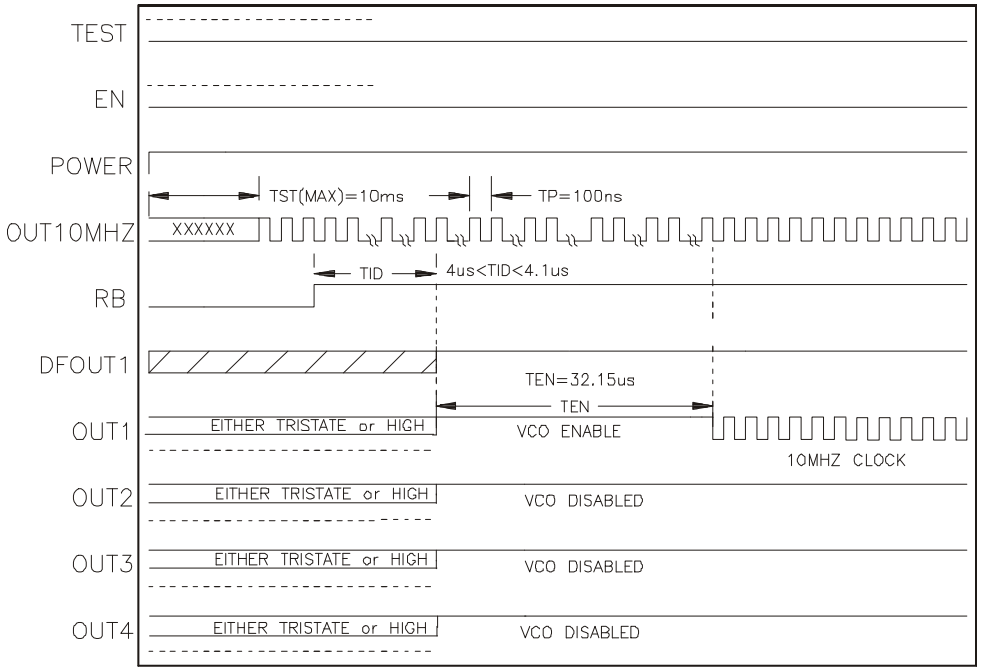


FIGURE 2 : POWER ON / RESET SEQUENCE
WITH DFOUT1 HIGH BEFORE TID

This diagram applies to the case that DFOUT1 goes High any time before time TID
Clock Frequency of OUT1 will be programmed to 10MHZ automatically after Reset.

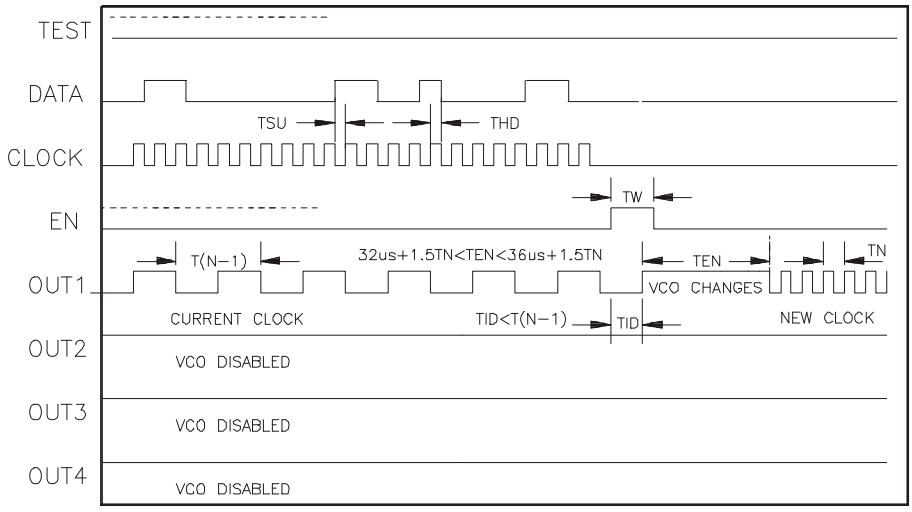


FIGURE 3 : SWITCHING FREQUENCY / MODE OF OPERATION

For simplicity, this diagram only shows events for OUT1, the same apply for OUT2 OUT3 OUT4.
When VCO is programmed to be disabled, OUT1 will go High at TID and remain High after.

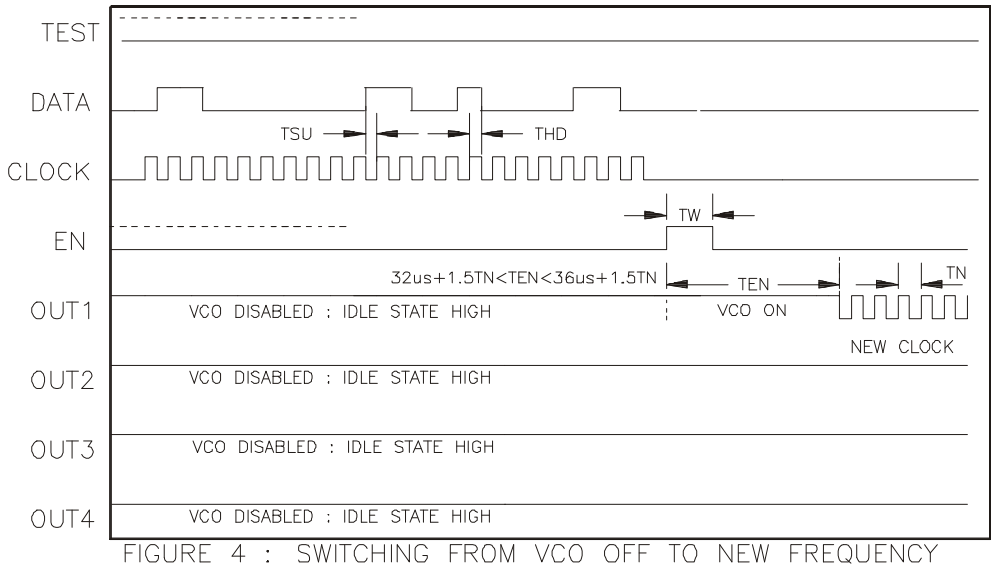


FIGURE 4 : SWITCHING FROM VCO OFF TO NEW FREQUENCY

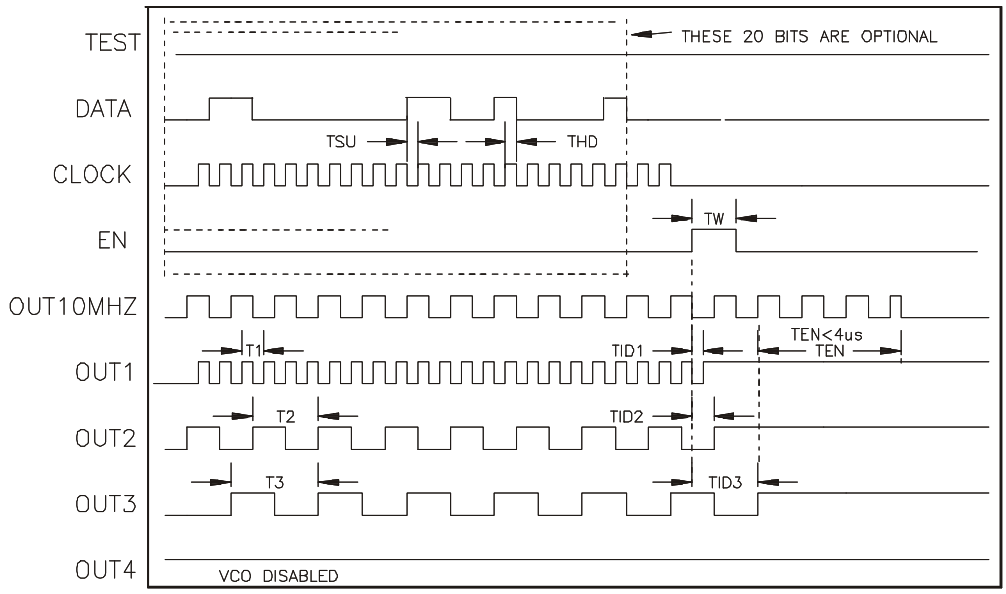


FIGURE 5 : PROGRAMMING TO DISABLE 10MHZ OSCILLATOR

Only 2 bits REF0 and CSS are necessary for this operation.
Bit REF1 programming for control of OUT10MHZ output BUFFER is allowed with this operation, but all other bits are irrelevant since they are not processed by the machine (all internal register of Clock Generators are kept intact)
This operation will make all outputs go to Static High

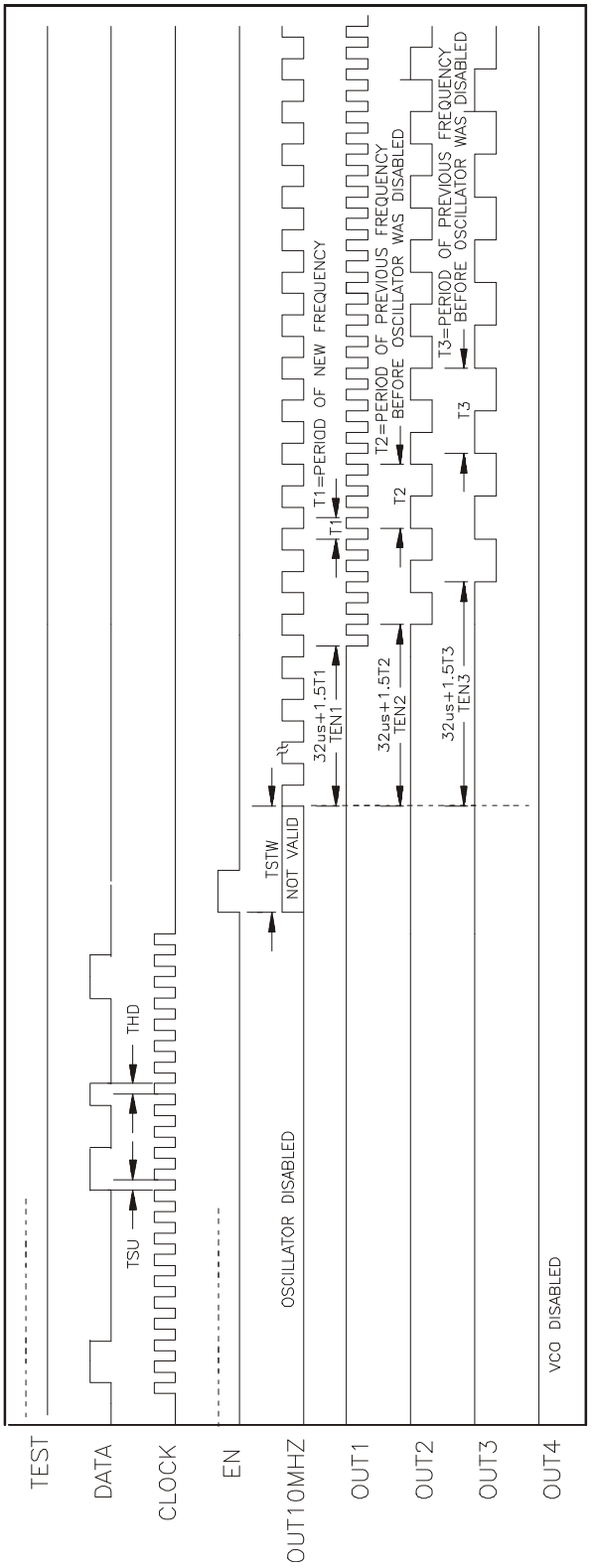


FIGURE 6 : 10MHZ OSCILLATOR FROM DISABLED TO ENABLED COMBINED WITH NEW FREQUENCY FOR OUT1

One of the 4 Clock Generators must be programmed with this operation, its new frequency and mode of operation could be the same as the one that exists before Oscillator is disabled. All other Clock Geneators will resume with previous frequency/mode of operations.

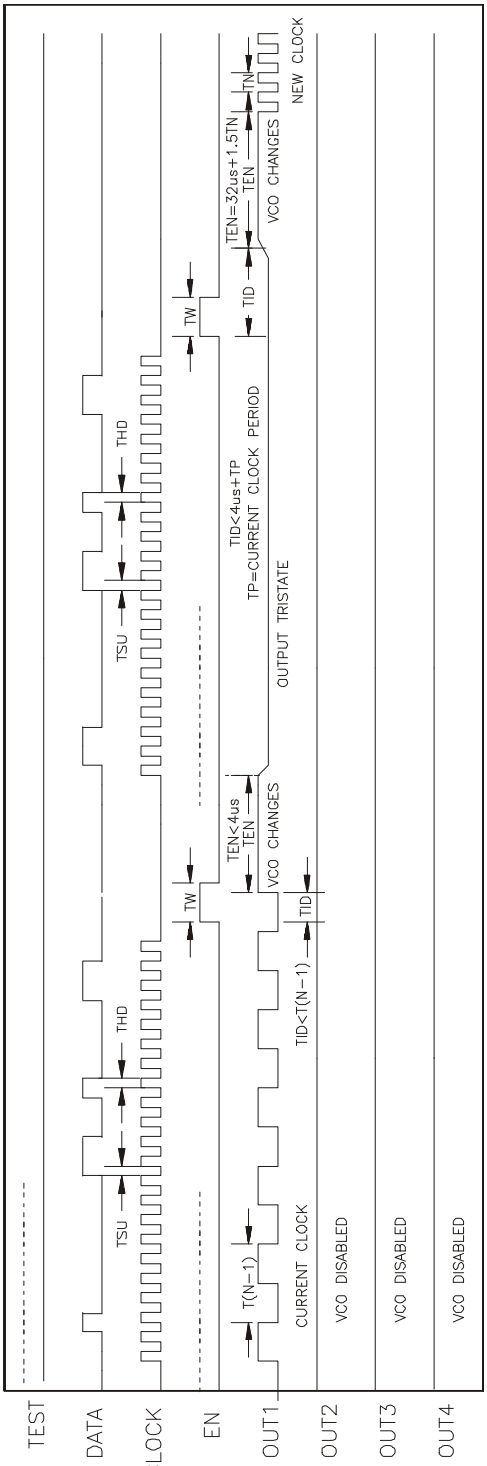


FIGURE 7 : PROGRAMMING OUTPUT BUFFERS ON / OFF

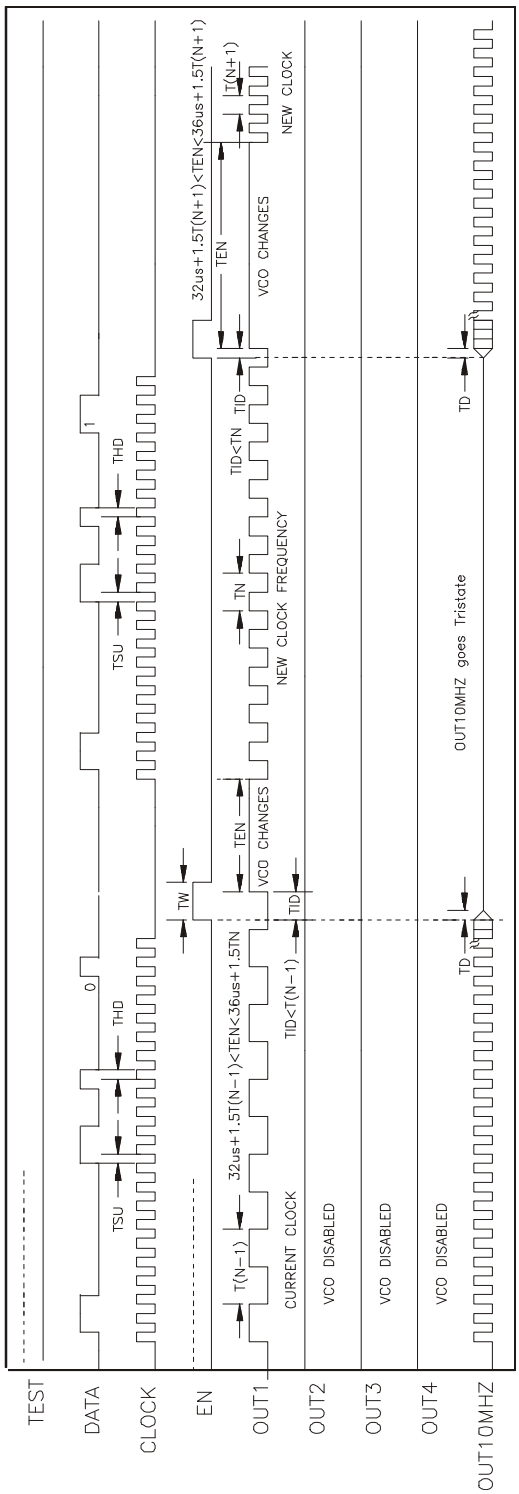


FIGURE 8 : PROGRAMMING OUT10MHZ BUFFER ON / OFF
The control of OUT10MHZ buffer will affect one of 4 clock generators
Output Buffer of OUT10MHZ will be disabled/enabled immediately after EN

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	VDD	Both DVDD and AVDD	4.5	5	5.5	V
Operating Temperature	T_a		0	25	85	^oC
Dynamic Current	I_{DYN}	VDD=5.5V Ta=0^{o}C XIN@10MHZ OUT10MHZ@10MHZ All VCO programmed for 200MHZ All OUTDIV for 128 division ratio All output loads = 50PF		20	40	mA
Static Current	I_{STATIC}	All VCO and Crystal Oscillator are OFF EN=LOW TEST=LOW RB=HIGH		1	10	µA
Input High Voltage	V_{IH}	All Inputs except XIN	2			V
		XIN	3.5			V
Input Low Voltage	V_{IL}	All Inputs except XIN			0.8	V
		XIN			1.5	V
Input High Current	I_{IH}	All Inputs except TEST, EN and (XIN @ REF0=0)	-1			
		XIN @ REF0=0	-10	-5	-2	µA
		TEST, EN (with Pull-Down resistor)	-200	-100	-50	µA
Input Low Current	I_{IL}	All Inputs Except RB and (XIN @ REF0=0)			1	µA
		RB (Pull-Up resistor)	50	100	200	µA
		XIN @ REF0=0	2	5	10	µA
Output High Current	I_{OH}	OUT1 OUT2 OUT3 OUT4 @ V_{OH}=2.4V	8,16,24			mA
		OUT10MHZ @V_{OH}=2.4V	8			mA
		XOUT @ V_{OH}=2.4V	4			mA
		VCOIN1 VCOIN2 VCOIN3 VCOIN4 @V_{OH}=2.4	20	50	100	µA
Output Low Current	I_{OL}	OUT1 OUT2 OUT3 OUT4 @ V_{OL}=0.4V	8,16,24			mA
		OUT10MHZ @V_{OL}=0.4V	8			mA
		XOUT @ V_{OL}=0.4V	4			mA
		VCOIN1 VCOIN2 VCOIN3 VCOIN4 @V_{OL}=0.4	4	8	20	µA
Tristate Leakage	I_Z	All outputs except XOUT	-1		1	µA
Input Impedance	R_I	XIN	500	1000	2000	kΩ
	C_I		2	4	6	PF
Output Impedance	R_O	XOUT	500	1000	2000	Ω
		VCOIN1 VCOIN2 VCOIN3 VCOIN4	20000	50000	100000	kΩ
		OUT1 OUT2 OUT3 OUT4 @8mA	15	25	50	Ω
	C_O	VCOIN1 VCOIN2 VCOIN3 VCOIN4 XOUT	2	4	6	PF
		OUT1 OUT2 OUT3 OUT4 @8mA	4	6	8	PF

MAXIMUM RATINGS

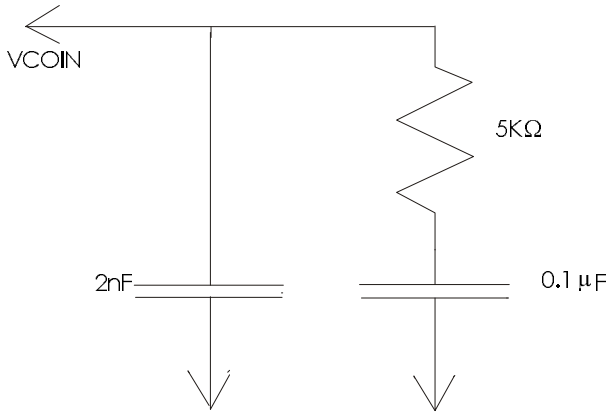
SUPPLY VOLTAGE	VSS-0.5V TO 7V
INPUT VOLTAGE	VSS-0.5V TO VDD+0.5V
ESD VOLTAGE	2000V
POWER DISSIPATION	1W
STORAGE TEMPERATURE	-65°C TO 150°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings may cause permanent damage to the device

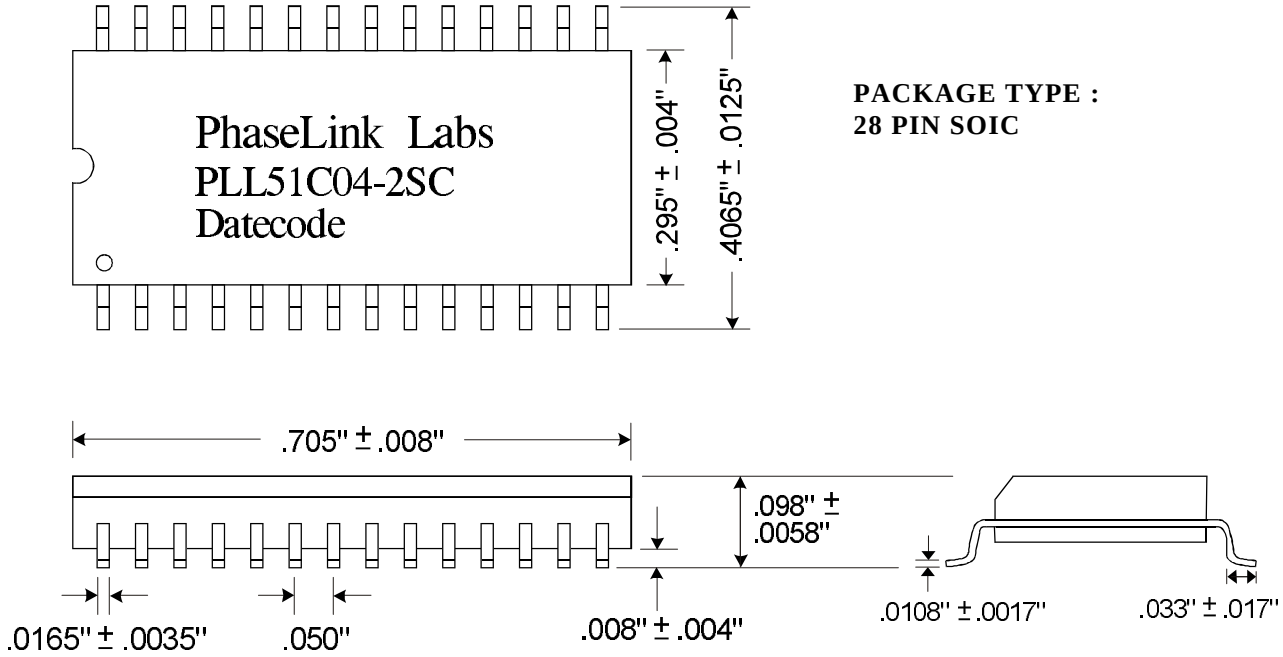
AC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start-Up Time 10MHZ Crystal Oscillator @VDD=5V Fundamental Serie resonance	T_{ST}	@ Power-On			10	mS
	T_{STW}	After oscillator was disabled (warm start up)			1	
Crystal specifications	R_S	Serie resistance	15	20	30	Ω
	C_S	Serie capacitor	3	4	5	PF
	L_S	Serie Inductance	12	14	17	mH
	C_P	Parallel Capacitance	0.015	0.018	0.022	PF
	O_C	Crystal Orientation		AT		
Frequency Accuracy	F_A	relative accuracy of output frequency versus programmed frequency.	same accuracy as crystal used			ppm
Jitter (one sigma)	T_{JS}	Jitter noise on OUT1 OUT2 OUT3 OUT4			150	pS
Absolute jitter	T_{JA}	Jitter noise on OUT1 OUT2 OUT3 OUT4			1	nS
Duty Cycle	D_C	OUT10MHZ	40/60	45/55	60/40	%
		OUT1 OUT2 OUT3 OUT4	48/52	50/50	52/48	%
Delay	T_D	From XIN to OUT10MHZ output,	1	2	5	nS
Skew Time	T_{SK}	Between OUT1 OUT2 OUT3 OUT4 when they have same clock frequencies.	-1	0.5	1	nS
Iddle Time	T_{ID}	From Rising Edge of EN to OUTx goes High	3nS		1 OUTx CLOCK	
Enable Time	T_{EN}	From Time OUTx goes High after Rising Edge of EN to Time OUTx has valid clock output with New Frequency and New Mode of Operation	32		36	µS
Setup Time	T_{SU}	From DATA to CLOCK	5			nS
Hold Time	T_{HD}	From CLOCK to DATA	5			nS

FILTER FOR GRAPHICS APPLICATIONS

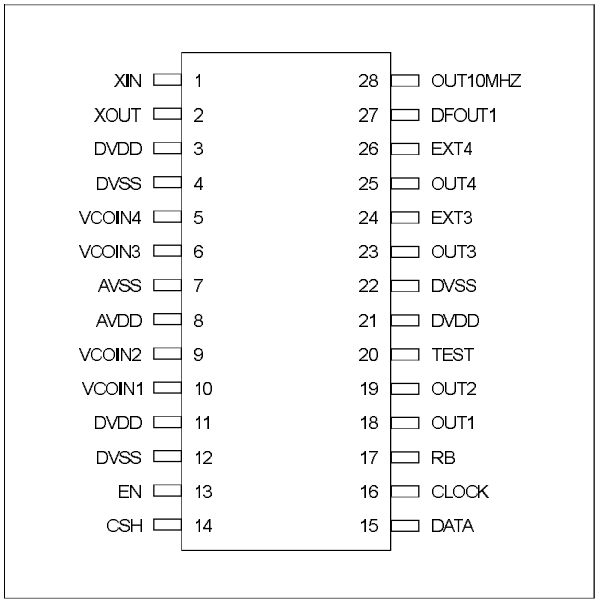


PACKAGE DRAWING



PACKAGE TYPE :
28 PIN SOIC

PIN CONFIGURATION



ORDERING INFORMATION

For part ordering, please contact our Sales Department :

45437 WARM SPRINGS Blvd.
Fremont, California 94539 U.S.A.
Tel :510-492-0990 Fax :510-492-0991
Or Our Website : www.phaselink.com

The order number for this device is a combination of the following :
device number, speed option, package type and operating temperature range.

PLL51C04- 2 S C

PART NUMBER

SPEED OPTION
2=200MHZ 4=400MHZ

TEMPERATURE
C=COMMERCIAL M=MILITARY I=INDUSTRIAL

PACKAGE
S=SOIC J=PLCC