

Fast CMOS 3.3V 8-Bit Registered Transceiver
Product Features

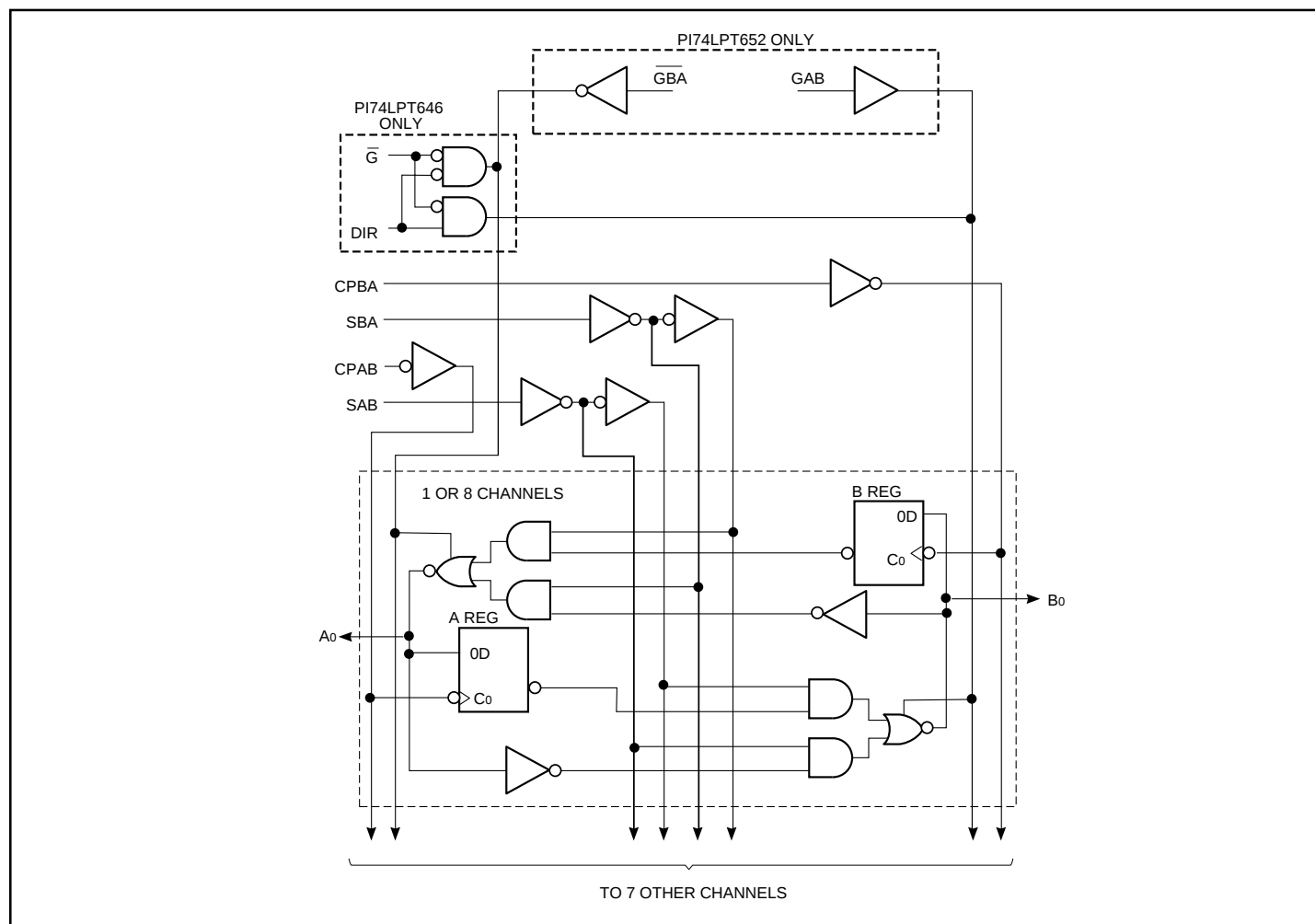
- Functionally compatible with FCT3, LVT, and 74 series 646 and 652 families of products
- Tri-State outputs
- 5V Tolerant inputs and outputs
- 2.0V-3.6V V_{CC} supply operation
- Balanced sink and source output drives (24 mA)
- Low ground bounce outputs
- Supports live insertion
- ESD Protection exceeds 2000V, Human Body Model
200V, Machine Model
- Packages available:
 - 24-pin 209-mil wide plastic SSOP (H)
 - 24-pin 173-mil wide plastic TSSOP (L)
 - 24-pin 150-mil wide plastic QSOP (Q)
 - 24-pin 300-mil wide plastic SOIC (S)

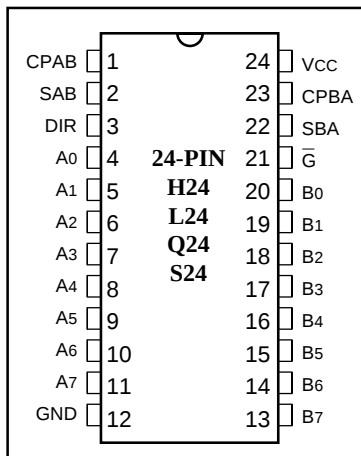
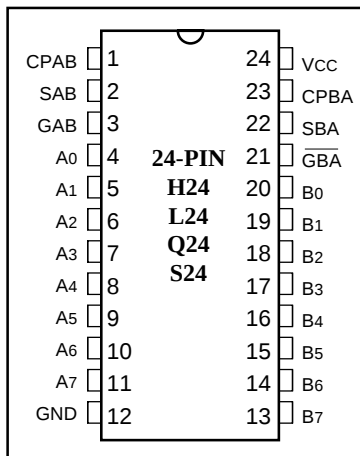
Product Description

Pericom Semiconductor's PI74LCX series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LCX646 and PI74LCX652 are designed with a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The PI74LCX652 utilizes GAB and GBA signals to control the transceiver functions. The PI74LCX646 uses the enable control ($\bar{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74LCX646 and PI74LCX652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram


PI74LCX646
Product Pin Configuration

PI74LCX652
Product Pin Configuration

Product Pin Description

Pin Name	Description
A0-A7	Data Register A Inputs Data Register B Outputs
B0-B7	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source SelectInputs
DIR, $\overline{G}$	Output Enable Inputs (LCX646)
GAB, $\overline{GBA}$	Output Enable Inputs (LCX652)
GND	Ground
VCC	Power

PI74LCX646 Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

PI74LCX652 Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾
Store A in Both Registers	H	H	↑	↑	X ⁽²⁾	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input
Store B in Both Registers	L	L	↑	↑	X	X ⁽²⁾	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

Notes:

- The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.
H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ..	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V _I	Input Voltage		0	5.5	
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}	
		TRI-State	0	5.5	
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V-3.6V	—	±24	mA
		V _{CC} = 2.7V	—	±12	
T _A	Free-Air Operating Temperature		–40	+85	°C
Δt/ΔV	Input Edge Rate	V = 0.8V-2.0V, V _{CC} = 3.0V	0	10	ns/V

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7\text{-}3.6$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	
		$V_{CC} = 2.7$	$I_{OH} = -12\text{mA}$	2.2	—	—	
		$V_{CC} = 3.0$	$I_{OH} = -18\text{mA}$	2.4	—	—	
			$I_{OH} = -24\text{mA}$	2.2	—	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.7\text{-}3.6$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	
		$V_{CC} = 2.7$	$I_{OL} = 12\text{mA}$	—	—	0.4	
		$V_{CC} = 3.0$	$I_{OL} = 16\text{mA}$	—	—	0.4	
			$I_{OL} = 24\text{mA}$	—	—	0.55	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5\text{V}$	$V_{CC} = 2.7\text{-}3.6$	—	—	± 5	μA
I_{OZ}	Tri-State Output Leakage	$0 \leq V_O \leq 5.5\text{V}$ $V_I = V_{IH}$ or V_{IL}	$V_{CC} = 2.7\text{-}3.6$	—	—	± 5	
I_{OFF}	Power Down Disable	$V_{CC} = 0\text{V}, V_{IN}$ or $V_{OUT} \leq 5.5\text{V}$		—	—	10	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} = \text{GND}$ or V_{CC}	—	0.1	10	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6\text{V}^{(3)}$	—	—	500	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.

Capacitance

Parameters	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0\text{V}$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V}$ or V_{CC}	8	
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V}$ or $V_{CC}, F = 10\text{ MHz}$	25	

Switching Characteristics over Operating Range

Parameters	Description	Conditions	V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		Units
			Min.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency	C _L = 50pF R _L = 500Ω	150	—	—	—	MHz
t _{PHL} t _{PLH}	Propagation Delay Bus to Bus		1.5	7.0	1.5	8.0	ns
t _{PHL} t _{PLH}	Propagation Delay Clock to Bus		1.5	8.5	1.5	9.5	
t _{PHL} t _{PLH}	Propagation Delay Select to Bus		1.5	8.5	1.5	9.5	
t _{PZL} t _{PZH}	Output Enable Time		1.5	8.5	1.5	9.5	
t _{PLZ} t _{PHZ}	Output Disable Time		1.5	8.5	1.5	9.5	
T _S	Setup Time		2.5	—	2.5	—	
T _H	Hold Time		1.5	—	1.5	—	
T _W	Pulse Width		3.3	—	3.3	—	
tsk(0)	Output to Output Skew ⁽¹⁾		—	1.0	—	—	

Note:

1. Skew between any two outputs, of the same package, switching in the same direction.

Dynamic Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions ⁽¹⁾	Typical	Units
V _{OLP}	Dynamic LOW Peak Voltage	V _{CC} = 3.3V, C _L = 50pF V _{IH} = 3.3V, V _{IL} = 0V	0.8	V
V _{OLV}	Dynamic LOW Valley Voltage	V _{CC} = 3.3V, C _L = 50pF V _{IH} = 3.3V, V _{IL} = 0V	0.8	V

Note:

1. Measured with n–1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.