PI74LCX543

Fast CMOS 3.3V 8-Bit Latched Transceiver

Product Features

- Functionally compatible with FCT3, LVT, and 74 series 543 families of products
- Tri-State outputs
- 5V Tolerant inputs and outputs
- 2.0V-3.6V V_{CC} supply operation
- Balanced sink and source output drives (24 mA)
- Low ground bounce outputs
- Supports live insertion
- ESD Protection exceeds 2000V, Human Body Model
  200V, Machine Model
- Packages available:
  - –24-pin 209-mil wide plastic SSOP (H)
  - –24-pin 173-mil wide plastic TSSOP (L)
  - –24-pin 150-mil wide plastic QSOP (Q)
  - –24-pin 300-mil wide plastic SOIC (S)

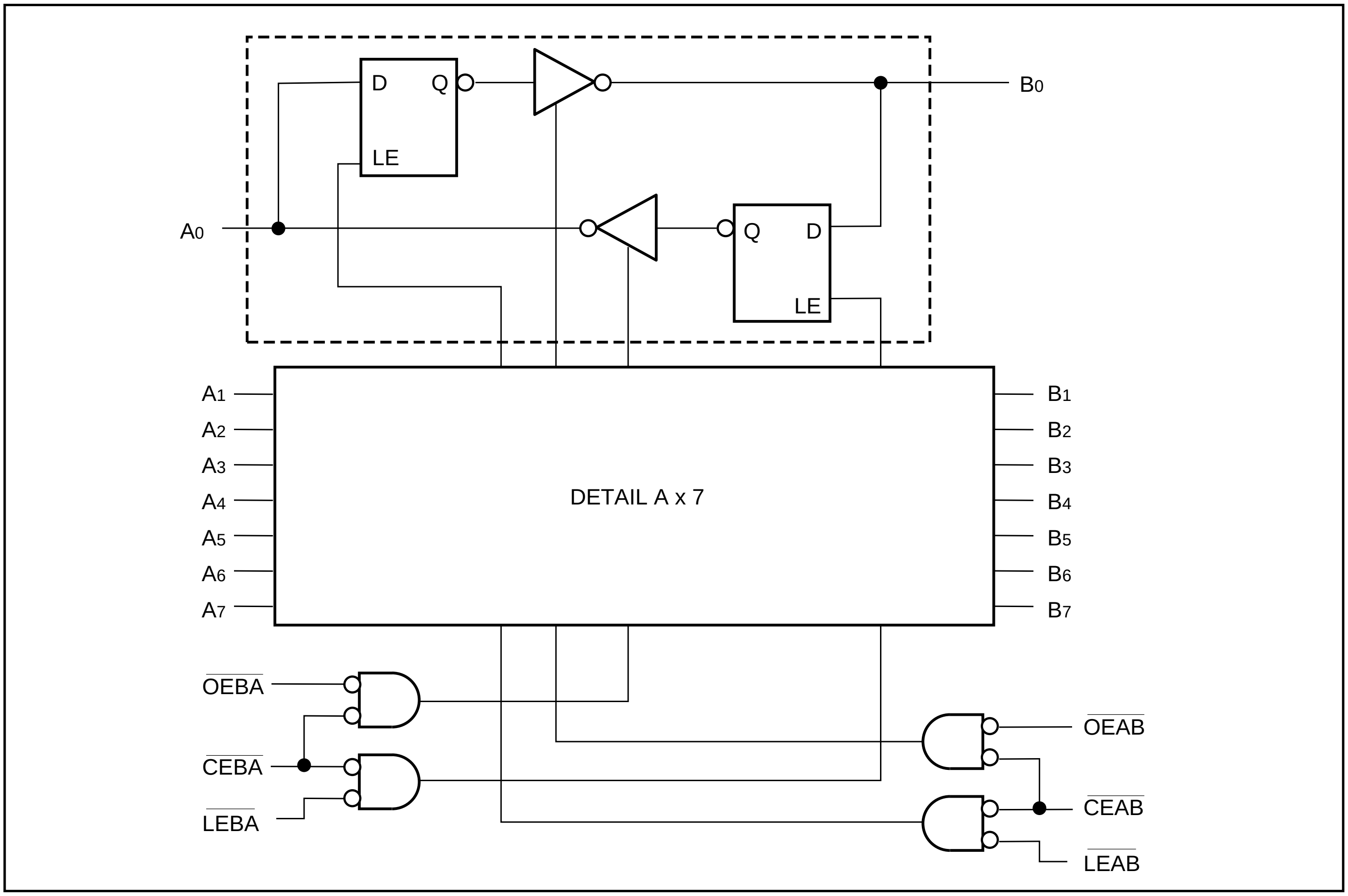
Product Description

Pericom Semiconductor's PI74LCX series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

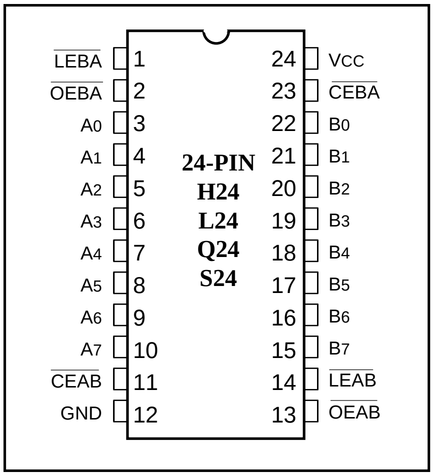
The PI74LCX543 is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{CEAB}}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Truth Table. With $\overline{\text{CEAB}}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{\text{CEAB}}$, $\overline{\text{LEAB}}$, and $\overline{\text{OEAB}}$ inputs.

The PI74LCX543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{\mathrm{OEAB}}$	A-to-B Output Enable Input (Active LOW)
$\overline{\mathrm{OEBA}}$	B-to-A Output Enable Input (Active LOW)
$\overline{\mathrm{CEAB}}$	A-to-B Enable Input (Active LOW)
$\overline{\mathrm{CEBA}}$	B-to-A Enable Input (Active LOW)
$\overline{\mathrm{LEAB}}$	A-to-B Latch Enable Input (Active LOW)
$\overline{\mathrm{LEBA}}$	B-to-A Latch Enable Input (Active LOW)
A0-A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0-B7	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
V_{CC}	Power

Truth Table (Non-Inverting)(1,2)
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{\mathrm{CEAB}}$	**$\overline{\mathrm{LEAB}}$**	**$\overline{\mathrm{OEAB}}$**	**A-to-B**	**B0–B7**
H	X	X	Storing	High-Z
X	H	X	Storing	—
X	X	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

1. *Before $\overline{\mathrm{LEAB}}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don’t Care or Irrevelant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{\mathrm{CEBA}}$, $\overline{\mathrm{LEBA}}$, and $\overline{\mathrm{OEBA}}$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	
		TRI-State	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V-3.6V	—	±24	mA
		V_{CC} = 2.7V	—	±12	
T_A	Free-Air Operating Temperature		–40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate	V = 0.8V-2.0V, V_{CC} = 3.0V	0	10	ns/V

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions(1)		Min.	Typ(2)	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7-3.6	I_{OH} = –0.1mA	V_{CC}-0.2	—	—	
		V_{CC} = 2.7	I_{OH} = –12mA	2.2	—	—	
		V_{CC} = 3.0	I_{OH} = –18mA	2.4	—	—	
			I_{OH} = –24mA	2.2	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.7-3.6	I_{OL} = 0.1mA	—	—	0.2	
		V_{CC} = 2.7	I_{OL} = 12mA	—	—	0.4	
		V_{CC} = 3.0	I_{OL} = 16mA	—	—	0.4	
			I_{OL} = 24mA	—	—	0.55	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	Vcc = 2.7-3.6	—	—	±5	µA
I_{OZ}	Tri-State Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	V_{CC} = 2.7-3.6	—	—	±5	
I_{OFF}	Power Down Disable	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 5.5V		—	—	10	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}	—	0.1	10	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V(3)	—	—	500	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.

Capacitance

Parameters	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	

Switching Characteristics over Operating Range

Parameters	Description	Conditions	V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V		Units
			Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	C_L = 50 pF R_L = 500Ω	1.5	7.0	1.5	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{LEBA}}$ to A_N, $\overline{\text{LEAB}}$ to B_N		1.5	8.5	1.5	9.5	
t_{PZH} t_{PZL}	Output Enable Time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A_N or B_N $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to A_N or B_N		1.5	9.0	1.5	10.0	
t_{PZH} t_{PZL}	Output Disable Time[3] $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A_N or B_N $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to A_N or B_N		1.5	7.0	1.5	7.5	
t_{SU}	Setup Time, HIGH or LOW A_N or B_N to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$		2.5	—	2.5	—	
t_H	Hold Time, HIGH or LOW A_N or B_N to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$		1.5	—	1.5	—	
t_W	$\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$ Pulse Width LOW[3]		3.3	—	3.3	—	
tsk(o)	Output Skew[1]		—	1.0	—	—	

Note:

1. Skew between any two outputs, of the same package, switching in the same direction.

Dynamic Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions[1]	Typ.	Units
V_{OLP}	Dynamic LOW Peak Voltage	V_{CC} = 3.3V, C_L = 50pF V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
V_{OLV}	Dynamic LOW Valley Voltage	V_{CC} = 3.3V, C_L = 50pF V_{IH} = 3.3V, V_{IL} = 0V	0.8	V

Note:

1. Measured with n–1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.