



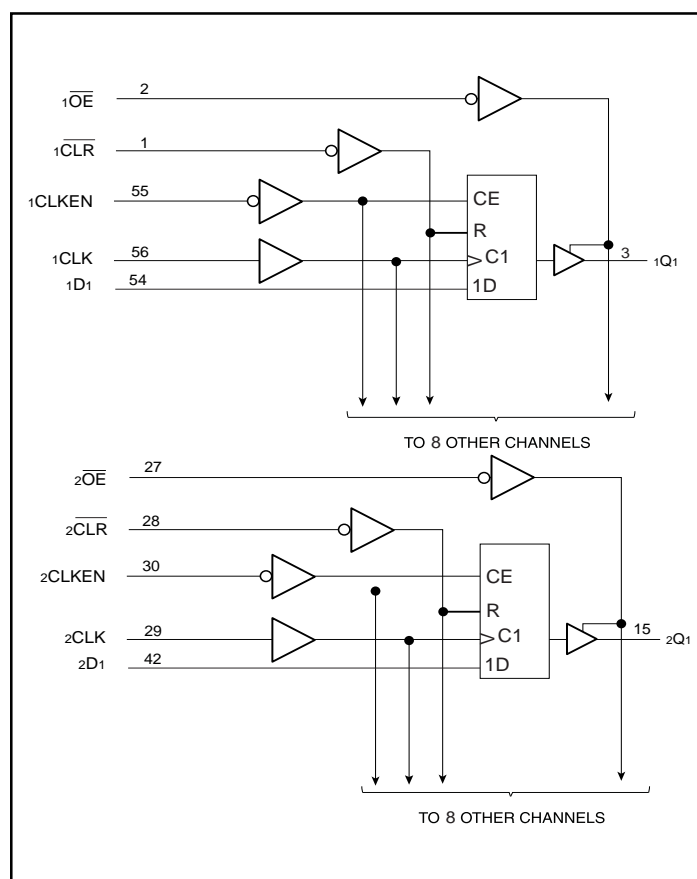
PI74AVC+16823

2.5V 18-Bit Bus Interface Flip-Flop with 3-State Outputs

Product Features

- PI74AVC+16823 is designed for low voltage operation, $V_{CC} = 1.65V$ to $3.6V$
- True $\pm 24mA$ Balanced Drive @ $3.3V$
- I_{OFF} supports partial power-down operation
- $3.6V$ I/O Tolerant Inputs and Outputs
- All outputs contain noise reduction circuitry reducing noise without speed degradation
- Industrial operation at $-40^{\circ}C$ to $+85^{\circ}C$
- Available Packages:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (K)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The 18-bit PI74AVC+16823 bus-interface flip-flop is designed for $1.65V$ to $3.6V$ V_{CC} operation. It features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The device can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the Clock Enable (CLKEN) input LOW, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN HIGH disables the clock buffer, thus latching the outputs. Taking the Clear (CLR) input LOW causes the Q outputs to go LOW independently of the clock.

A buffered Output Enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The Output Enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW)
\overline{CLR}	Clear Input (Active LOW)
\overline{CLKEN}	Clock Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
VCC	Power

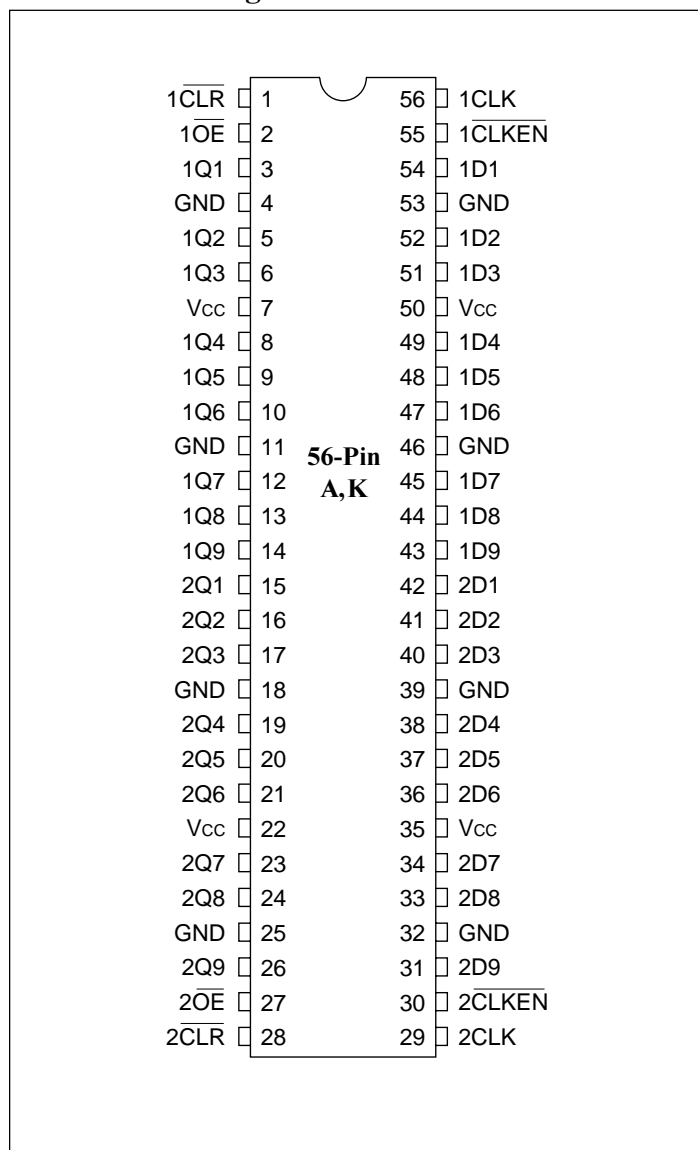
Truth Table⁽¹⁾

Inputs					Output
\overline{OE}	\overline{CLR}	\overline{CLKEN}	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q ₀
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

Note:

1. H = High Signal Level
- L = Low Signal Level
- X = Irrelevant
- Z = High Impedance
- ↑ = LOW-to-HIGH Transition

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC}	−0.5V to +4.6V
Input voltage range, V_I	−0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	−0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	−0.5V to $V_{CC} + 0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	−50mA
Output clamp current, I_{OK} ($V_O < 0$)	−50mA
Continuous output current, I_O	±50mA
Continuous current through each V_{CC} or GND	±100mA
Package thermal impedance, $\theta_{JA}^{(3)}$: package A	64°C/W
package K	48°C/W
Storage Temperature range, T_{stg}	−65°C to 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	$V_{CC} = 1.2V$	V_{CC}		
	$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3V$ to $2.7V$	1.7		
	$V_{CC} = 3V$ to $3.6V$	2		
V_{IL} Low-level Input Voltage	$V_{CC} = 1.2V$		Gnd	
	$V_{CC} = 1.65V$ to $1.95V$		$0.35 \times V_{CC}$	
	$V_{CC} = 2.3V$ to $2.7V$		0.7	
	$V_{CC} = 3V$ to $3.6V$		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	$V_{CC} = 1.65V$ to $1.95V$		−6	mA
	$V_{CC} = 2.3V$ to $2.7V$		−12	
	$V_{CC} = 3V$ to $3.6V$		−24	
I_{OL} Low-level output current	$V_{CC} = 1.65V$ to $1.95V$		6	
	$V_{CC} = 2.3V$ to $2.7V$		12	
	$V_{CC} = 3V$ to $3.6V$		24	
$\Delta t \Delta v$ Input transition rise or fall rate	$V_{CC} = 1.65V$ to $3.6V$		5	ns/V
T_A Operating free-air temperature		−40	85	°C

Notes:

1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$)

Parameters		Test Conditions ⁽¹⁾	V _{CC}	Min.	Typ.	Max.	Units
V _{OH}		I _{OH} = −100μA	1.65V to 3.6V	V _{CC} −0.2V			V
		I _{OH} = −6mA V _{IH} = 1.07V	1.65V	1.2			
		I _{OH} = −12mA V _{IH} = 1.7V	2.3V	1.75			
		I _{OH} = −24mA V _{IH} = 2V	3V	2.0			
V _{OL}		I _{OL} = 100μA	1.65V to 3.6V			0.2	
		I _{OL} = 6mA V _{IH} = 0.57V	1.65V			0.45	
		I _{OL} = 12mA V _{IH} = 0.7V	2.3V			0.55	
		I _{OL} = 24mA V _{IH} = 0.8V	3V			0.8	
I _I	Control Inputs	V _I = V _{CC} or GND	3.6V			±2.5	μA
I _{OFF}		V _I or V _O = 3.6V	0			±10	
I _{OZ}		V _I = V _{CC} or GND	3.6V			±10	
I _{CC}		V _O = V _{CC} or GND I _O = 0	3.6V			40	
C _I	Control Inputs	V _I = V _{CC} or GND	2.5V		4		pF
			3.3V		4		
	Data Inputs		2.5V		6		
			3.3V		6		
C _O	Outputs	V _O = V _{CC} or GND	2.5V		8		
			3.3V		8		

Note: Typical values are measured at $T_A = 25^{\circ}\text{C}$.

Timing Requirements over recommended operating free-air temperature range
(unless otherwise noted, see Figures 1 thru 4)

		$V_{CC} = 1.2V$		$V_{CC} = 1.5V \pm 0.1V$		$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{clock} Clock Frequency							150		180		180	MHz
t_w Pulse duration	\overline{CLR} Low					3.4		3.0		3.0		ns
	\overline{CLK} high or low					3.4		3.0		3.0		
t_{su} Setup time	CLR Low					0.8		0.1		0.6		
	Data Low					0.8		1.0		1.2		
	Data High					1.2		1.0		0.8		
	\overline{CLKEN} Low					2.0		1.6		1.2		
t_h Hold time	Data Low					0.4		0.4		0.4		
	Data High					0.6		0.6		0.6		
	\overline{CLKEN} Low					0.4		0.4		0.4		

Switching Characteristics over recommended operating free-air temperature range
(unless otherwise noted, see Figures 1 thru 4)

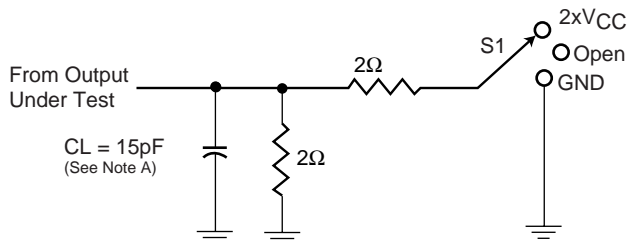
Parameter	From (Input)	To (Output)	V _{CC} = 1.2V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{max}							150		180		180		MHz
t _{pd}	CLK	Q						4.0		2.7		2.3	ns
	$\overline{\text{CLR}}$						3.7		2.8		2.4		
t _{en}	$\overline{\text{OE}}$							3.9		2.7		2.3	
t _{dis}								3.5		2.5		2.7	

Operating Characteristics, T_A=25°C

Parameters		Test Conditions	$V_{CC} = 1.8V \pm 0.15V$	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Units
			Typical	Typical	Typical	
C _{pd} Power Dissipation Capacitance	Outputs Enabled	C _L = 0pF, f = 10 MHz	25	30	37	pF
	Outputs Disabled		10	12	18	

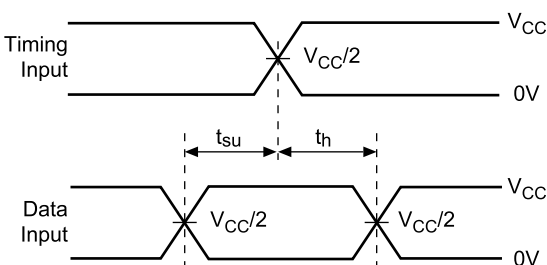
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2V \text{ AND } 1.5V \pm 0.1V$

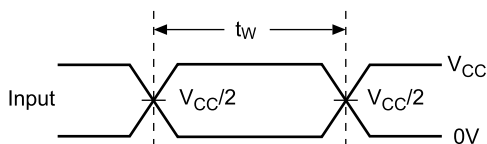


Load Circuit

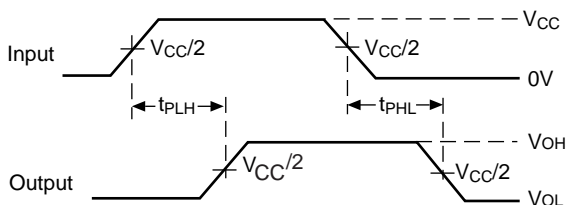
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



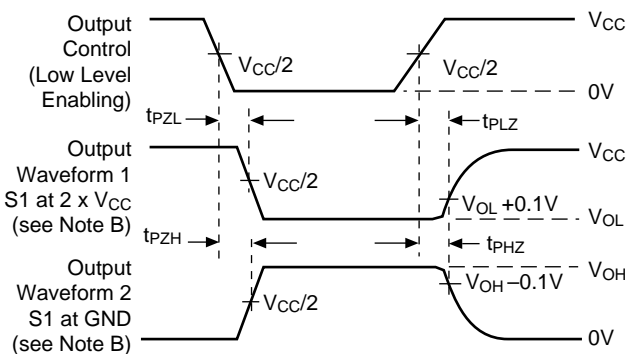
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

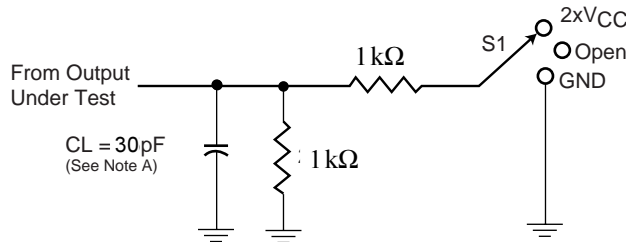
Figure 1. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0ns$, $t_F \leq 2.0ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

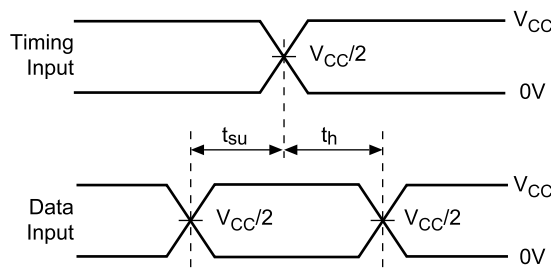
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8V \pm 0.15V$$

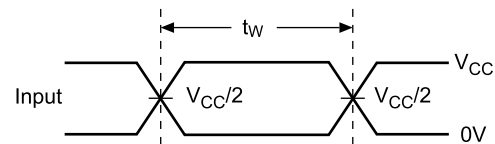


Load Circuit

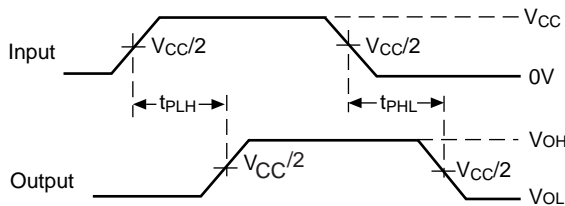
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x VCC GND



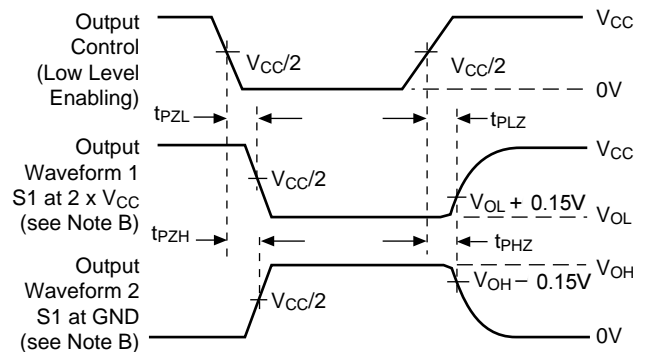
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

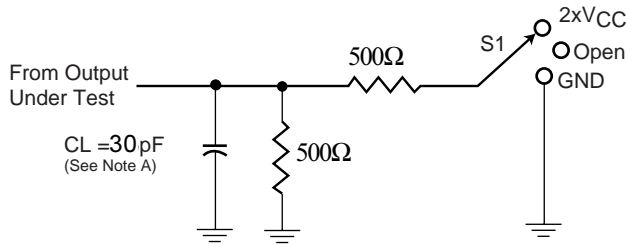
Figure2. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0ns$, $t_F \leq 2.0ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

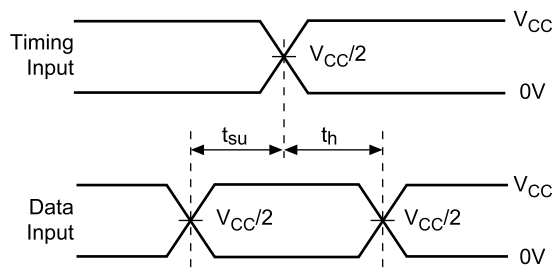
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5V \pm 0.2V$$

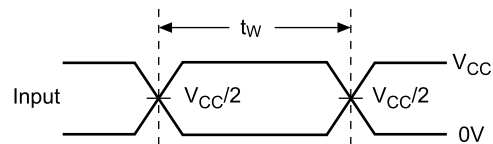


Load Circuit

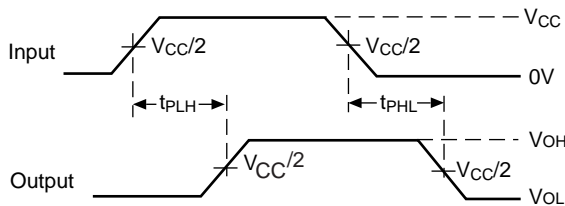
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



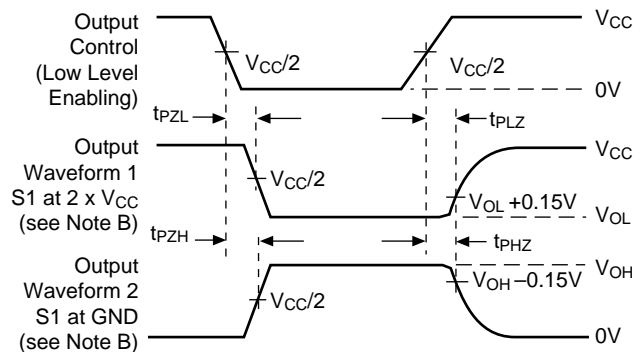
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

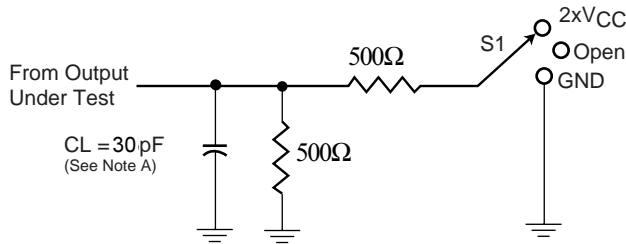
Figure3. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2.0ns, t_f ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

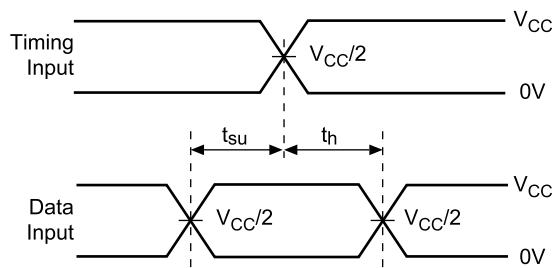
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3V \pm 0.3V$$

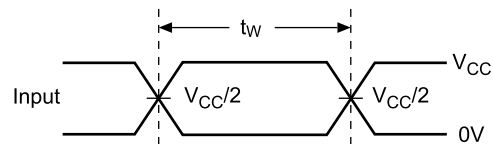


Load Circuit

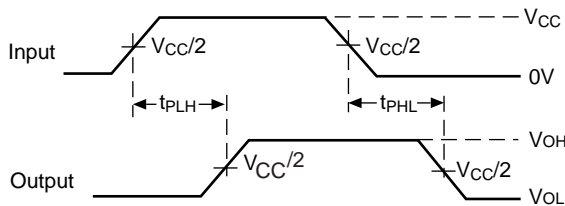
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



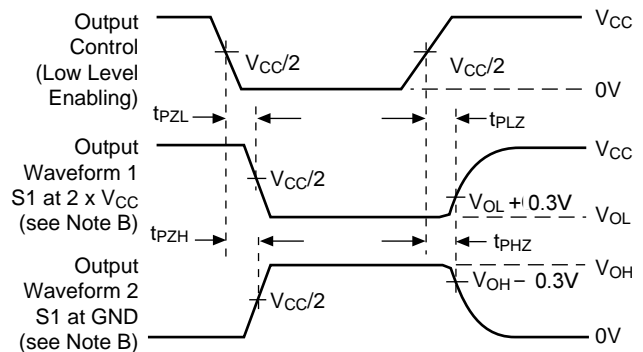
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2.0ns, t_f ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

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