



PI74AVC+16721

2.5V 20-Bit Flip-Flop with 3-State Outputs

Product Features

- PI74AVC+16721 is designed for low voltage operation, $V_{CC} = 1.65V$ to $3.6V$
- True $\pm 24mA$ Balanced Drive @ $3.3V$
- I_{OFF} supports partial power-down operation
- $3.6V$ I/O Tolerant inputs and outputs
- All outputs contain noise reduction circuitry reducing noise without speed degradation
- Industrial operation at $-40^{\circ}C$ to $+85^{\circ}C$
- Available Packages:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (TSSOP) (K)

Product Description

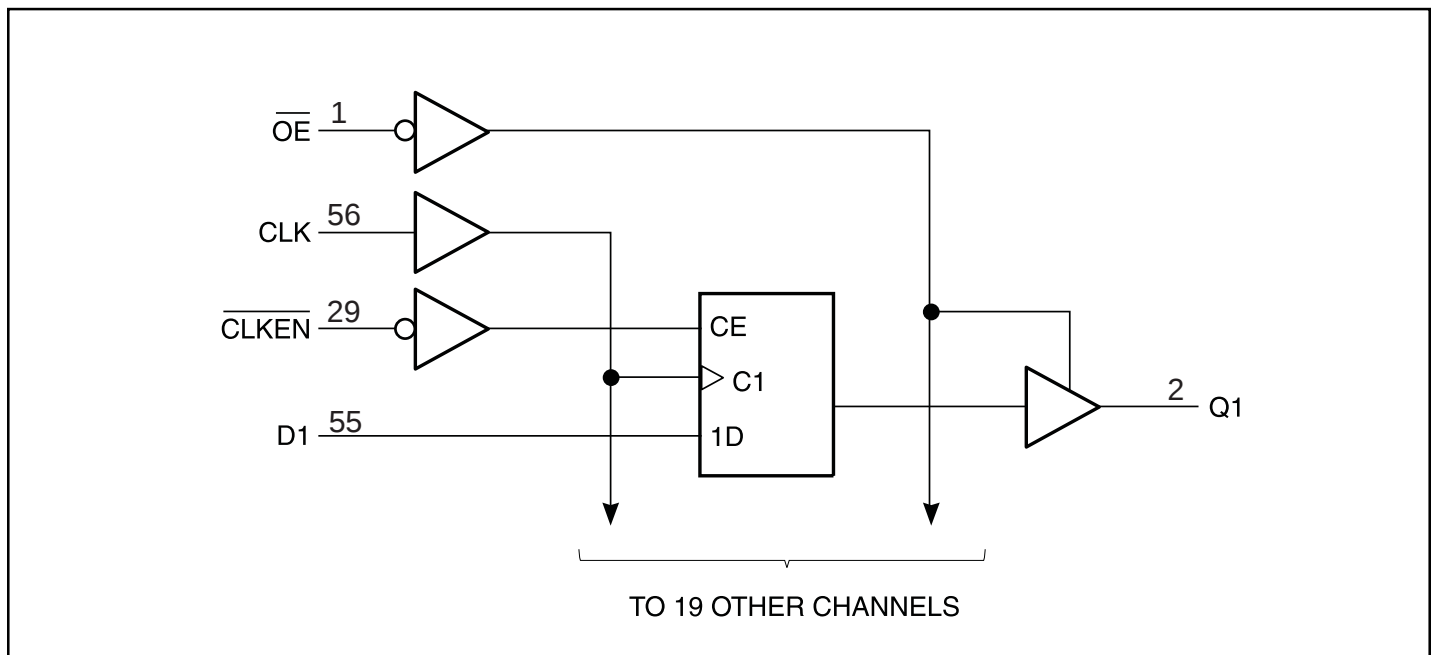
Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16721 is a 20-bit flip-flop with 3-state outputs designed specifically for $1.65V$ to $3.6V$ V_{CC} operation. The device is designed with edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of clock (CLK) input, the device provides true data at the Q outputs, provided that the clock-enable (CLKEN) input is LOW. If CLKEN is HIGH, no data is stored.

A buffered output-enable ($\overline{OE}$) input can be used to place the 20 outputs in either a normal logic state (HIGH or LOW level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capacity to drive bus lines without the need for interface or pullup components. $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{CLKEN}$	Clock Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
VCC	Power

Product Pin Configuration

$\overline{OE}$	1	56	CLK
Q1	2	55	D1
Q2	3	54	D2
GND	4	53	GND
Q3	5	52	D3
Q4	6	51	D4
VCC	7	50	VCC
Q5	8	49	D5
Q6	9	48	D6
Q7	10	47	D7
GND	11	46	GND
Q8	12	45	D8
Q9	13	44	D9
Q10	14	43	D10
Q11	15	42	D11
Q12	16	41	D12
Q13	17	40	D13
GND	18	39	GND
Q14	19	38	D14
Q15	20	37	D15
Q16	21	36	D16
VCC	22	35	VCC
Q17	23	34	D17
Q18	24	33	D18
GND	25	32	GND
Q19	26	31	D19
Q20	27	30	D20
NC	28	29	$\overline{CLKEN}$

Truth Table⁽¹⁾

Inputs				Outputs
$\overline{OE}$	$\overline{CLKEN}$	CLK	Dx	Qx
L	H	X	X	Q ₀
L	L	–	H	H
L	L	–	L	L
L	L	L or H	X	Q ₀
H	X	X	X	Z

Notes:

- H = High Signal Level
L = Low Signal Level
X = Don't Care or Irrelevant
Z = High Impedance
↑ = LOW-to-HIGH Transition

Maximum Ratings above which the useful life may be impaired. (For user guidelines, not tested.)

Supply voltage range, V_{CC}	–0.5V to +4.6V
Input voltage range, V_I	–0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	–0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	–0.5V to $V_{CC}+0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	–50mA
Output clamp current, I_{OK} ($V_O < 0$)	–50mA
Continuous output current, I_O	±50mA
Continuous current through each V_{CC} or GND	±100mA
Package thermal impedance, $\theta_{JA}^{(3)}$: package A	64°C/W
package K	48°C/W
Storage Temperature range, T_{stg}	–65°C to 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	$V_{CC} = 1.2V$	V_{CC}		
	$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3V$ to $2.7V$	1.7		
	$V_{CC} = 3V$ to $3.6V$	2		
V_{IL} Low-level Input Voltage	$V_{CC} = 1.2V$		Gnd	
	$V_{CC} = 1.65V$ to $1.95V$		$0.35 \times V_{CC}$	
	$V_{CC} = 2.3V$ to $2.7V$		0.7	
	$V_{CC} = 3V$ to $3.6V$		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	$V_{CC} = 1.65V$ to $1.95V$		– 6	mA
	$V_{CC} = 2.3V$ to $2.7V$		– 12	
	$V_{CC} = 3V$ to $3.6V$		– 24	
I_{OL} Low-level output current	$V_{CC} = 1.65V$ to $1.95V$		6	
	$V_{CC} = 2.3V$ to $2.7V$		12	
	$V_{CC} = 3V$ to $3.6V$		24	
$\Delta t_{\Delta v}$ Input transition rise or fall rate	$V_{CC} = 1.65V$ to $3.6V$		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Notes:

1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics over the Operating Range ($T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$)

Parameters		Test Conditions ⁽¹⁾	V _{CC}	Min.	Typ.	Max.	Units
V _{OH}		I _{OH} = −100μA	1.65V to 3.6V	V _{CC} −0.2V			V
		I _{OH} = −6mA V _{IH} = 1.07V	1.65V	1.2			
		I _{OH} = −12mA V _{IH} = 1.7V	2.3V	1.75			
		I _{OH} = −24mA V _{IH} = 2V	3V	2.0			
V _{OL}		I _{OL} = 100μA	1.65V to 3.6V			0.2	
		I _{OL} = 6mA V _{IH} = 0.57V	1.65V			0.45	
		I _{OL} = 12mA V _{IH} = 0.7V	2.3V			0.55	
		I _{OL} = 24mA V _{IH} = 0.8V	3V			0.8	
I _I	Control Inputs	V _I = V _{CC} or GND	3.6V			±2.5	μA
I _{OFF}		V _I or V _O = 3.6V	0			±10	
I _{OZ}		V _I = V _{CC} or GND	3.6V			±10	
I _{CC}		V _O = V _{CC} or GND I _O = 0	3.6V			40	
C _I	Control Inputs	V _I = V _{CC} or GND	2.5V		4		pF
			3.3V		4		
	Data Inputs		2.5V		6		
			3.3V		6		
C _O	Outputs	V _O = V _{CC} or GND	2.5V		8		
			3.3V		8		

Note: Typical values are measured at $T_A = 25^{\circ}\text{C}$.

Timing Requirements over recommended operating free-air temperature range

(unless otherwise noted, see Figures 1 thru 4)

		V _{CC} = 1.2 V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{clock} Clock Frequency							150		180		180	MHz
t _w Pulse duration, CLK high or low						6.0		3.0		3.0		ns
t _{su} Setup time	Data before CLK↑					5.7		3.5		2.4		
	$\overline{\text{CLKEN}}$ before CLK↑					2.2		2.0		1.6		
t _h Hold time	Data after CLK↑					0		0		0		
	$\overline{\text{CLKEN}}$ after CLK↑					1.2		1.0		1.0		

Switching Characteristics over recommended operating free-air temperature range

(unless otherwise noted, see Figures 1 thru 4)

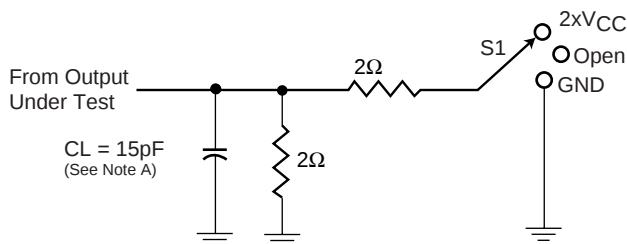
Parameters	From (Input)	To (Output)	V _{CC} = 1.2V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{max}							150		180		180		MHz
t _{pd}	CLK	Q						4.3		3.0		2.6	ns
t _{en}	$\overline{\text{OE}}$	Q						5.8		4.8		4.0	
t _{dis}	$\overline{\text{OE}}$	Q						4.8		3.6		3.4	

Operating Characteristics, T_A = 25°C

Parameters		Test Conditions	V _{CC} = 1.8V ±0.15V	V _{CC} = 2.5V ±0.2V	V _{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C _L = 0pF, f = 10 MHz	65	80	100	pF
	Outputs Disabled		40	50	75	

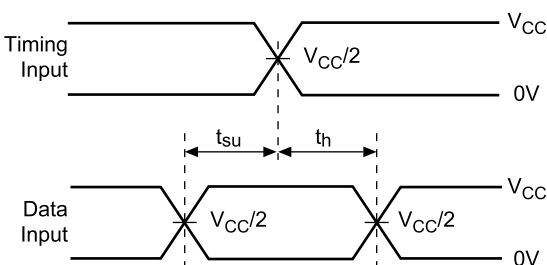
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2V \text{ and } 1.5V \pm 0.1V$

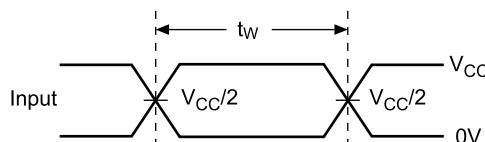


Load Circuit

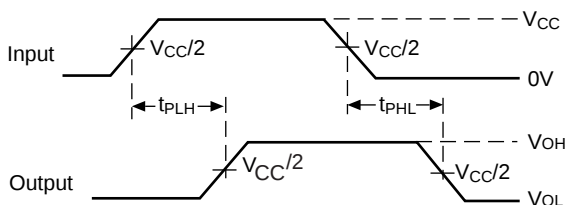
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



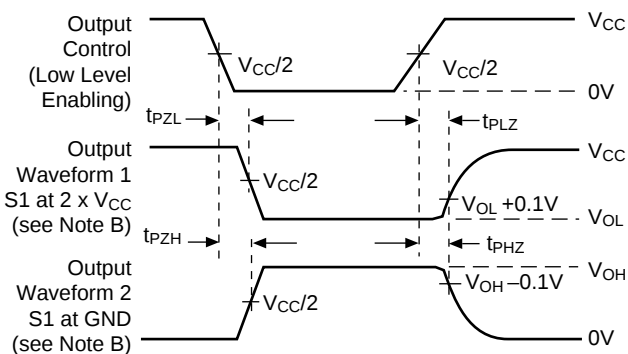
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

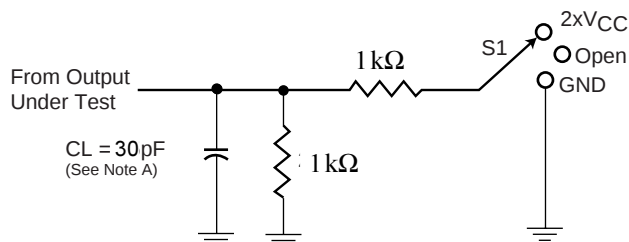
Figure 1. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0ns$, $t_F \leq 2.0ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

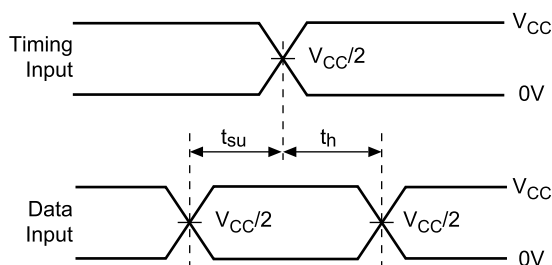
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8V \pm 0.15V$$

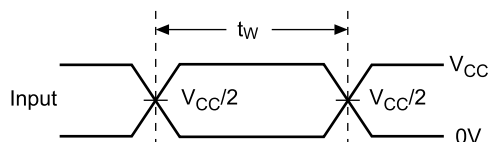


Load Circuit

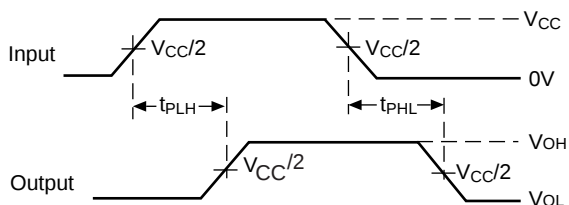
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x VCC GND



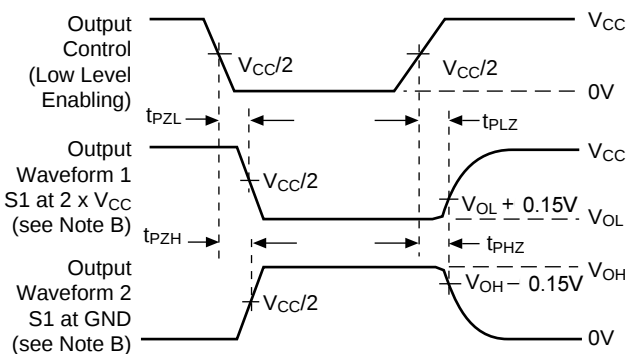
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

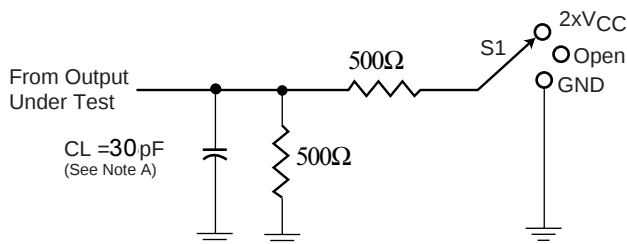
Figure2. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ ns}$, $t_F \leq 2.0\text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

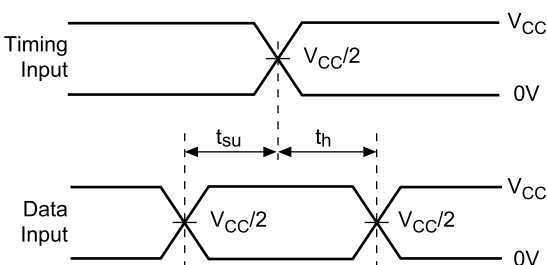
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5V \pm 0.2V$$

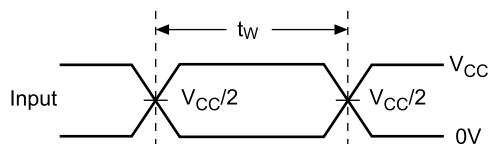


Load Circuit

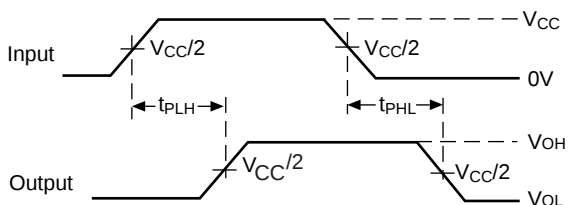
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



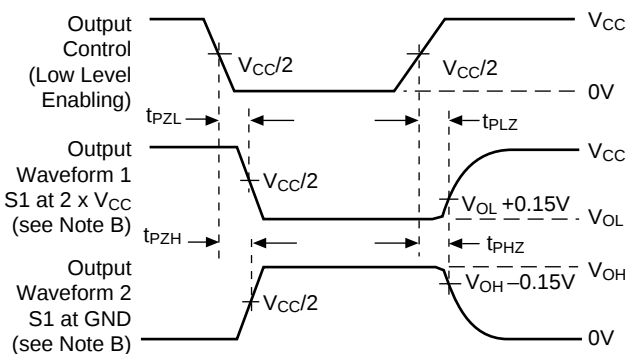
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Enable and Disable Times**

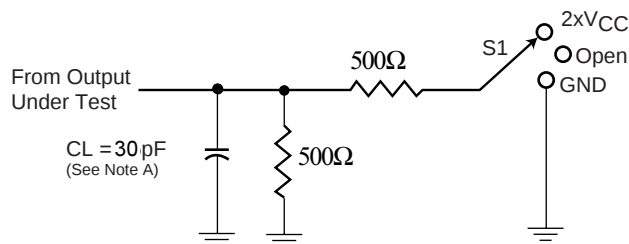
Figure3. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

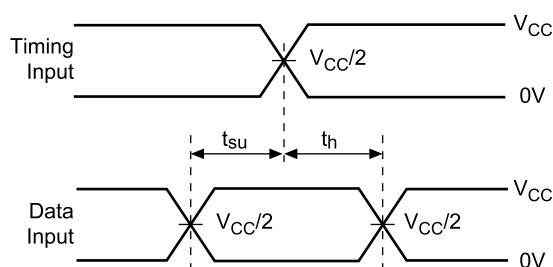
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3V \pm 0.3V$$

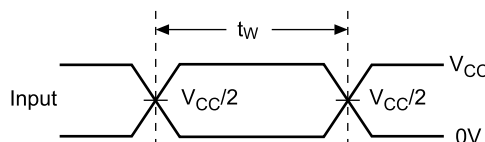


Load Circuit

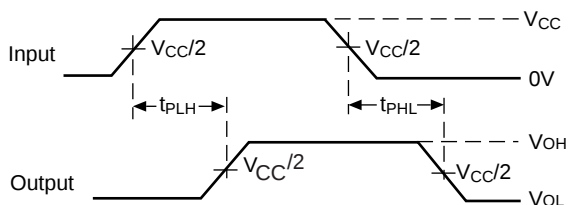
Test	S1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 x V _{CC} GND



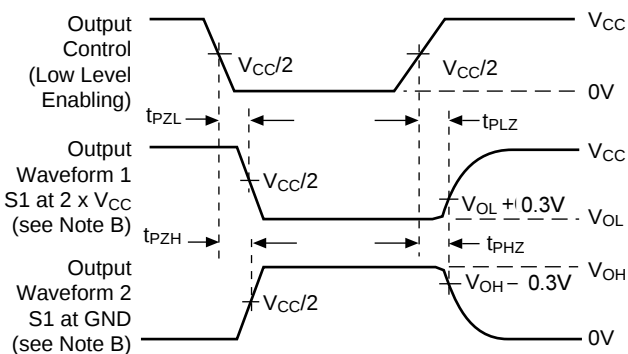
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



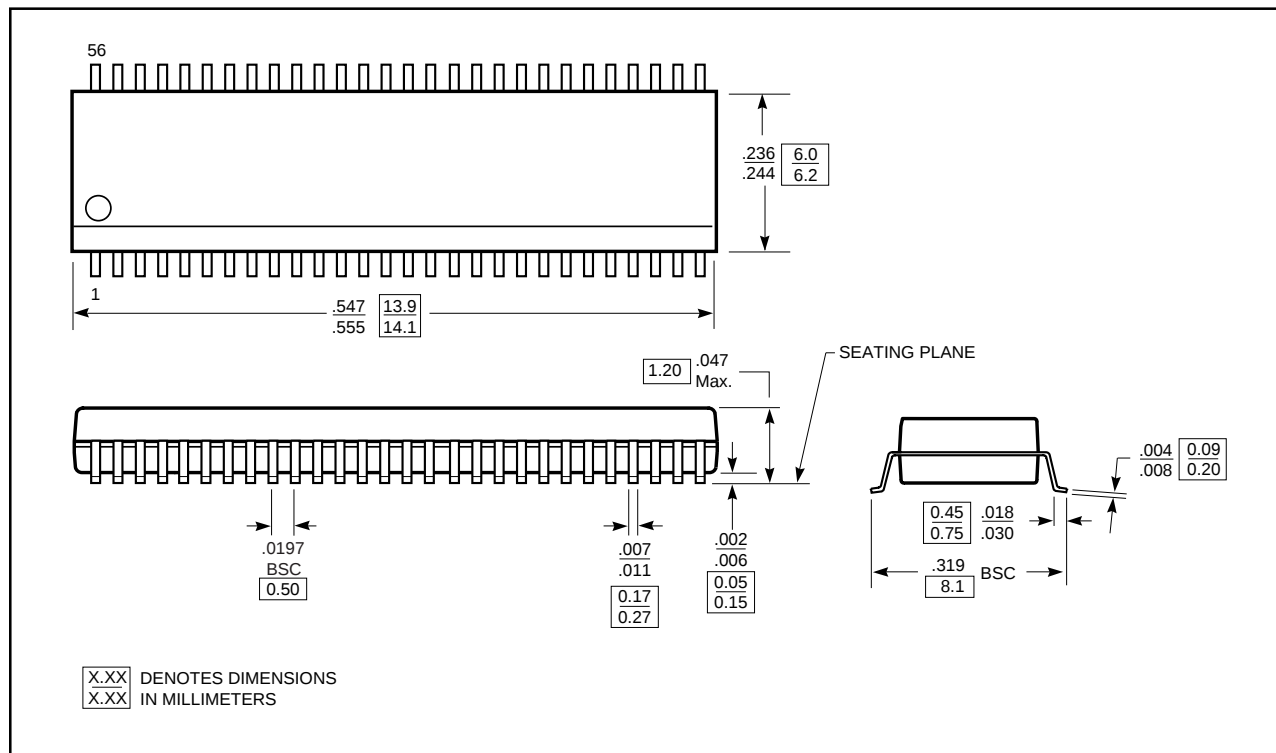
Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

Package Diagram : 56-pin 240-mil, Wide Plastic TSSOP (A)



Package Diagram : 56-pin 173-mil, Wide Plastic TVSOP (TSSOP) (K)

