PERICOM

PI74FCT161/163T
(25Ω Series) PI74FCT2161/2163T

High Speed CMOS Synchronous 4-Bit Binary Counters

Product Features:

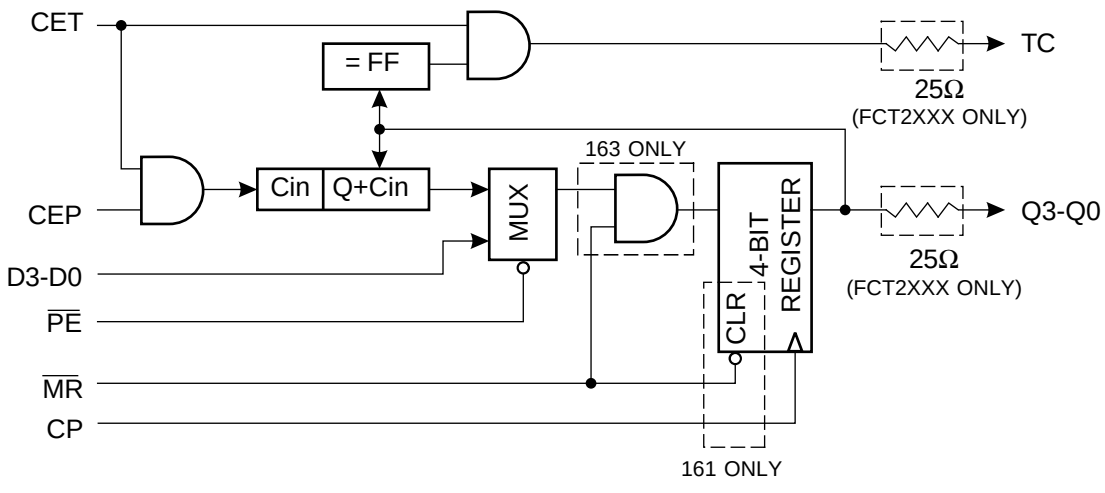
- PI74FCT161/163/2161/2163T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs (25Ω series only)
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  - 16-pin 150 mil wide plastic QSOP (Q16)
  - 16-pin 300 mil wide plastic SOIC (S16)

Product Description:

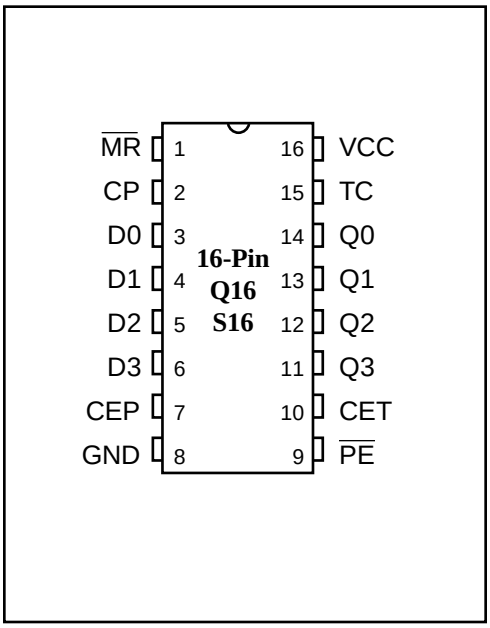
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT161T and PI74FCT163T are high-speed CMOS synchronous presettable 4-bit binary counters. The 161 has an asynchronous clear; the 163 has a clocked synchronous clear. Data is preloaded or the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs. and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression .

Logic Block Diagram



Product Pin Configurations (All Pins Top View)



Product Pin Description

Pin Name	I/O	Description
D3-D0	I	Data Inputs
Q3-Q0	O	Data Outputs
CP	I	Clock
$\overline{MR}$	I	Master Reset
CEP	I	Count Enable
CET	I	Count and TC Enable
TC	O	Terminal Count
$\overline{PE}$	I	Parallel Load Enable

Truth Table[1]

Inputs						Outputs			
						Q3-Q0			
$\overline{MR}$	$\overline{PE}$	CP	CEP	CET	DI	161	163	TC	Function
L	X	X	X	X	X	L	—	L	Clear 16l
L	X	↑	X	X	X	—	L	L	Clear l63
H	L	↑	X	X	D3-D0	D3-D0	D3-D0	X	Load Data
H	H	↑	H	H	X	Q+1	Q+1	X	Count
H	H	↑	L	X	X	Q	Q	X	Count Inhibit P
H	H	↑	X	L	X	Q	Q	x	Count Inhibit T
H	H	X	X	H	X	F	F	H	Count = 1111
H	H	X	X	H	X	0-E	0-E	L	Count ≠ 1111
H	H	X	X	L	X	X	X	L	TC Inhibit

Notes:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.3	0.50	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA (25Ω Series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	$V_{IN} \geq V_{HC}$; $V_{IN} \geq V_{LC}$		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND $T/\overline{R}$ = GND or V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_I = 10 MHz 50% Duty Cycle $T/\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		2.0	4.0[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		2.3	5.0[5]	
		Vcc = Max., Outputs Open fi = 10 MHz 50% Duty Cycle $T/\overline{R}$ = $\overline{OE}$ = GND Eight Bit Toggling	Vin = Vcc Vin = GND		3.5	6.5[5]	
			Vin = 3.4V Vin = GND		5.5	14.5[5]	

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics (Over Operating Range)

Symbol	Description[1]	Conditions	161, 163, 2161, 2163 Min	161, 163, 2161, 2163 Max	161A, 163A, 2161A, 2163A Min	161A, 163A, 2161A, 2163A Max	161C, 163C Min	161C, 163C Max	Unit
t_{CPQ}	Propagation Delay CP TO Qi, 161/3	C_L = 50 pF R_L = 500Ω	2.0	9.5	2.0	6.2	2.0	5.6	ns
t_{CPQ}	Propagation Delay CP to Qi, 2161/3		2.0	9.5	2.0	6.2	—	—	ns
t_{MRQ}	Propagation Delay $\overline{MR}$ to Qi, 161		2.0	13	2.0	8.5	2.0	7.8	ns
t_{MRQ}	Propagation Delay $\overline{MR}$ to Qi, 2161		2.0	14	2.0	9.1	—	—	ns
t_{CPTC}	Propagation Delay CP to TC		2.0	15	2.0	9.8	2.0	8.8	ns
t_{CETC}	Propagation Delay CET to TC		1.5	8.5	1.5	5.5	1.5	5.0	ns
t_{MRTC}	Propagation Delay $\overline{MR}$ to TC		1.5	11.5	1.5	7.5	1.5	6.8	ns

Notes:

1.See Test Circuit and Waveforms.

2. Minimum limits are guaranteed but not tested on Propgation Delays.

3. This parameter guaranteed but not production tested.

Timing Characteristics (Over Operaating Range)

Symbol	Description[1]	Conidtions	161 163 2161 2163 Min	Max	161A 163A 2161A 2163A Min	Max	161C 163C 2161C 2163C Min	Max	Unit
t_S	Data Setup Time Di to CP	C_L = 50 pF R_L = 500Ω	5.0		4.0		3.5		ns
t_H	Data Hold Time Di to CP		1.5		1.5		1.5		ns
t_{CH}	Count Enab. Setup Time CEP, CET to CP		11.5		9.5		8.5		ns
t_H	Count Enable Hold Time CEP, CET to CP		0		0		0		ns
t_{MRS} t_{PES}	Control Setup Time $\overline{MR}$, $\overline{PE}$ to CP		11.5		9.5		8.5		ns
t_{MRH} t_{PEH}	Control Hold Time $\overline{MR}$, $\overline{PE}$ to CP		1.5		1.5		1.5		ns
t_{CPW}	Clock Pulse Width HIGH or LOW		5.0		4.0		3.0		ns
t_{MRW}	MR Reset Pulse Width 161,2161		5.0		4.0		3.0		ns
t_{MRW}	Reset Recovery Time $\overline{MR}$ to CP, 161, 2161		6.0		5.0		4.0		ns

Notes:
1.See Test Circuit and Waveforms.
2. Minimum limits are guaranteed but not tested on Propgation Delays.
3. This parameter guaranteed but not production tested.