PI6C673 Single Chip Mobile Clock

440 BX™/VIAPromedia™ Chipset Clock for Pentium II™/Pentium III™/Celeron™ Processors

Features

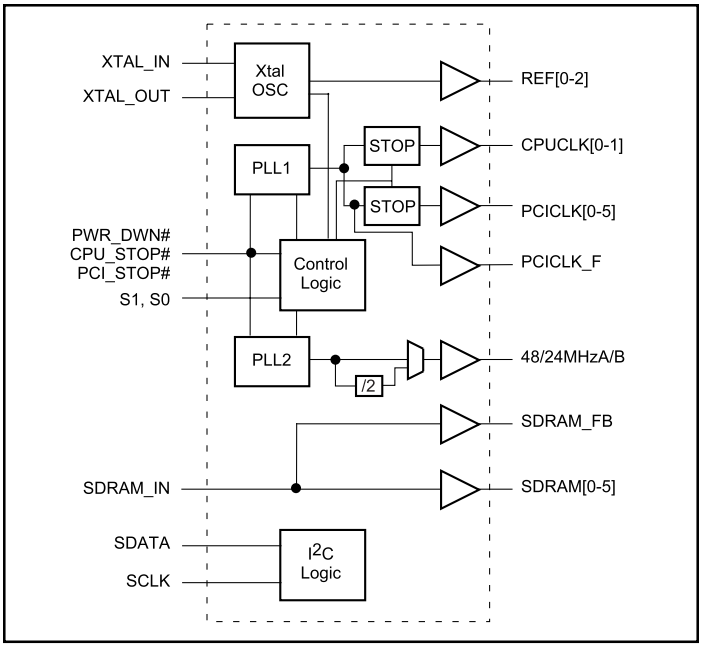
- A single chip provides both clock generation and clock buffer functions for supporting Mobile Pentium II™/Pentium III™/Celeron™ processors.
- I²C: 2-Wire Serial Interface. Device vendor ID is readable.
- Edge rate control of clock output signals for EMI suppression.
- Eight bandwidth selections of Spread Spectrum, optimizing for EMI suppression.
- Individual clock output enable/disable.
- Two CPUCLKs, with enhanced drive.
- Seven PCI clocks
- Seven SDRAM clocks for 3 SO DIMMs.
- Three 14.31818 MHz clocks
  (REF2 has an enhanced output drive).
- Two 48/24 MHz clocks.
- Separate power management control pins.
- Low skew and low power consumption
- Packages:
  – 48-pin 300 mil SSOP (V)
  – 48-pin 240 mil TSSOP (A)

Description

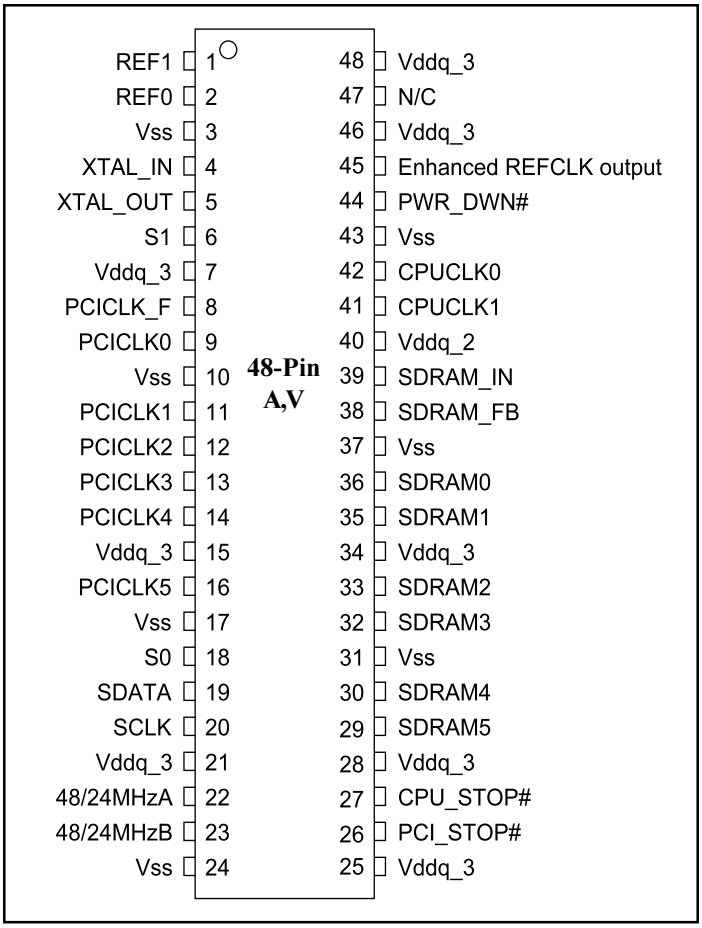
PI6C673 is the ideal low-cost solution for the 66/100 MHz SDRAM-based mobile/handheld platform. It integrates high-speed, low-noise, low-jitter, and low-skew clock generator and SDRAM buffers. The device supports either discrete or modular processors, three SO DIMMs, two 48/24 MHz outputs for USB and Super I/O, and a combination of six PCI slots and devices. Power management controls are realized with standard control signals such as: PWR_DWN#, CPU_STOP#, and PCI_STOP#. To further reduce power consumption and to minimize EMI emission, each individual output can be enabled/disabled through I²C interface. A wide range of SSC (Spread Spectrum Clock) options allow users to choose the best mode for minimal EMI. Generous power supply pins ensure that the device will have low noise and high performance.

Purchase of I²C components from Pericom conveys a license to use them in an I²C system as defined by Philips.

Block Diagram



Pin Configuration



Frequency Selection Table

S1	S0	CPUCLK	PCICLK
0	0	60.0	30.0
0	1	66.6	33.3
1	0	133.3	33.3
1	1	100	33.3

Pin Description

Pin	Type	Qty	Signal Name	Description
2,1,45	Out	3	REF[0-2]	14.318 MHz clock outputs.
8	Out	1	PCICLK_F	Free running PCI clock, not affected by PCI_STOP#.
9,11,12,13,14,16	Out	6	PCICLK[0-5]	PCI Clocks, greater than 1V/ns slew rate into 30pF load while maintaining 50 ±5% duty cycle.
6	In	1	S1	See Frequency Selection Table & Frequency Selection Pin
18	In	1	S0	See Frequency Selection Table & Frequency Selection Pin
22,23	Out	2	48/24 MHz	Selectable 48/24 MHz clock output by I²C. Default to 48 MHz.
29,30,32,33,35,36	Out	6	SDRAM[0-5]	SDRAM clocks, same frequency as SDRAM_IN.
27	In	1	CPU_STOP#	Stop CPUCLKs, active LOW.
26	In	1	PCI_STOP#	Stop PCICLKs, except PCICLK_F. Active LOW.
41,42	Out	2	CPUCLK	Host clock outputs, powered by Vddq_2.
38	Out	1	SDRAM_FB	Feedback clock outputs, same frequency as SDRAM_IN.
39	In	1	SDRAM_IN	Clock input for SDRAM[0–5] and SDRAM_FB outputs.
44	In	1	PWR_DWN#	Powers down the chip, active LOW.
4	In	1	XTAL_IN	Crystal input or driven by an externally generated reference clock input.
5	Out	1	XTAL_OUT	Crystal output. If an externally generated reference clock input is used at XTAL_IN pin, this pin is unconnected.
19	Bi-Dir	1	SDATA	Serial data in for serial configuration port. Has internal pull-up resistor. Conforms to the Philips I²C spec.
20	In	1	SCLK	Clock input for serial configuration port. Has internal pull-up resistor. Conforms to the Philips I²C spec.
7,15,21,25,28,34, 46,48	Power	8	Vddq_3	3.3V I/O power supply.
40	Power	1	Vddq_2	2.5V CPU Clock power supply.
3,10,17,24,31,37,43	Ground	7	Vss	Ground, common.

Power Management: Clock Enable Configuration*

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	Other Clock: SDRAM, REF, 48/24 MHzA 48/24 MHzB	Crystal, VCOs
X	X	0	low	low	low	off
0	0	1	low	low	running	running
0	1	1	low	running	running	running
1	0	1	running	low	running	running
1	1	1	running	running	running	running

*Full clock cycle timing is guaranteed at all times after initially powered up.

PI6C673 Power Management Requirements

Signal	Signal state	Latency: No. of rising edges of free-running PCICLK
CPU_STOP#	1 (enabled)(1)	1
	0 (disabled)(2)	1
PCI_STOP#	1 (enabled)(1)	1
	0 (disabled)(2)	1
PWR_DWN#	1 (normal operation)(3)	2ms
	0 (power down)	2 max.

Notes:
1. Clock ON latency is defined from when the clock enable goes active to the first valid clock.
2. Clock OFF latency is defined from when the clock enable goes inactive to the last clock is driven low out of the device.
3. Power UP latency is when PWR_DWN# goes inactive (HIGH) to when the first valid clocks are driven from the device.

I²C Serial Interface

By using standard I²C command bytes, the I²C registers can be written. The ID number at Byte 8 can be read back for identification purposes.

Address Assignment

A6	A5	A4	A3	A2	Al	A0	R/W
1	1	0	1	0	0	1	-----

Data Protocol

1 bit	7 bits	1	1	8 bits	1	
Start bit	Slave Addr	R/W	Ack	Command Code	Ack	Byte Count = N

1 bit	8 bits	1	8 bits	1		8 bits	1	1
ACK	Data Byte 1	ACK	Data Byte 2	ACK	---	Data Byte N	ACK	STOP

Byte 0: Functional and Frequency Select Clock Register (1 = enable, 0 = disable).

Bit	Pin #	Power-Up Default	Description
Bit 7	N/A	X	(Reserved)
Bit 6	N/A	1	Spread Spectrum Selection bit SSC2
Bit 5	N/A	1	Spread Spectrum Selection bit SSC1
Bit 4	N/A	1	Spread Spectrum Selection bit SSC0
Bit 3	22	1	48/24 MHz (Freq Select) 1=48MHz, 0=24MHz
Bit 2	23	1	48/24 MHz (Freq Select) 1=48MHz, 0=24MHz
Bit 1 Bit 0	N/A N/A	0 0	**Bit1 Bit 0** 1 1 : Tri-State (all outputs) 1 0 : Spread Spectrum enabled 0 1 : Test mode (see table) 0 0 : Non-Spread Spectrum Operating Mode

Spread Spectrum Bandwidth Selection Table

SSC2	SSC1	SSC0	Bandwidth	Direction
0	0	0	±0.625 %	Center
0	0	1	±0.5 %	Center
0	1	0	–0.35 %	Down
0	1	1	–0.25 %	Down
1	0	0	–2.5 %	Down
1	0	1	–1 %	Down
1	1	0	–1.21 %	Down
1	1	1	–0.9 %	Down (default)

Test Mode Selection

S1	S0	CPU	PCI, PCI_F	REF	24MHz	48MHz
0	0	TCLK/4	TCLK/8	TCLK	TCLK/4	TCLK/2
0	1	TCLK/4	TCLK/8	TCLK	TCLK/4	TCLK/2
1	0	TCLK/4	TCLK/12	TCLK	TCLK/4	TCLK/2
1	1	TCLK/4	TCLK/12	TCLK	TCLK/4	TCLK/2

Note:
TCLK is a test clock over driven on the XTAL_IN input during test mode.

Byte 1: CPU, 24/48 MHz Active/Inactive Register
(1 = enabled, 0 = stopped, output held LOW)

Bit	Pin #	Power-Up Default	Description
Bit 7	22	1	48/24 MHz (Enabled/Stopped)
Bit 6	23	1	48/24 MHz (Enabled/Stopped)
Bit 5	N/A	X	(Reserved)
Bit 4	N/A	1	(Reserved)
Bit 3	38	1	SDRAM_FB (Enabled/Stopped)
Bit 2	–	1	(Reserved)
Bit 1	41	1	CPUCLK1 (Enabled/Stopped)
Bit 0	42	1	CPUCLK0 (Enabled/Stopped)

Byte 2: PCI Active/Inactive Register (1 = enable, 0 = stopped, output held LOW)

Bit	Pin #	Power-Up Default	Description
Bit 7	N/A	x	Reserved
Bit 6	8	1	PCICLK_F (Enabled/Stopped)
Bit 5	16	1	PCICLK5 (Enabled/Stopped)
Bit 4	14	1	PCICLK4 (Enabled/Stopped)
Bit 3	13	1	PCICLK3 (Enabled/Stopped)
Bit 2	12	1	PCICLK2 (Enabled/Stopped)
Bit 1	11	1	PCICLK1 (Enabled/Stopped)
Bit 0	9	1	PCICLK0 (Enabled/Stopped)

Byte 3: SDRAM Active/Inactive Register (1= enabled, 0 = stopped, output held low)

Bit	Pin #	Power-Up Default	Description
Bit 7	N/A	1	(Reserved)
Bit 6	N/A	1	(Reserved)
Bit 5	29	1	SDRAM5 (Enabled/Stopped)
Bit 4	30	1	SDRAM4 (Enabled/Stopped)
Bit 3	32	1	SDRAM3 (Enabled/Stopped)
Bit 2	33	1	SDRAM2 (Enabled/Stopped)
Bit 1	35	1	SDRAM1 (Enabled/Stopped)
Bit 0	36	1	SDRAM0 (Enabled/Stopped)

Byte 4: SDRAM Active/Inactive Register (1= enabled, 0 = stopped, output held LOW)

Bit	Pin #	Power-Up Default	Description
Bit 7	N/A	1	Reserved
Bit 6	N/A	1	Reserved
Bit 5	N/A	1	Reserved
Bit 4	N/A	1	Reserved
Bit 3	N/A	1	Reserved
Bit 2	N/A	1	Reserved
Bit 1	N/A	1	Reserved
Bit 0	N/A	1	Reserved

Byte 5: Peripheral Active/Inactive Register (1= enabled, 0 = stopped)

Bit	Pin #	Power-Up Default	Description
Bit 7	N/A	X	Reserved
Bit 6	N/A	1	Reserved
Bit 5	N/A	1	Reserved
Bit 4	45	1	REF2 (Enabled/Stopped)
Bit 3	N/A	X	Reserved
Bit 2	N/A	1	Reserved
Bit 1	1	1	REF1 (Enabled/Stopped)
Bit 0	2	1	REF0 (Enabled/Stopped)

Byte 8: Pericom ID Register (Read only, not writable)

Bit	Pin #	Power-Up Default	Description
Bit 7		0	x50H, ASCII Character Upper Case "P"
Bit 6		1	
Bit 5		0	
Bit 4		1	
Bit 3		0	
Bit 2		0	
Bit 1		0	
Bit 0		0	

Operating Conditions

Maximum Ratings

Description	Min.	Max.
Input Voltage	Vss - 0.5V	Vdd + 0.5V
Storage temperature	- 65ºC	150ºC

Recommended Operating Conditions

Parameter	Operating Conditions
Vddq_3	3.3V ±5%
Vddq_2	2.5V ±5%
Ambient temperature	0ºC to +70ºC

DC Characteristics at Recommended Operating Conditions(2)

Parameter	Min.	Typ.	Max.	Units
Input Low voltage for S[0:1], CPU_STP#, PCI_STP#, PWR_DWN#			0.8	V
Input High voltage for S[0:1], CPU_STP#, PCI_STP#, PWR_DWN#	2.0			
Tri-State leakage currrent			10	µA
Dynamic supply current, Idd, at CPUCLK = 100 MHz			150	mA
Static supply current (PWR_DWN# = 0)			30	µA

AC Characteristics at Recommended Operating Conditions(1,2)

Parameter	Min.	Typ.	Max.	Units
CPUCLK leading PCICLK offset	1		4	ns
Clock output duty cycle	45	50	55	%
Skews: (CPUCLK-CPUCLK), (PCICLK-PICCLK), (SDRAM-SDRAM)			175	ps
Period Jitter, Adjacent cycles			250	
Period Jitter, Ajacent Cycles (PCLK,48 MHz)			500	

Notes:
1. CPUCLKs are measured at 1.25V, other clock outputs are measured at 1.5V.
2: Loads: CPUCLKs, 48/24MHz, and REF clocks: 20pF max., SDRAMs, PCICLKs: 30pF max.

CPUCLK(0:1) 2.5V Buffer Operating Characteristics

(T_A=0~70ºC; Vddq_2=2.5V ±5%; C_L=20pF)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Ioh	Pull-up current	Vout = Vddcpu –0.5V	–23	44		mA
Ioh	Pull-up current	Vout = 1.2V	–37	78		
Iol	Pull-down current	Vout = 0.4V	15	51		
Iol	Pull-down current	Vout = 1.2V	38	105		
tr	Rise time	0.4V-2.0V	0.4		1.3	ns
tf	Fall time	2.0V-0.4V	0.4		1.3	

PCICLK(_F,0:5) 3.3V Buffer Operating Characteristics

(T_A=0~70ºC; Vddq_3=3.3V±5%; C_L=30pF)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Ioh	Pull-up current	Vout = Vddpci –0.5V	–23	24		mA
Ioh	Pull-up current	Vout = 1.5V	–48	58		
Iol	Pull-down current	Vout = 0.4V	13	26		
Iol	Pull-down current	Vout = 1.5V	44	67		
tr	Rise time	0.4V-2.4V	0.4		2.4	ns
tf	Fall time	2.4V-0.4V	0.4		2	

48/24MHz(A,B), REF(0:1) 3.3V Buffer Operating Characteristics

(T_A=0~70ºC; Vddq_3 = 3.3V ±5%; C_L= 20pF max.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Ioh	Pull-up current	Vout = Vdd48 –0.5V or Vddref –0.5V	–23	15		mA
Ioh	Pull-up current	Vout = 1.5V	–48	34		
Iol	Pull-down current	Vout = 0.4V	13	16		
Iol	Pull-down current	Vout = 1.5V	40	41		
tr	Rise time	0.4V-2.4V	0.4		4	ns
tf	Fall time	2.4V-0.4V	0.4		4	

SDRAM(_FB, 0:5), REF2 Buffer Operating Characteristics

(T_A=0~70ºC; Vddq_3 =3.3V ±5%; C_L=30pF max. for SDRAM; C_L=20pF max. for REF2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Ioh	Pull-up current	Vout = Vddm - 0.5V	–27	30		mA
Ioh	Pull-up current	Vout = 1.5V	–56	77		
Iol	Pull-down current	Vout = 0.4V	22	31		
Iol	Pull-down current	Vout = 1.5V	74	82		
tr	Rise time	0.4V-2.4V	0.4		1.8	ns
tf	Fall time	2.4V-0.4V	0.4		1.8	

Buffer Characteristics for Enhanced REFCLK

Characteristic	Conditions	Symbol	Min.	Typ.	Max.	Units
Pull-Up Current	Vout = VDD - 0.5V	IOH_1	-23	-	-	mA
Pull-Up Current	Vout = VDD/2	IOH_2	-48	-	-	
Pull-Down Current	Vout = 0.4V	IOL_1	13	-	-	
Pull-Down Current	Vout = VDD/2	IOH_2	44	-	-	
Rise/Fall Time, @ 0.4V-2.4V	See Switching Characteristic Note 1	Tr, Tf	0.4	-	1.3	nS

Ordering Information

Part Number	Description
PI6C673V	48-pin 300-mil wide, 2.80mm SSOP
PI6C673A	48-pin 240-mil wide, 1.20mm TSSOP

Packaging Mechanical Information

• Plastic 48-pin 300-mil SSOP Package (Pericom V48)
• Plastic 48-pin 240-mil TSSOP Package (Pericom A48)