

PFM21020 SPECIFICATION

2.11-2.17 GHz, 20W, Two-Stage Power Module

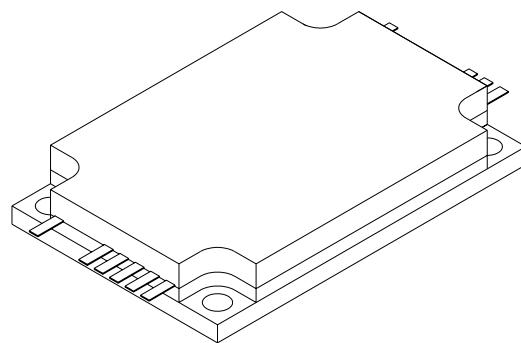
Enhancement-Mode Lateral MOSFETs

This UMTS module has been designed to serve as a driver amplifier in either the output or the error path of a multi-channel amplifier. The transistors are Si LDMOS devices biased in Class AB operation, in order to achieve high linearity and efficiency. Particular emphasis has been placed on wideband operation with excellent gain flatness and phase linearity. The PFM21020 is a fully integrated power amplifier with temperature compensation circuitry and extensive internal power supply bypassing.

The module has separate drain supply leads (one per stage) and high impedance gate voltage inputs. The gate supply voltage is nominally +12 volts to set an optimum bias quiescent current. The user may optimize the bias for a particular application by adjusting the gate supply voltages. The drain supply is normally +28 VDC, although the amplifier will operate with drain supply ranging from +25 to +30 VDC.

ELECTRICAL CHARACTERISTICS (Vdd=28Vdc, Tc=25deg C, 50 ohm system, unless otherwise specified)

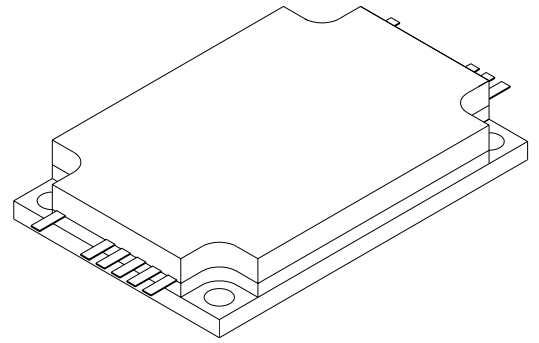
Characteristic	Symbol	Min	Typ.	Max	Unit	Test Conditions	Comments
Frequency Range	BW	2110		2170	MHz		Performance degrades minimally for the extended 2080-2200 MHz band.
Quiescent Current (total current)	Idq		210	240	mA	No RF applied	Bias at which performance is measured.
Power Gain @f=2140 MHz	Pg	26.5	27.5	28.5	dB	CW	
Gain Flatness versus Frequency A) At T=+25 deg C B) -10<T<+90 deg C	Gf		±0.15 ±0.20	±0.25 ±0.35	dB	CW	
Gain Variation over -10 to +80 deg C	Gt		-0.025	-0.04	dB/degC		Refer to appended typical data.
Phase Flatness	ΔΦ		±1.0	±1.5	Deg		Deviation from linear phase. Allows a constant time delay offset in the measurement.
Group Delay	td		4.1		nsec		
Linearity – CW Tones (2-Tone Cont. Random Phase, 900 kHz)	IM3 IM5 IM7		-42 -47 -50	-37 -42 -45	dBc dBc dBc		+24 < Pave < +37.5 dBm Idsq = 75, 135 mA



PFM21020 SPECIFICATION (Continued)

2.11-2.17 GHz, 20W, Broadband Two-Stage Power Module

Characteristic	Symbol	Min	Typ.	Max	Unit	Test Conditions	Comments
W-CDMA (PAR=9.4dB) ACPR (3.84 MHz BW) a) 5.0 MHz Offset b) 10.0 MHz Offset	ACPR		-47 -58	-45 -56	dBc	Average Output Power = 34 dBm	ACPR is relative to the total in-channel power. Idsq = 75, 135 mA
EDGE modulation Error Vector Magnitude	EVM		1.5	2.5	%	EDGE signal, Pave= 38 dBm	Idsq = 75, 135 mA
EDGE Adjacent Channel Rejection (RMS) a) 400 KHz Offset b) 600 KHz Offset	ACPR		-61 -72	-57 -67	dBc dBc	EDGE signal, Pave= 38 dBm	Idsq = 75, 135 mA
EDGE Power Added Efficiency		20	22		%	@ EVM=2.5%	Idsq = 75, 135 mA
Power Output @ 1dB compression	P1dB	20	25		W	CW	Idsq = 40, 160 mA
Efficiency (with one CW signal operated at 1 dB gain compression).		32	36		%	CW	Idsq = 40, 160 mA
Input Overdrive Level				+25	dBm	Peak	
Input VSWR	VSWR		1.5:1	1.7:1			Pin ≤ +13 dBm
Output VSWR	VSWR		1.2:1	1.4:1			
Gate Supply Terminal Impedance			10		KOhm		Typical gate supply voltage is +12.0 volts.
Input & output decoupling		The input has a low impedance path (10 ohms) to ground at video frequencies. The output is isolated by a 24 pF capacitor (refer to schematic).					
Load Mismatch Stress Load VSWR=3:1, all phase angles		Unconditionally stable. Reliably operates with 20 Watts CW forward power, at case temperatures to +70 degrees C.					



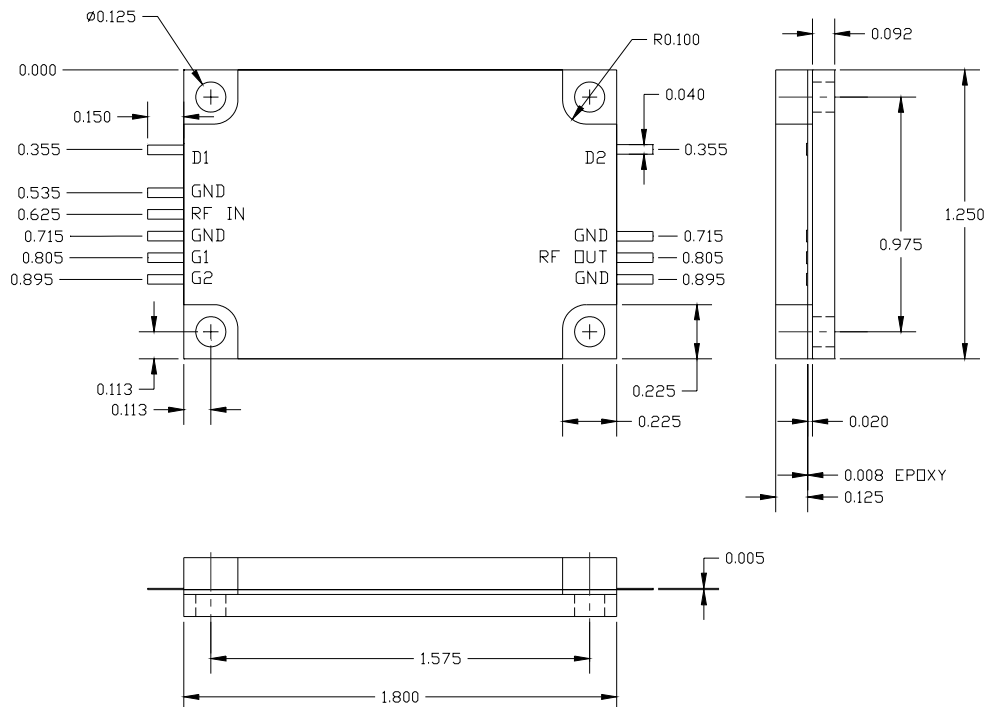
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MAXIMUM RATINGS (@25degC, unless otherwise specified)

Rating	Symbol	Value	Unit
DC Supply Voltage	Vs	30	Vdc
RF Input Power	Pin	+24	dBm
Storage Temperature Range	Tstg	-40 to +150	Deg C
Operating Case Temperature Range	Tc	-30 to +90	Deg C
RF Output Power	Pout	40	W
Thermal Resistance (Max channel temp rise divided by module dissipation for Pout=20W, at Tbase=+85 C)	Θ_{jc}	2.0	Deg C/W

Module Outline

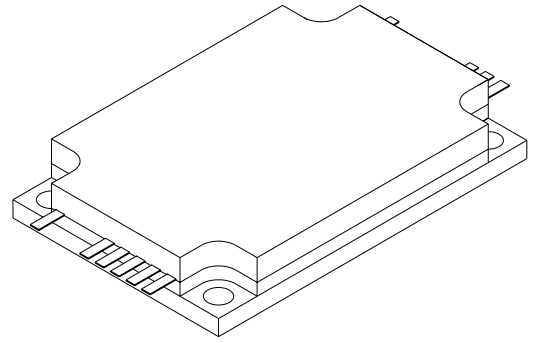


The unit must be well grounded and thermally attached to a heat conducting surface for proper operation. The module is designed to accept 4-40 socket head screws, either Torx or Allen head. The use of a split lockwasher and flatwasher is recommended. The screws should be torqued to 4 - 6 inch-lbs. A thermally conductive compound (a thin layer between the unit base and the mounting surface) is recommended for applications with



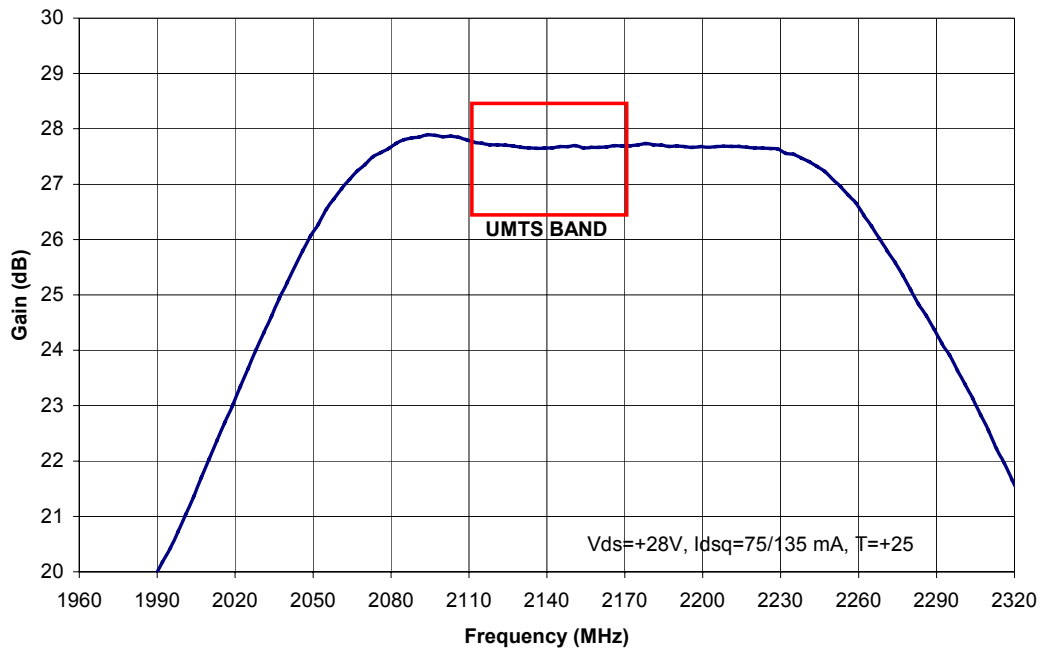
high average power dissipation in which the mounting surface may exceed 50 degrees C. Thermal compound is optional (may not be necessary) for situations with low average power dissipation, such as WCDMA or error amplifier applications with very high peak-to-average signals. The PFM21020 bottom surface is designed to have better than 1 mil flatness. It is recommended that the mounting surface (to which the unit is attached) have similar flatness characteristics.

The most essential precaution to achieve specified performance is proper grounding. Refer to the test fixture figure for illustration of a typical RF interface. It is recommended that the ground tabs adjacent to the RF input and RF output tabs be connected to RF ground through via holes in the mating RF circuit boards.

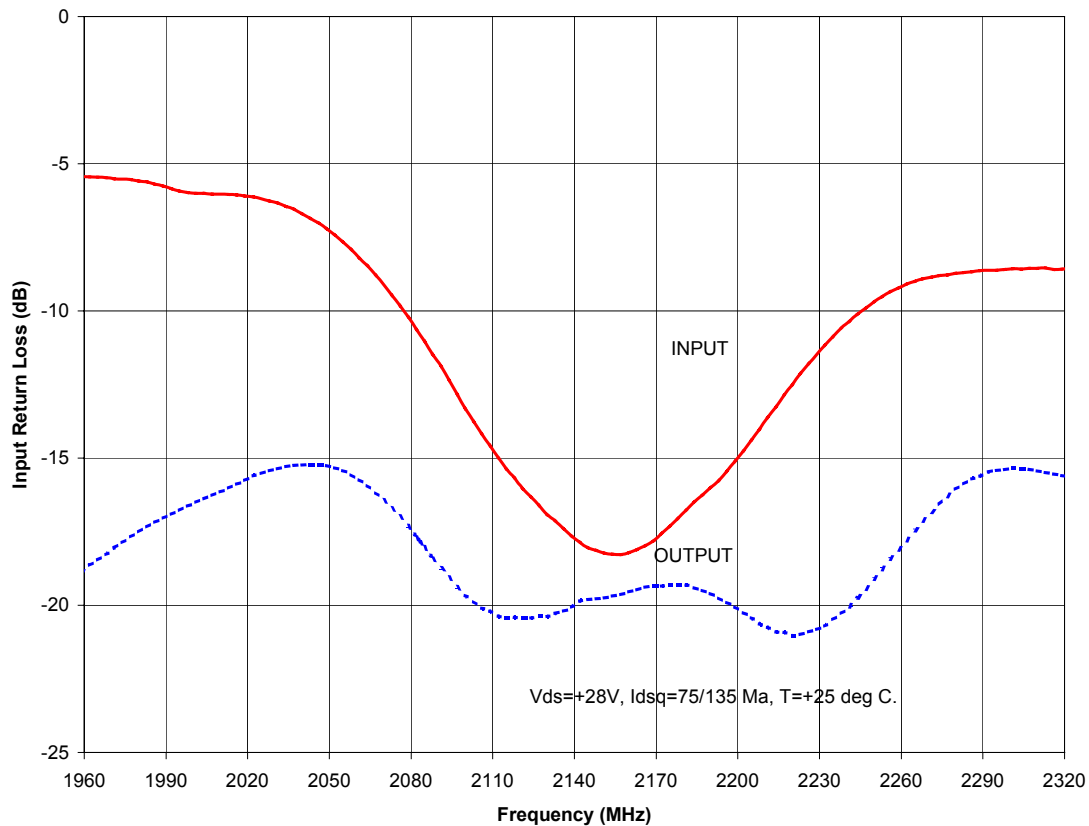


PFM21020 Typical Electrical Characteristics

PFM21020 UMTS 2-Stage Module Gain



PFM21020 UMTS Module Input and Output Return Loss

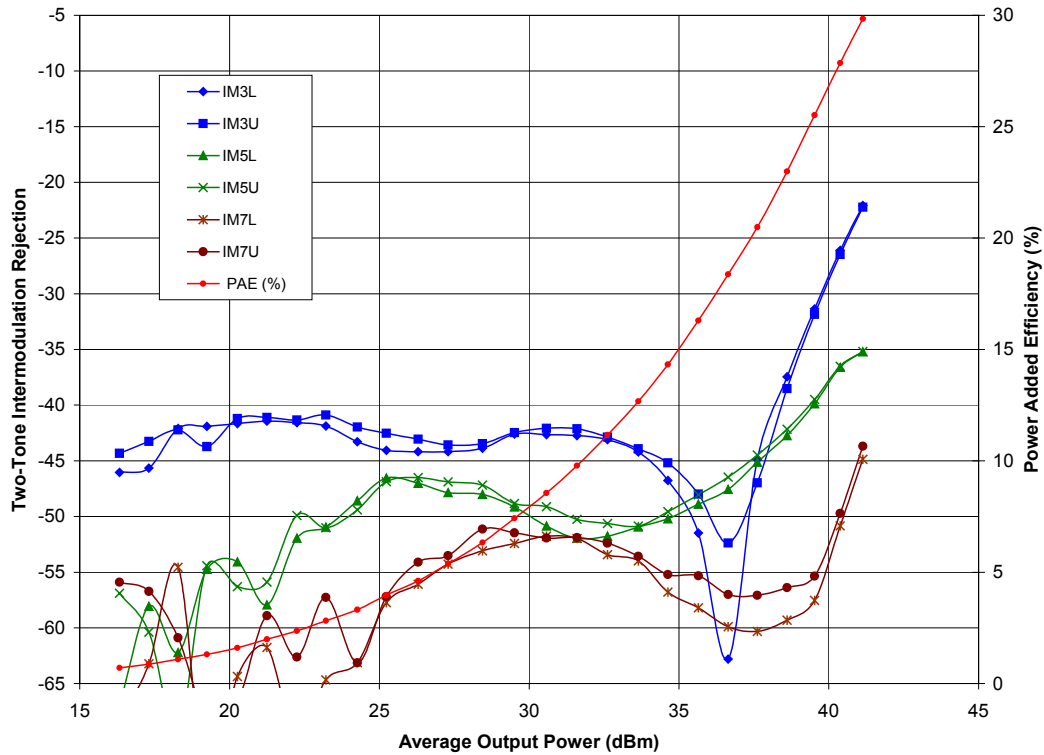




PFM21020 Typical Electrical Characteristics- Continued

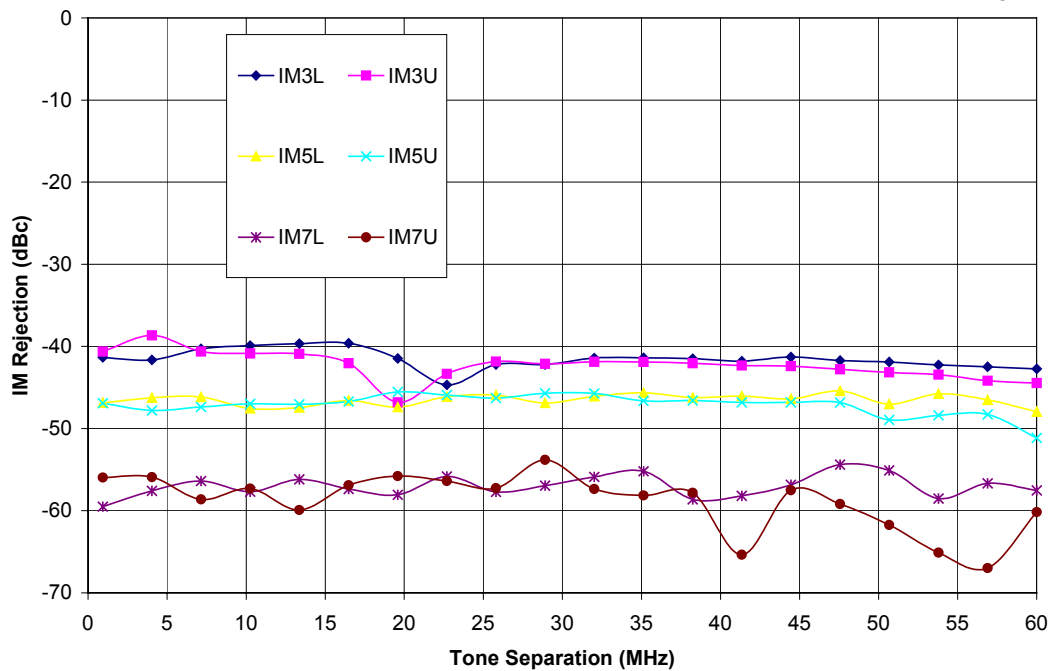
PFM21020 Two-tone IMDs & P.A.E. vs. Pout, F = 2140 MHz

VDC=+28 V, Idsq= 75, 135 mA, Delta F= 900 KHz



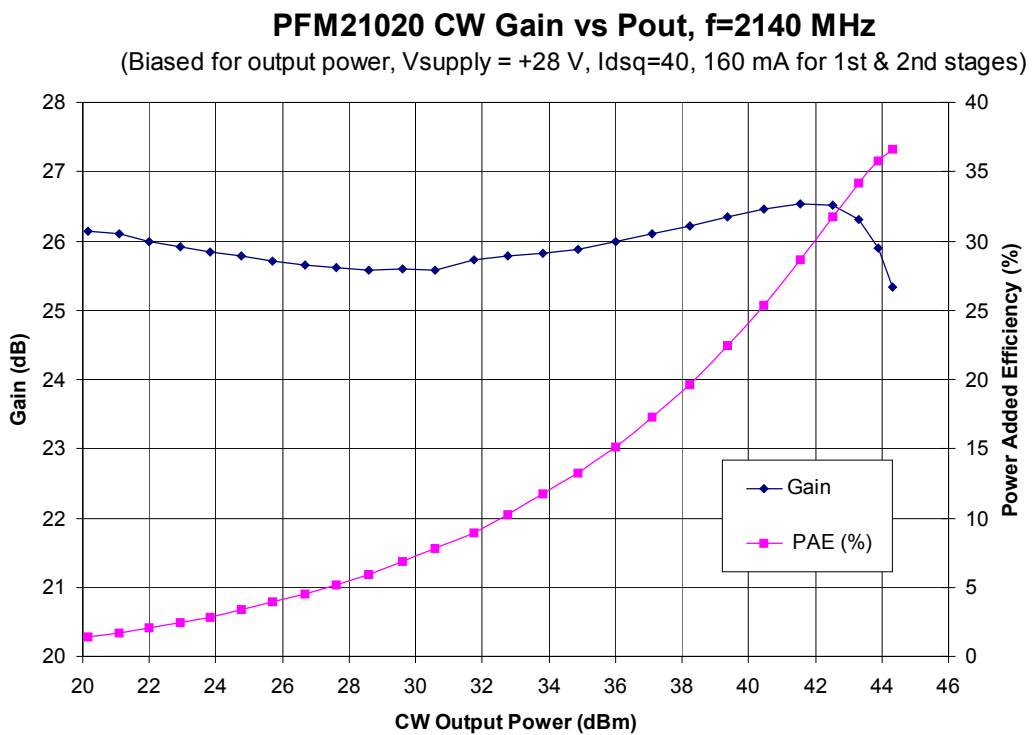
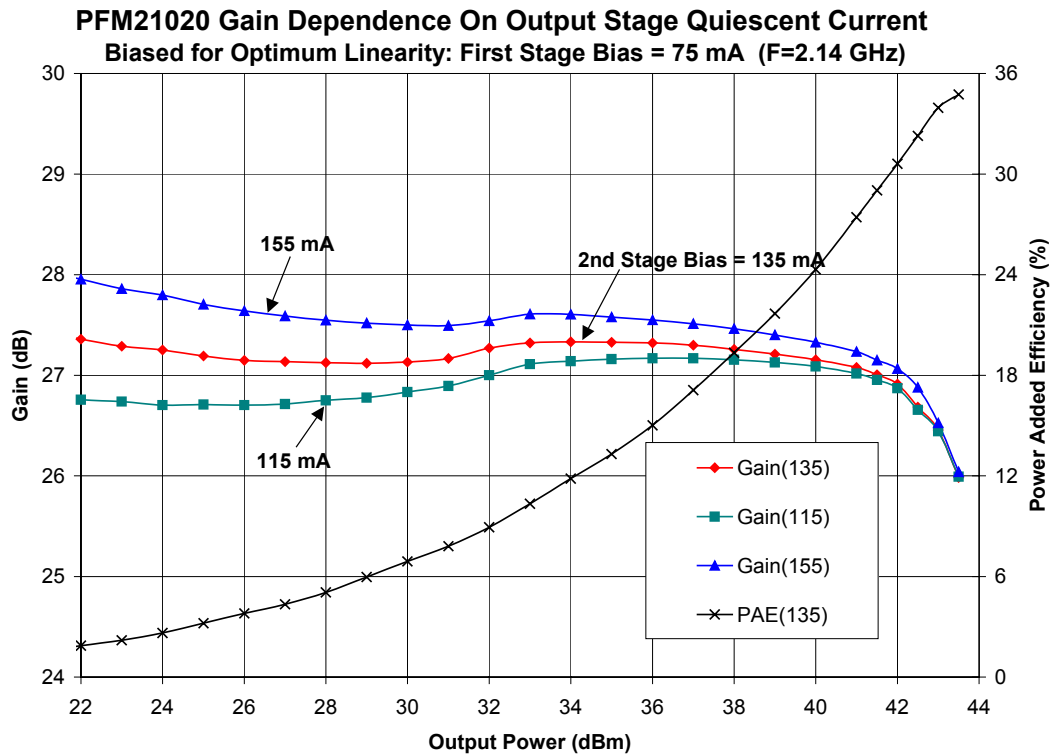
PFM21020 Intermodulation versus Tone Separation

F1=2110 MHz, F2=(F1+Tone Separation), Idsq=75, 135 mA, Pout =23 dBm average





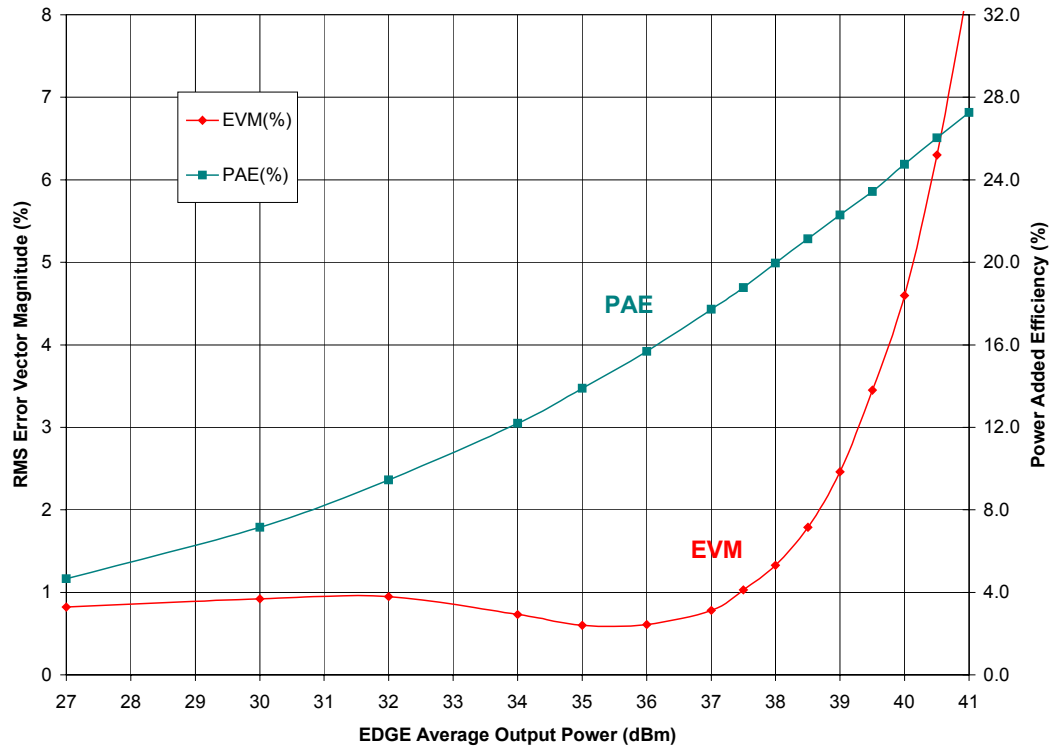
PFM21020 Typical Electrical Characteristics- Continued





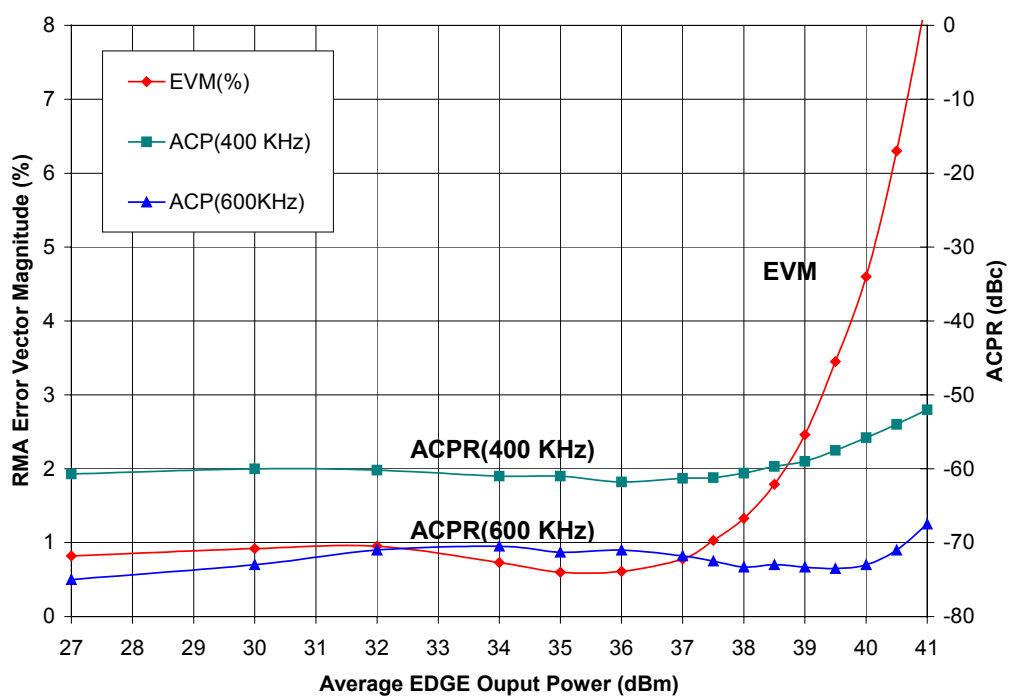
PFM21020 UMTS 20W Amplifier, EDGE EVM & PAE

F=2140 MHz, Vsupply = +28V, Idq = 75/135 mA (input/output stages), T=+25 C



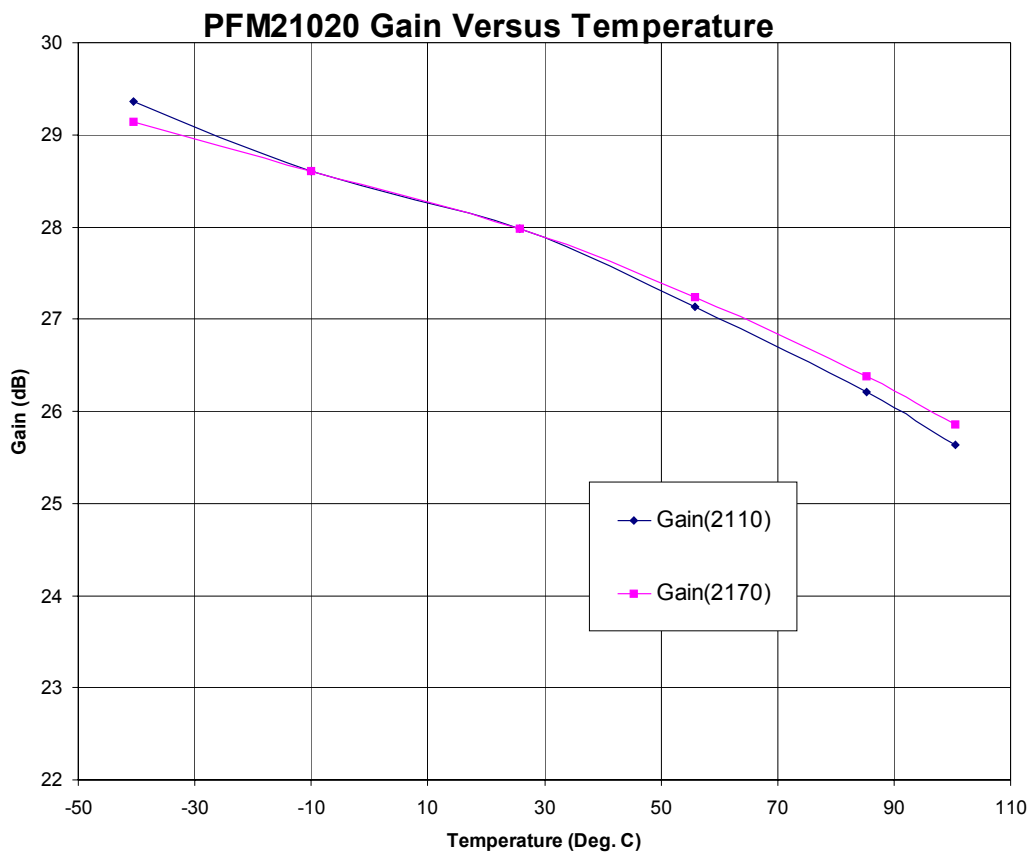
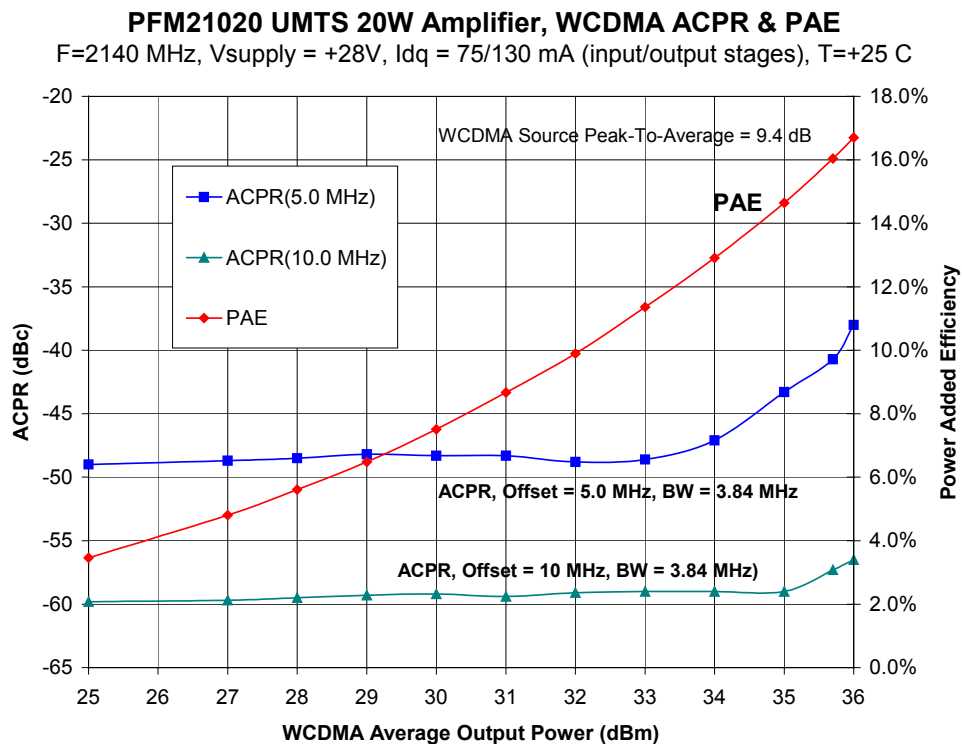
PFM21020 UMTS 20W Amplifier, EDGE EVM & ACPR

F=2140 MHz, Vsupply = +28V, Idq = 75/135 mA (input/output stages), T=+25 C



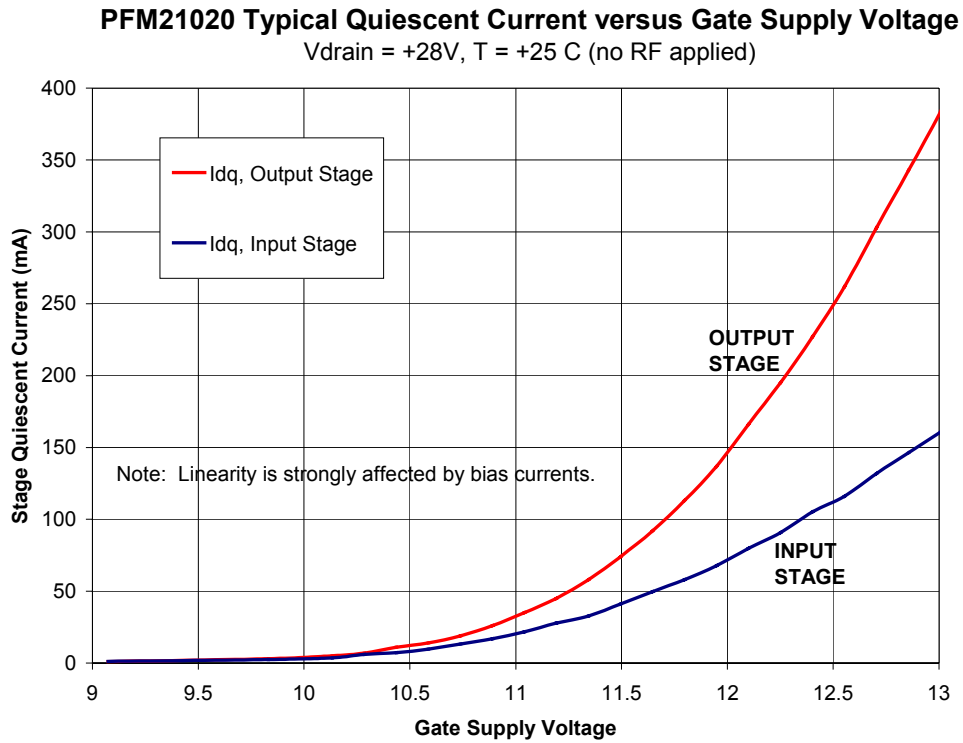


PFM21020 Typical Electrical Characteristics- Continued





PFM21020 Typical Electrical Characteristics- Continued



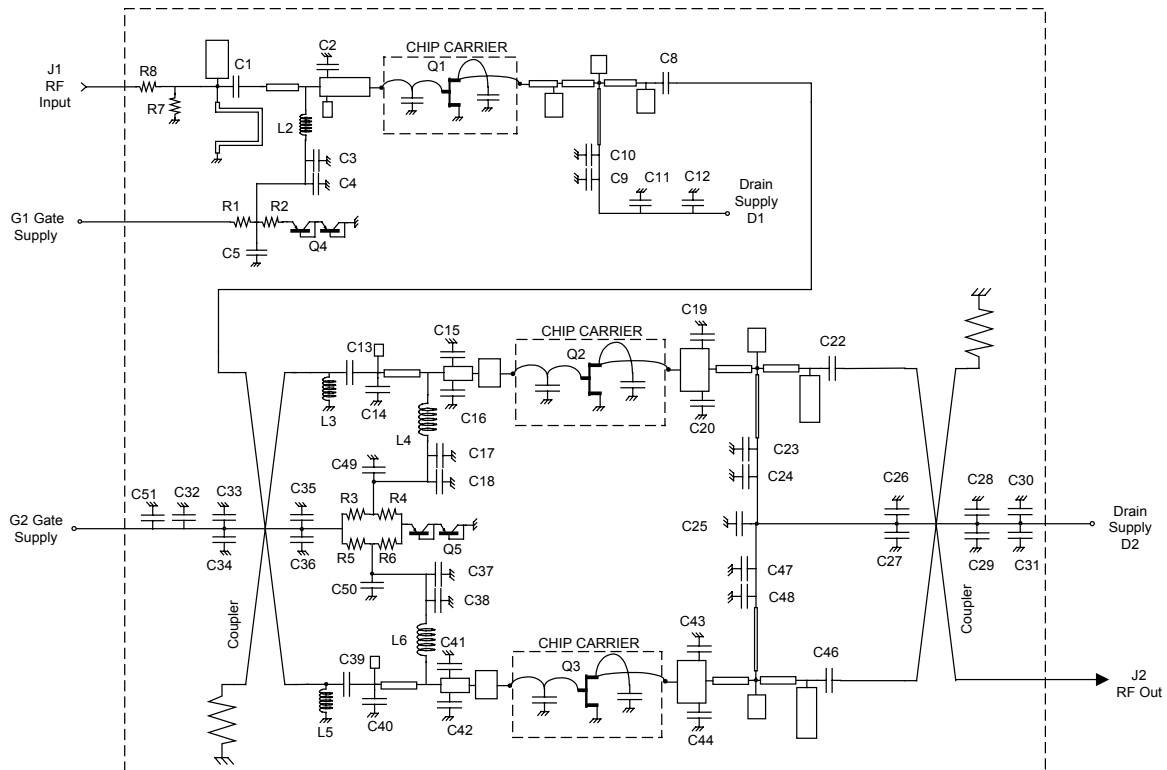
Bias for optimum linearity is typically 75 mA for the input stage and 130 to 150 mA for the output stage. Optimum bias for maximum output power at 1 dB gain compression and efficiency at higher output levels is typically 40 mA for the input stage and 160 mA for the output stage. It is recommended that the effect of bias level be determined for the particular signal protocol of each application.



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Schematic for UMTS 20W Two-Stage Module



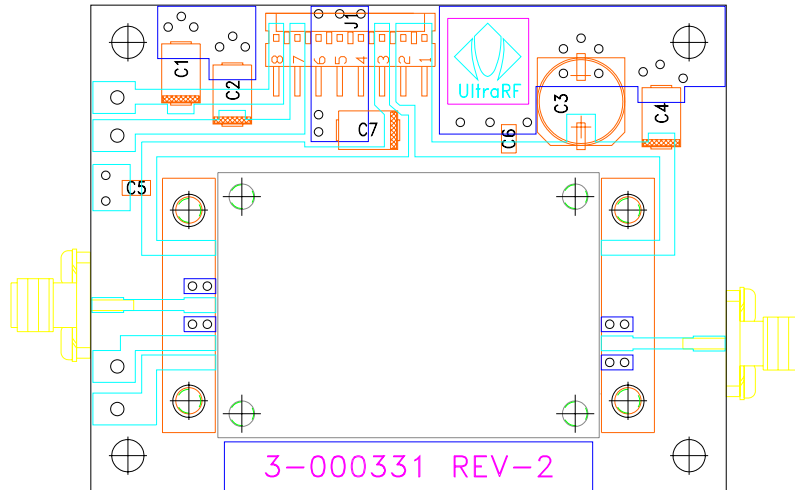
Note: Extensive power supply decoupling is provided internal to the module. Bypass capacitors to 0.1 microfarad are included on the drain supplies. It is recommended that an external 47 microfarad capacitor be used on the power supply line to the drain, and that a 1 microfarad external capacitor be used on the gate supply lines.



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Test Fixture for 2.11-2.17 GHz, Two-Stage Power Module

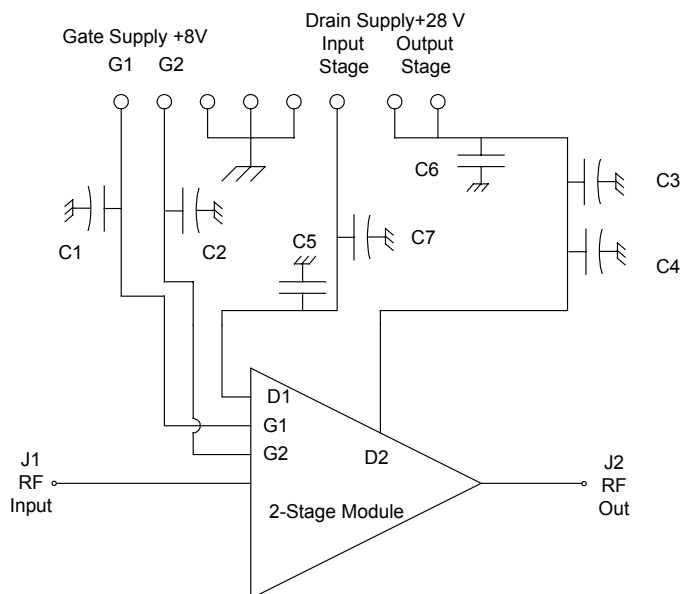


Note: This figure also serves as an illustration of appropriate RF interfaces on mating RF PCBs. Low inductance ground paths are provided for the pair of RF ground tabs adjacent to the RF Input and RF output tabs. Additionally, care has been taken to preserve the flatness of the conducting surface on which the unit will mount. Non-conducting clamps secure the RF and bias tabs to the PCB for this fixture. These clamps are not used for typical applications, wherein the tabs are soldered directly to the PCB at the interface pads.



PFM21020 SPECIFICATION (Continued) **2.11-2.17 GHz, 20W, Two-Stage Power Module**

Schematic for Test Fixture for 2.11-2.17 GHz, Two-Stage Power Module



Parts List for RF Test Fixture

Designator	Description	Qty
C4, C7	CAP, 2.2uf SMT TANTALUM, 50V	1
C1, C2	CAP, 10uf 16V SMT TANTALUM	2
C3	CAP, 47UF, 50V, ELECTR SMT	1
C5, C6	CAP, 24 pF, 200V, 0603 (ATC)	2