Application Of Zero Delay Buffers in Systems with Large Memory Arrays

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Abstract

Pericom's family of Zero Delay Clock Drivers have the best specifications compared to any PLL clock drivers to move data into and out of large memory array without errors and data misalignments. The PI6C2501/2(3V), PI6C5932(5V), PPI6C9910(5V), PI6C9930(3V), PI6C2308A(3V), PI6C2509A(3V), and PI6C2510A(3V) provide multiple copies of a reference clock driven from a state-of-the-art PLL (phase-locked loop) technology developed by Pericom. These devices provide the best characteristics in terms of tight specification on skew, jitter, and phase error.

Clocking any large memory array composed of SDRAM modules, such as the array inside a RAID controller card, is a perfect example of a system needing a large number of clocks with zero delay compared to a reference clock. Memory arrays composed of clusters of fast, synchronous dual-port RAMs require multiple clocks with very little skew between them and zero delay with respect to the reference clock. Pericom's PI6C2308A provides eight clock outputs with less than 200ps skew between them and 150ps delay from input to all outputs. From a maximum reference clock input of up to 134 MHz, the PI6C2509A generates nine identical copies with 150 ps delay. The PI6C2510A generates 10 identical clocks from a reference clock.

Zero Delay Drivers can significantly reduce the performance. Pericom Application Brief 24 recommends use of an inexpensive single output zero-delay buffer and a non-zero-delay buffer such as PI6C3818A. As shown in Figure 1, this combination produces, a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, combined with PI6C3818A, the system designer can create an eighteen-output zero-delay buffer. This application note intends to discuss the use of Zero Delay PLL buffers in a RAID controller board. It briefly explains the RAID concept and the RAID Controller card. A description of the controller card and the use of Zero Delay PLL in conjunction with the memory array inside the card follows.

Redundant Array of Independent Disks (RAID)

Not long ago 1GB of Disk space was considered huge. Now, 1GB is the starting point for servers. If a system needs 8GB of Disk space, buying one 8 GB disk is not the best choice in terms of performance and fault tolerance. A better solution would be four 2-GB disks. More disks provide more spindles spinning and thus more data can be written to the disks at the same time. The arrangements of multiple disks are very important. No matter what arrangement, systems are implementing some forms of RAID.

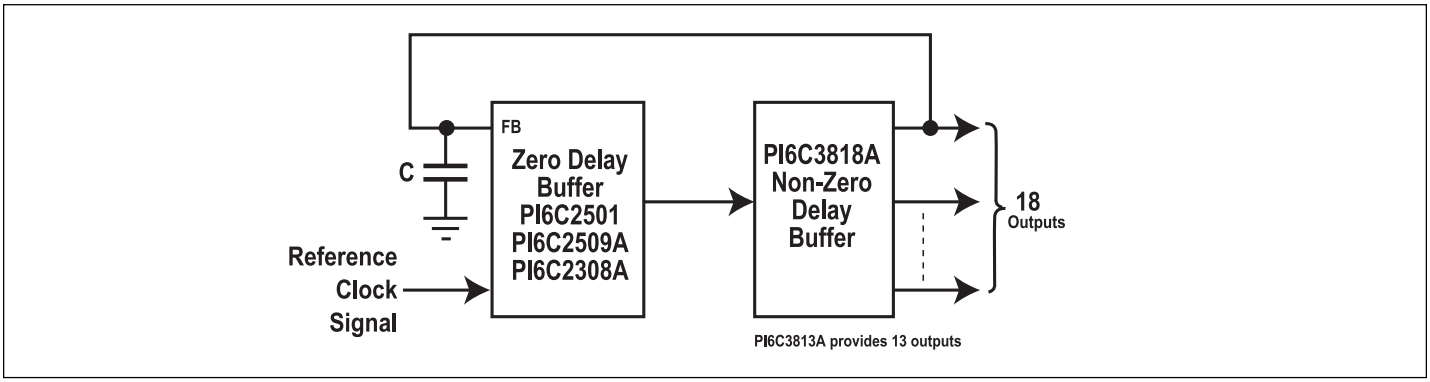

Figure 1. This Combination Provides Zero Delay Between the Reference Clock Signal and 18 Outputs

Introduction

A big advantage of the PI6C2509A and PI6C2308A is that they allow the system designer to adjust or move the output clocks forward or backward in time with respect to the reference clock, to fine-tune a design. As depicted in Figure 1, this is done by using a capacitor C at the FB input of the PLL. The P6C2509A and PI6C2510A provide nine or ten copies of the reference clock respectively. If the design requires more than 10 zero delay clock outputs, using two or more PI6C2509A or PI6C2510A drivers is impractical. The device-to device skew as a result of using two

Open servers are adding fault tolerance since they tend to pour resources into I/O. RAID subsystems provide both performance and reliability. To achieve high throughput, RAID subsystems can stripe data across several disk drives. For reliability purposes, to provide fail safe data back up, disk mirroring is the continuous duplication of data on a second drive. For all these reasons RAID is becoming almost synonymous with servers. SCSI's presence in the emerging open servers architecture is assured since much of server technology is focusing on I/O performance.

RAID Disk Controller Card

A disk controller card typically has a large onboard memory array that increases performance by keeping recently used data in the faster Synchronous DRAM Array. The amount of memory can range from 125 MB to 512 MB. The data bandwidth path between the RAID controller and the PC server is increased to 266 MB/sec with the 64-bit PCI bus architecture. Figure 2 shows the block diagram of a RAID controller.

2509A/2510A PLL Drivers

The PLL buffer needs a reference clock from the main system. It then generates 9 or 10 clock signals with zero delay compared to the reference clock. The system only needs to provide one clock signal, which greatly reduces the number of clock signals generated (minimize EMI).

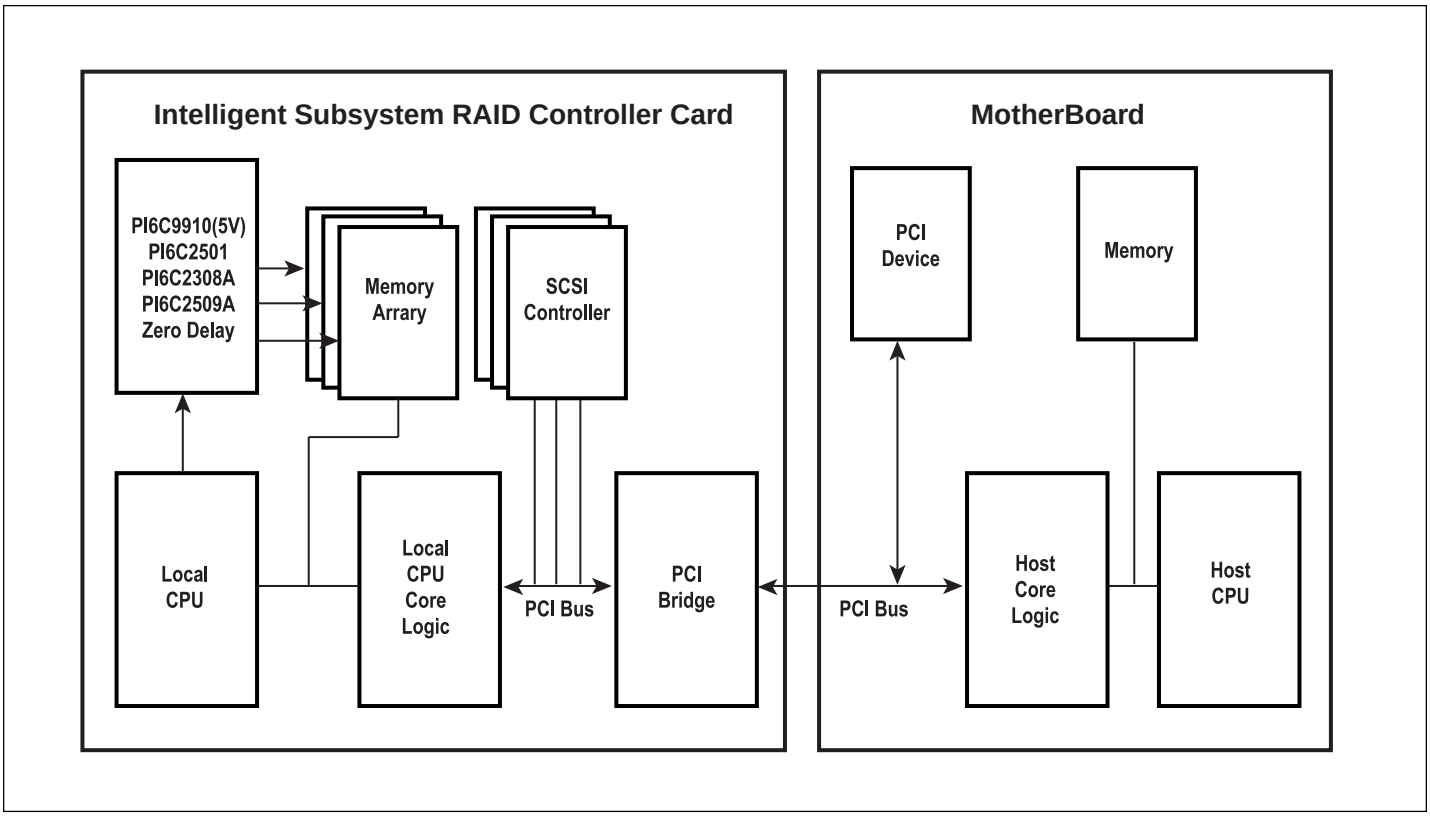

Figure 2. RAID Controller Card

The memory array composed of SDRAM modules inside a RAID controller card uses multiple clocks with zero delay compared to a reference clock to input and output data from memory to the local CPU. Through the PCI bridge, the host only sees a single device with a single PCI address space rather than seeing a collection of SCSI controllers, a processor, and a memory array. This configuration boundary between the host domain and controller domain provides an intelligent processor in the controller with much more control and flexibility in terms of how it allocates those resources and assigns them in the address space. The PCI bridge provides features to help the intelligent processor so either side can communicate with each other. These include an I^2C interface that is used in the RAID controller.

As shown in Figure 3, the feedback output FBOUT pin is directly connected to the feedback input FBIN pin. Figures 4 and Figure 5 show the output clocks lead and lag the Input Clock, respectively. The C1 capacitor is designed to adjust the relative timing between the Input Clock and the output clocks, if needed. C1 is typically not connected. As the C1 value increases, the timing of the output clocks will become more leading in time relative to the Input Clock.

The output drivers of Pericom's PI6C2509A have been carefully designed to provide sufficiently heavy pull-up and pull-down drive currents such that the clock signals at the SDRAM chips meet the rise/fall time requirements of the SDRAM chips. The output drivers are also designed to keep undershoot and overshoot of the clock signals to a minimum.

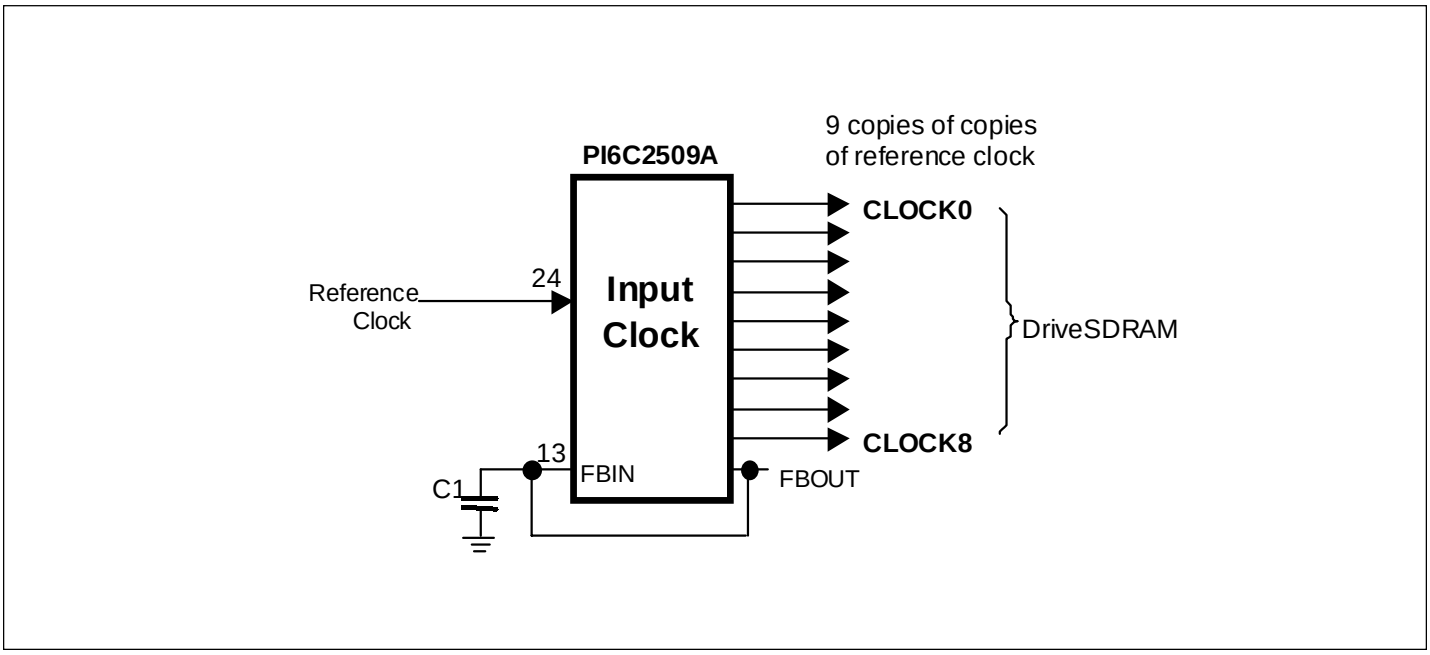

Figure 3. Block Diagram of PI6C2509A

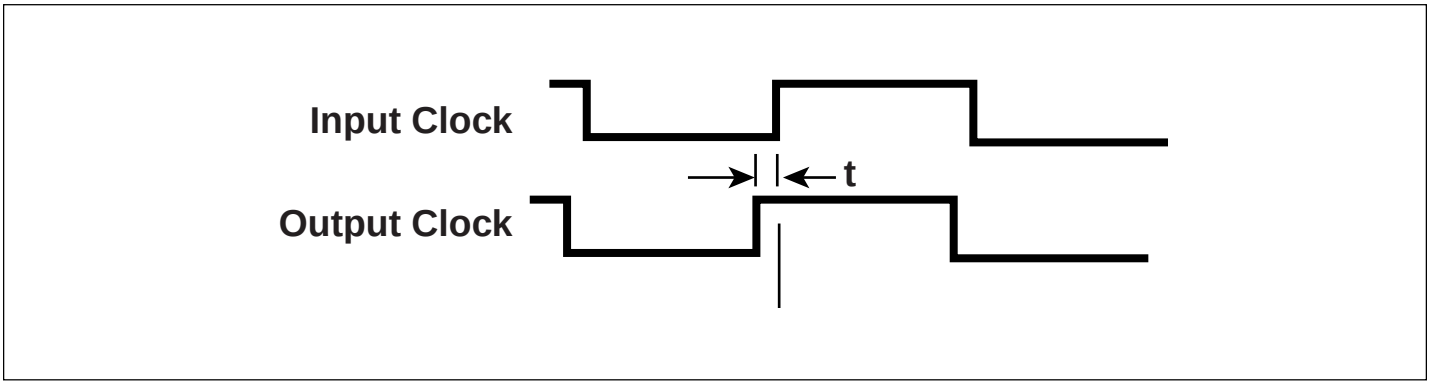

Figure 4. The Output Clocks Lead the Input Clock

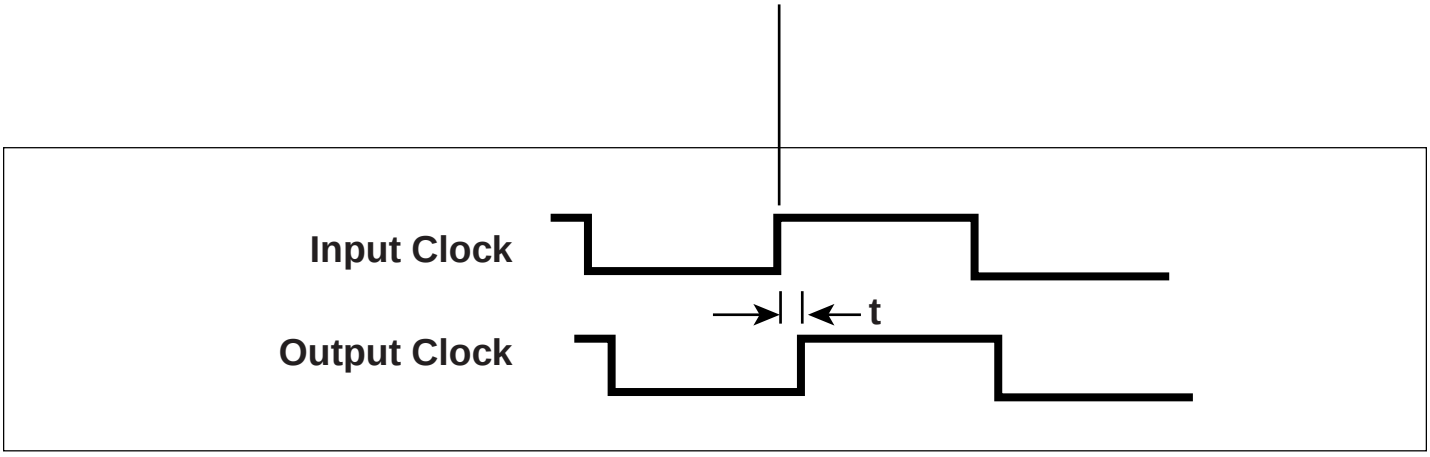

Figure 5. The Output Clocks Lag the Input Clock

When a designer selects a PLL driver chip for a large SDRAM array design, the following AC parameters are critical:

Phase Error: propagation-time between Clock Input pin and clock feedback input FBIN pin. Ideally, when clock outputs are exactly identical to the Clock Input, phase error should be very small. A phase error of 150ps leading or lagging is fine in 100 MHz and 66MHz clock distribution circuits.

***Cycle-to-Cycle Jitter*:** difference of period-time between one clock cycle to the adjacent clock cycle. A critical issue on jitter is the Clock Input with spread spectrum. Many PLL circuits will increase jitter and fail to meet jitter spec when the motherboard clock generator enables spread spectrum modulation. The 2509A/2510A parts are designed to meet the jitter spec when spread spectrum is disabled as well as enabled (also for 100MHz & 66MHz).

Output Skew: time skew among all clock outputs. The 2509A/2510A output drivers meet the 200ps spec for 100MHz and 66MHz.

PI6C2501 Clock Driver

The PI6C2501 features a low-skew, low-jitter, phase-lock loop (PLL) clock driver (see Figure 6). By connecting the CLKBOUT output to the feedback FBIN input, the propagation delay from the CLKIN input to any clock output will be nearly zero.

Product Features

- High performance Phase-Lock Loop Clock Distribution for 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V Vcc
- Packaged in Plastic 8-pin SOIC Package (S8)
- Wide range of Clock Frequencies

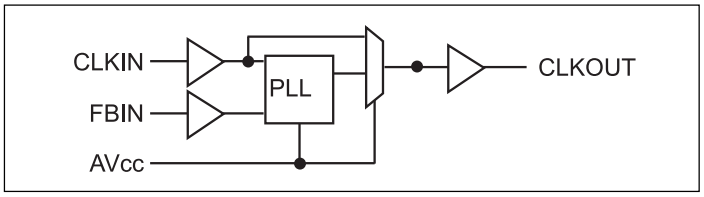

Figure 6. PI6C2501 Block Diagram

PI6C2308A PLL Driver

Providing two banks of four outputs, the PI6C2308A and PI6C2308 are 3.3V zero delay buffers designed to distribute clock signals in applications such as PC, workstation, datacom, telecom, and high performance systems. Each bank of four outputs can be controlled by the select inputs. Figure 7 depicts the block diagram for the PI6C2308.

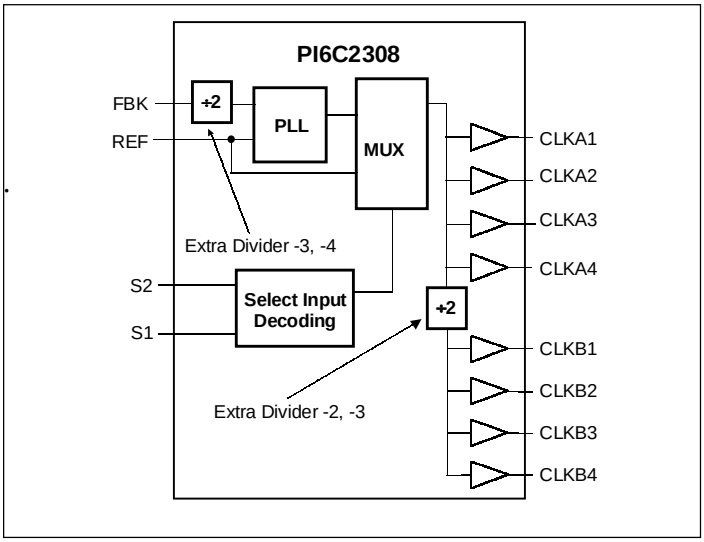

Figure 7. PI6C2308 Block Diagram

With much better electrical characteristics than the competition, the PI6C2308A provides 8 copies of a clock signal that has 150 ps phase error compared to a reference clock. Skew between output clock signals for PI6C2308A is less than 200 ps. When there are no rising edges on the REF input, the PI6C2308/A enters a power down state where the PLL is off and all outputs are three-stated resulting in less than 50 μA of current draw. The base part, PI6C2308/A-1 provides output clocks in sync with a reference clock. For designs that require faster rise and fall times, the PI6C2308/A-1H is the high drive version of the PI6C2308/A-1. Depending on which output drives the feedback pin, the PI6C2308/A-2 provides 2X and 1X clock signals on each output Bank. The PI6C2308/A-3 provides 4X and 2X clock signal on the output. The PI6C2308/A-4 provides 2X clock signal on all outputs. PI6C2308/A allows bank B to be three-Stated if all output clocks are not required. For testing purposes, the Select inputs connect the input clock directly to outputs.

Summary

PLL clock drivers, can be used to de-skew the delay through large clock trees. These devices are also used in applications where the system designer needs large clock signal multiples that are in sync with a reference clock. Almost all significantly large memory arrays need this clocking scheme. This application note has mainly focused on clocking for larger memory arrays inside RAID controller cards or other systems such as networking switches. Large synchronous memory arrays are used in almost all datacom applications to move data in-between modules or cards.

Pericom has developed an array of low-skew, Zero Delay Clock Drivers such as the PI6C5932 (3V), PI6C9910 (3V), PI6C9930(3V), PI6C2501(3V), PI6C2509A(3V), PI6C2510A (3V) and PI6C2308A for both 5V and 3.3V applications. Low clock skews guarantee better designs and optimum performance. This application note can be applied to any system that requires multiple clocking for large memory arrays.