# PI6C110/PI6C110E Layout Guidelines

*By Nelson Soo, September1, 1999*

## Introduction

The PI6C110/110E is an integrated clock generator and SDRAM buffer, providing all the timing signals for the Intel Whitney 810/ 810E chipset. This brief provides the recommended connections for the PI6C110/110E clock generator to control EMI and to ensure proper device performance. Many of the following techniques can be applied to a variety of high-speed clock designs.

## Power Supply Connection

Figure 1 depicts the dual-supply connection for the PI6C110/110E. A power supply noise reduction circuit, consisting of a ferrite bead, filter capacitor, and bypass capacitors for each system $V_{CC}$, should be implemented. A summary of each component of the power supply noise reduction circuit follows:

### Ferrite Bead (FB)

A ferrite bead is used to block high-frequency noise from the power supply. This component prevents the noise generated by the clock generator from reaching the main power supply plane. A minimum of 1.7 Henries is recommended, however, the bigger the ferrite bead, the better the noise reduction. Available board space must be considered when choosing the ferrite bead's value because if provides noise isolation only – and does not enhance or degrade the performance of a clock generator.

Use only those ferrite beads that can provide the rated DC current to the Vcc island without saturating. In addition, the DC impedance of the ferrite bead must be as low as possible, preferably between 0-5 Ohms. At the clock frequency, the impedance of the ferrite bead must be relatively high, typically greater than 50 Ohms under loaded conditions with DC current flowing through it. The ferrite bead will then present a large impedance at the clock frequency, and will prevent noise arising from clock harmonics spreading around the PCB.

### Bypass Capacitor

Each clock generator VDD pin should have a 0.1µF capacitor to ground for elimination of crosstalk between clock output frequencies. These capacitors must be placed as close to the device pins as possible on the same side of the clock generator chip, preferably within 0.25 inches of the pins. For the best performance, the use of high-quality, monolithic, ceramic, surface-mount capacitors is suggested.

### Filter Capacitor

A 22µF tantalum capacitor is used to eliminate low frequency noise from the power supply. This capacitor prevents power supply droop when the clock generator is switching all outputs simultaneously with maximum capacitive load. Destabilization of the power supply will result in increased jitter of the clock outputs. Place this capacitor on the clock-generator side of the ferrite be as close to it a physically possible.

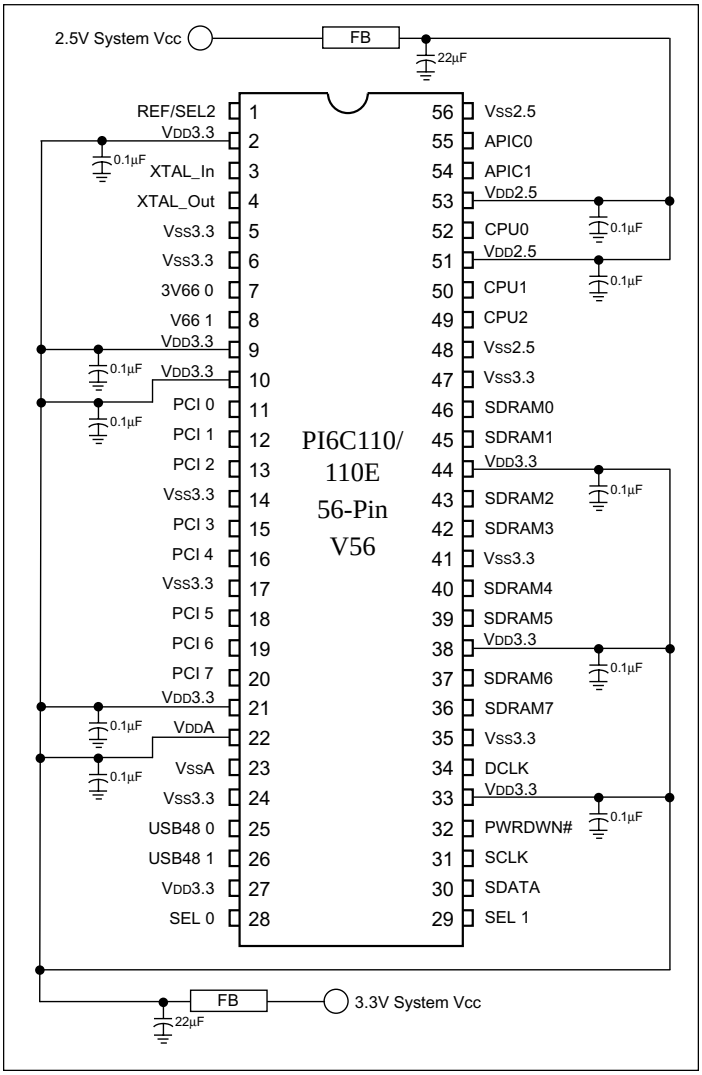


**Figure 1. PI6C110/110E Recommended Power Supply Schematic**

## Ground Plane Connection

All PI6C110/110E ground pins should be connected to the system ground plane. These connections should be as short as possible. Do not short individual ground pins together, always connect each separately to the ground plane.

## Crystal Oscillator Connection

An input reference clock is necessary for the PI6C110/110E to generate the required output frequencies. An internal crystal oscillator circuit used with a quartz crystal may be used to model a parallel resonant crystal oscillator circuit. It is recommended that a 14.31818 MHz parallel resonant crystal be used with the PI6C110/110E.

The crystal oscillator leads connected to the PI6C110/110E XTAL_In and XTAL_Out pins should be as short as possible because of the high impedance of the XTAL_In pin. This pin's high impedance characteristic results in the input being extremely sensitive to noise. To prevent inductive and capacitive coupling, no other clock signal should be routed close to the PI6CPI6C110/110E XTAL_In and XTAL_Out pins.

## Clock Outputs Connection

Depending on the length of the clock output line, one of the two termination schemes should be used.

### Short Clock Lines

Clock lines one inch or less in length can be connected directly from the clock output pin to the clock load. A series damping resistor is not required for short traces (one inch or less). Matching the output driver impedance plus the series damping resistor to the PCB trace is not necessary.

### Long Clock Lines

Clock lines one inch and longer must be treated as a transmission line. A series damping resistor must be used to match the impedance of the output driver plus the damping resistor to the PCB trace. Matching the impedance will minimize the EMI of the system and eliminate signal reflections back to the driver.

The clock line width should be chosen to produce a 60 Ohm trace impedance. The PCB trace width varies with the type of material used. Refer to Table 1 for the value of the series damping resistor.

**Table 1. Clock Output Buffer DC Characteristics**

| Buffer Name | Vcc Range (V) | Impedance (Ω) | Damping Resistor (Ω) |
|---|---|---|---|
| CPU, APIC | 2.375 - 2.625 | 22.4 - 37.5 | 22 - 36 |
| USB48, REF | 3.135 - 3.465 | 32.3 - 42.8 | 18 - 27 |
| SDRAM, DCLK | | 19.4 - 25.6 | 33 - 39 |
| PCI, 3V66 | | 27.2 - 34.9 | 24 - 33 |

## Checklist for Noise Reduction Techniques when Designing with Clocks

- ☐ If there are Op Amps in the design, terminate unused op-amps in dual and quad packs by grounding the positive input and connecting the – input to the output.
- ☐ Filter all signals leaving a noisy environment and filter all signals entering the board.
- ☐ Place I/O drivers near where they leave the board.
- ☐ Place the crystals flush to board and ground them.
- ☐ Place the clock at the center of the board, however, if the clock goes off the board, place the clock near the connector.
- ☐ Divide the circuits on the board based on their frequency and current switching levels.
- ☐ Separate noisy and quiet leads.
- ☐ Separate digital and analog lines and route the signals away from each other.
- ☐ Clock and digital signal lines must be placed as far away as analog input and voltage reference pins.
- ☐ Clock circuits must be placed away from I/O cables.
- ☐ The length of sensitive leads such as decoupling capacitors must be as short as possible.
- ☐ Use all power and ground pins of an IC.
- ☐ To cancel mutual coupling, twist noisy leads together.
- ☐ Place a ground lead between low-level signal leads and noisy leads in the same connector like a ribbon cable.
- ☐ Keep high-speed lines short and direct.
- ☐ Avoid running traces under the crystal.
- ☐ Sensitive traces should not be run in parallel with high current, fast switching signals.
- ☐ Critical traces should have wide trace width and must be guarded with a ground on each side of the trace.

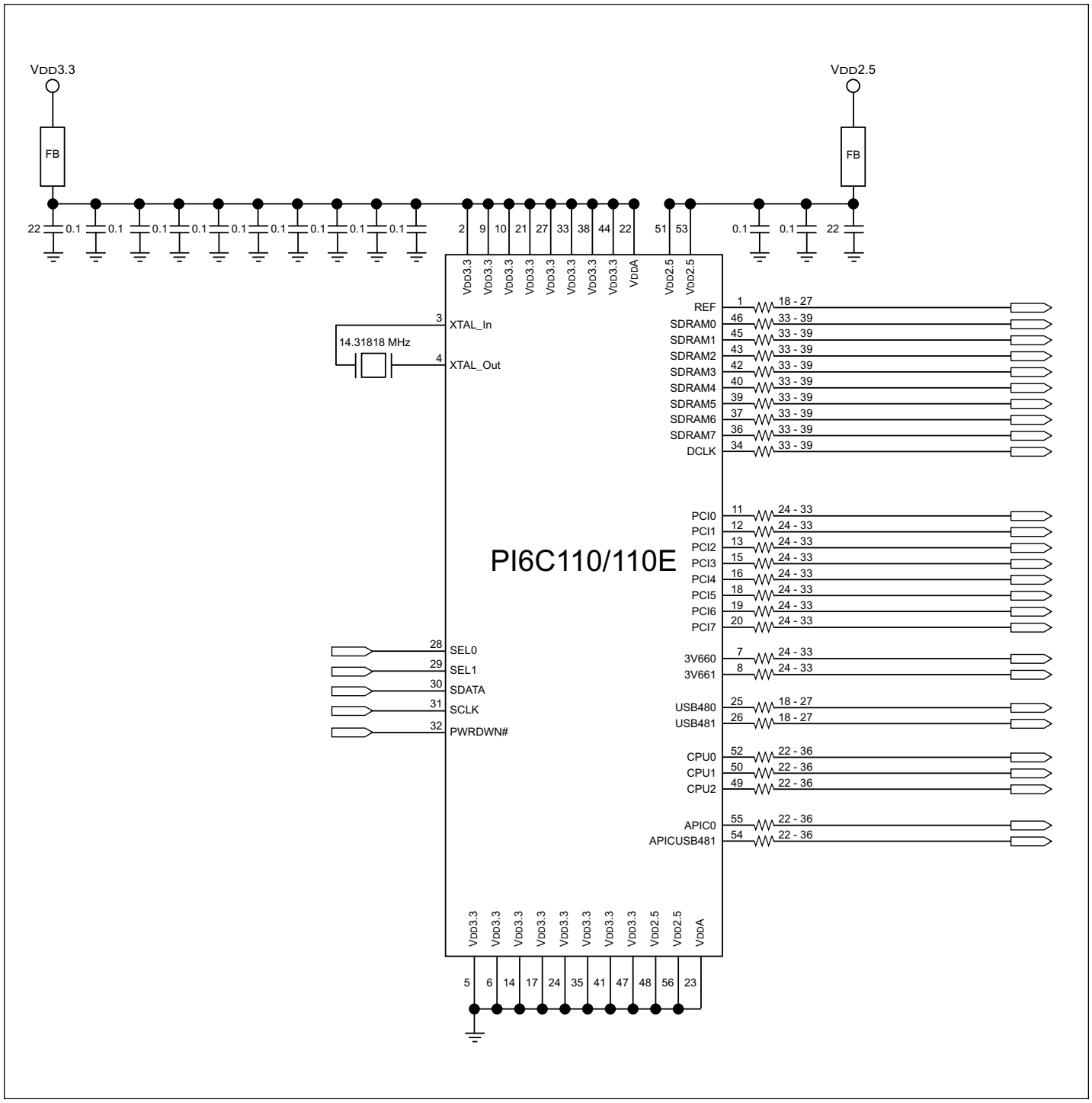


**Figure 2. PI6C110/110E Layout Schematic**