Managing Clock Distribution and
Optimizing Clock Skew in Networking Applications

by Cameron Katrai

Abstract

Today's high performance systems need low skew clock generation and distribution. Clock skew is defined as the difference in time between simultaneous clock transitions within a system. The skew has become the major part of constraints that form the upper boundary for the system clock frequency.

Reduction in system clock skew reduces cost by avoiding complicated architecture or faster logic. Phase Lock Loop-based clock distribution is becoming one of the most sought after solutions for creating low skew system designs. Pericom has developed the following set of low-skew PLL Clock Drivers: PI6C2501(3V), PI6C2308A (3V), PI6C2509A (3V), PI6C2510 (3V), PI6C5932 (5V), PI6C9910 (5V), and PI6C9930 (3V). They provide zero input-to-output delay using high-speed process and phase lock loop technology. In a 24-pin TSSOP package, the PI6C2509A supports Spread Spectrum modulation of timing signals and operates faster and consumes less space than alternative devices, providing significant improvements in performance and cost. PI6C2501(3V), PI6C2308A(3V), PI6C2509A/2510A(3V), PI6C5932(5V), PI6C9910(5V), and PI6C9930(3V), provide the lowest phase error over all frequencies and introduce no additional jitter as a result of Spread Spectrum modulated input clock signal. It is these features that allow Pericom's PLL clock drivers to support stringent input-to-output delay (150ps) and output-to-output skew less than 200ps.

Introduction

Better Clock distribution strategies using PLL clock drivers have made a significant contribution to high-performance system design. If clock distribution networks are not properly constructed, they may detract from system-level performance. This application note defines the skew in a system, describing its effect on performance. Recommendation and supporting analysis are given for designing near optimal clock networks.

This note also illustrates that clock network design can be a surprisingly complex task involving many tradeoffs.

Clock networks must be designed to minimize skew or the differences in delay throughout a clocking network. It is ideal that every component, such as sequential elements, i.e. flip-flops and latches, that need clocking, should receive the edge of the clock at the same time within each clock period. Fully synchronous designs require this methodology. Synchronous designs are highly recommended since they can tolerate higher clock rates and are easier to perform timing analysis.

To ensure that the network operates as closely to the ideal as possible, the skew must be minimized along the entire clocking network. This ensures that all sequential elements see a common clock edge. For any design with more than 100 flops and latches, Pericom strongly suggests some form of clock tree structure for clocking. Buffer delays and wiring delays are the two most significant factors contributing to skew. The clock topology can significantly contribute to skew. As will be discussed, a good clock network must balance factors such as skew and clock tree delays. In the next section a real clock design is examined for analysis of clock skew.

Design Example

Both the delay in the data path and the clock skew affect data transfer from one section of the design to the other sections. The data path delay is defined as the delay from a register (F1) in a section to the D input of another register (F2). Figure 1 depicts this delay. The delay includes CLKA to Q1 and set up hold time at point B.

The clock skew or Tskew is the difference between a rising edge on CLKA in F1 and CLKB in F2. The Tskew defines both the positive and negative skew. Positive skew affects data transfer from a hold time standpoint. Negative skew affects data transfer from a set up time standpoint. If the data path from F1 to F2 is too long, a set up time violation is realized on F2. Clock skews also affect the set up and hold time. A more practical and realistic clock distribution is shown in Figure 2.
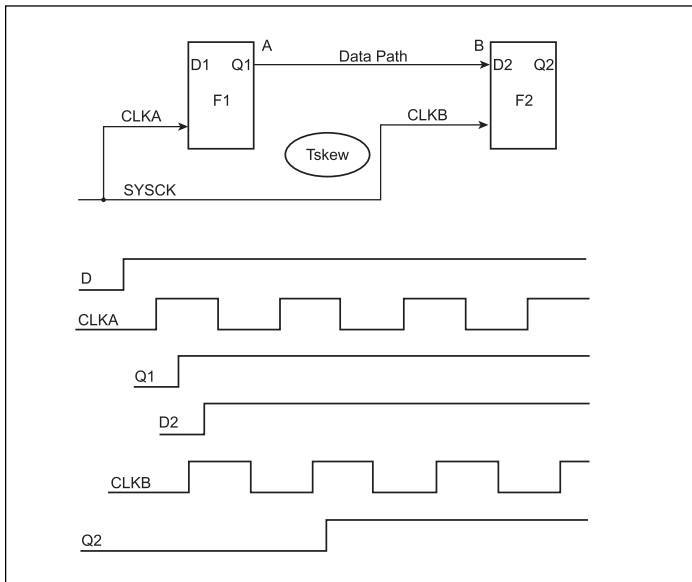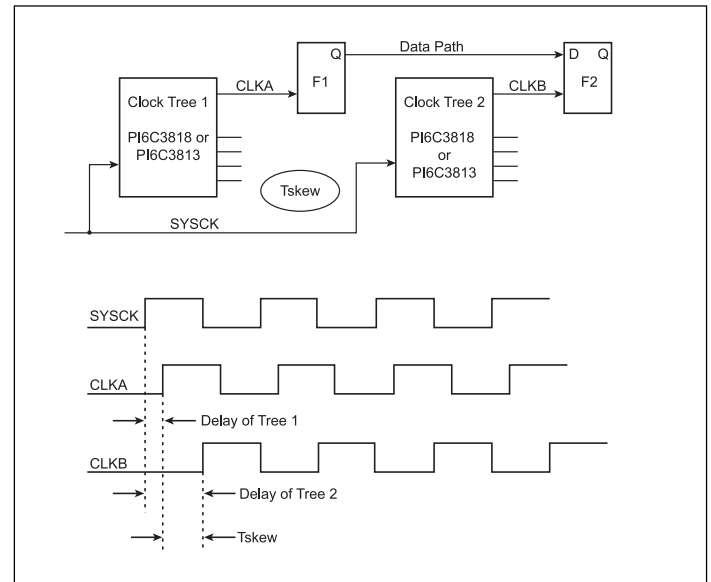
Figure 1. Data Path Delay

Figure 2. Practical and Realistic Clock Distribution

Buffers are used as Clock Trees to distribute the clock throughout the system. Clock trees introduce a third delay into the design that can cause problems. PLL clock buffers are included to eliminate this additional delay as shown in Figure 3.

PLLs, which can provide skew management to help compensate for clock tree delays, can also be added to each section to reduce the effects of Tree delay differences and help manage skew from chip-to-chip. The PLL synchronizes the rising edge on SYSCK so that it will be simultaneous with a rising edge on flop ck (Figure 3). If the PLL is used on each section, all flop ck signals on each section will be simultaneous within the error of the PLL. The PLL will compensate for differences in delays from section to section.
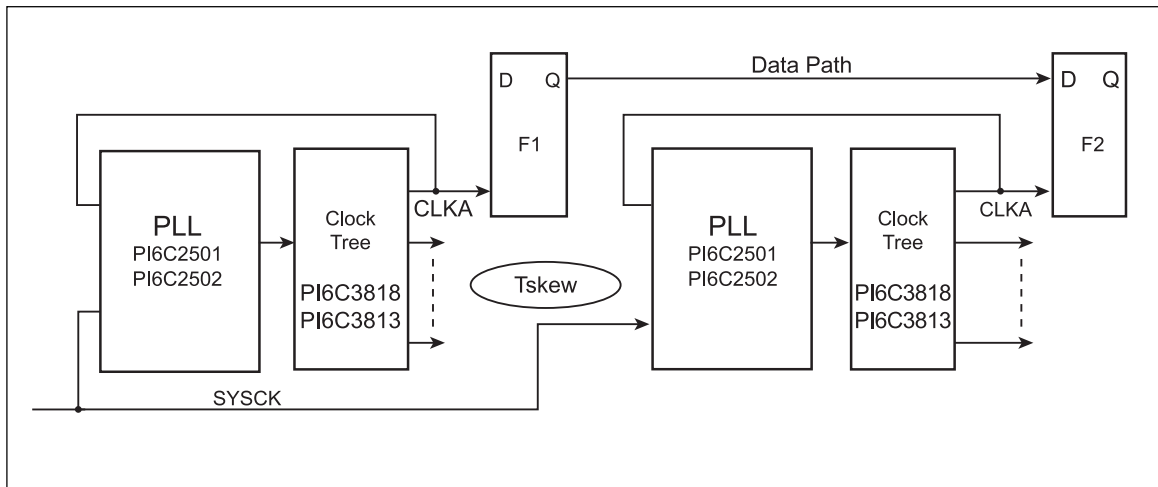

Figure 3. Synchronize the Rising Edge on SYSCK

PI6C2501 Clock Driver

The PI6C2501 features a low-skew, low-jitter, phase-lock loop (PLL) clock driver (see Figure 4). By connecting the CLKOUT output to the feedback FBIN input, the propagation delay from the CLKIN input to any clock output will be nearly zero.

Product Features

· Allows Clock Input to have Spread Spectrum modulation for EMI reduction

· Zero Input-to-Output delay

· Low jitter: Cycle-to-Cycle jitter ±100ps max.

· On-chip series damping resistor at clock output drivers for low noise and EMI reduction

· Operates at 3.3V Vcc

· Packaged in Plastic 8-pin SOIC Package (W8)
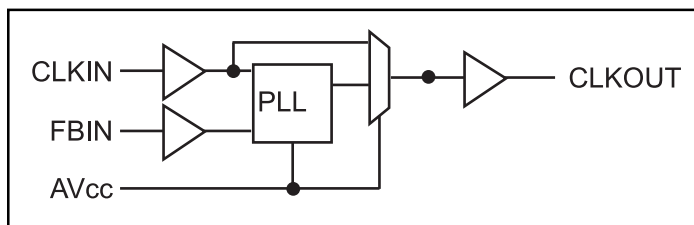
· Wide range of Clock Frequencies

Figure 4. PI6C2501 Block Diagram

Figure 5. Block Diagram

PI6C2308A Product Features

• Zero input-output propagation delay
• Input-to-output skew less than 150ps (Cypress is 250ps)
• Output-output skew less than 200ps
• Device-device skew less than 300ps (Cypress is 700ps)
• Two banks of four outputs (Three-Stateable)
• 10 MHz to 134 MHz operating range
• Low jitter, less than 100ps cycle-cycle (-1, -1H, -4)
• Space-saving 16-pin TSSOP (-1H only) & 150-mil SOIC pkg.

Providing two banks of four outputs, the PI6C2308A and PI6C2308 are 3.3V zero-delay buffers designed to distribute clock signals in applications such as PCs, workstations, datacom, telecom, and high performance systems. Each bank of four outputs can be controlled by the select inputs.

With much better electrical characteristics, the PI6C2308A provides 8 copies of a clock signal that has 150ps phase error compared to a reference clock. The skew between the output clock signals fo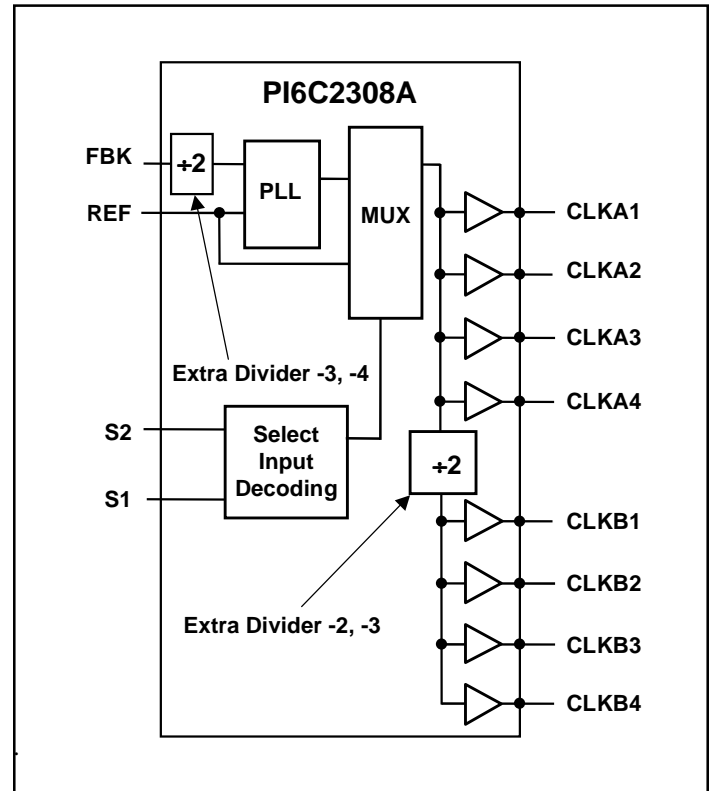r PI6C2308A is less than 200 ps. When there is no rising edge on the REF input, the PI6C2308/A enters a power-down state. In this mode, the PLL is off and all outputs are three-stated resulting in less than 50µA of current draw.

Base part, PI6C2308/A-1, provides output clocks in sync with a reference clock. For designs requiring faster rise and fall times, PI6C2308/A-1H is the high-drive version of the PI6C2308/A-1. Depending on which output drives the feedback pin, PI6C2308/A-2 provides 2X & 1X clock signals on each output bank. PI6C2308/A-3 provides 4x and 2X clock signals on the output. PI6C2308/A-4 provides 2X clock signals on all outputs. PI6C2308/A allows bank B to be Three-stated if all output clocks are not required. For testing purposes, the select inputs connect the input clock directly to outputs.

For zero delay operation, PI6C2308A has an open feedback path that is easily closed (by driving any output into the FBK pin, see Figure 5). By adjusting the feedback path, other interesting applications can be achieved
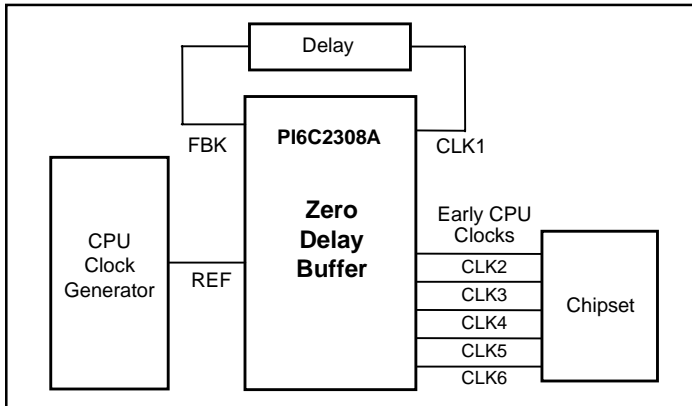
Figure 6. Zero Delay Operation

Of interest is the generation of "Early" Clocks using a discrete delay element in the feedback path. Outputs can then lead the input signal. These outputs are "Early"compared to the input clock. Certain chipsets require some copies of the host clock, which are early compared to the rest of the host clock's copies. Figure 6 shows such application.

By placing an N divider in the feedback path (see Figure 7), a designer can adjust all outputs to run at a frequency that is XN times in the input frequency. Whatever the multiplication factor, input and output frequencies must be in the 10-130 MHz range, which means the divider cannot be larger than 13.
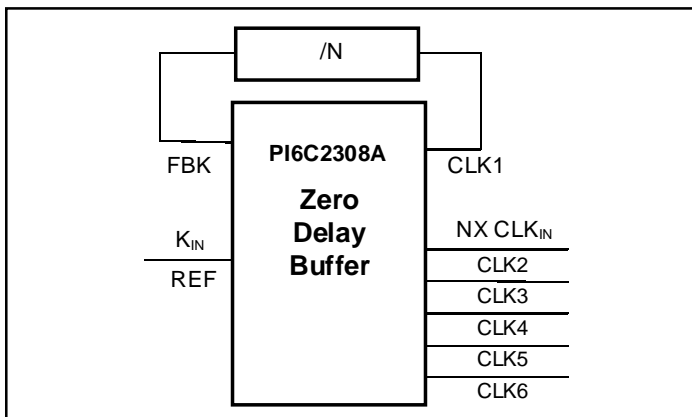

Figure 7. N Divider in Feedback Path

The PLL compares the phase of two signals: phase of FBK pin at a threshold of vdd/2 with that of the REF pin at the same vdd/2 threshold. Transition of all the outputs are at the same time. This also includes the output driving FBK. By changing the load on a specific output, the designer is able to change the rise time of that output and therefore change the time it takes for that output to get to vdd/2 threshold relative to when REF input reaches the vdd/2 threshold. Notice that the zero-delay buffer will always adjust itself to keep the vdd/2 point of the output at zero delay from the vdd/2 point of reference.

The result is that outputs can be advanced by loading this output more heavily than the others or outputs can be lagged by loading this output less heavily than the other (see Figure 8).
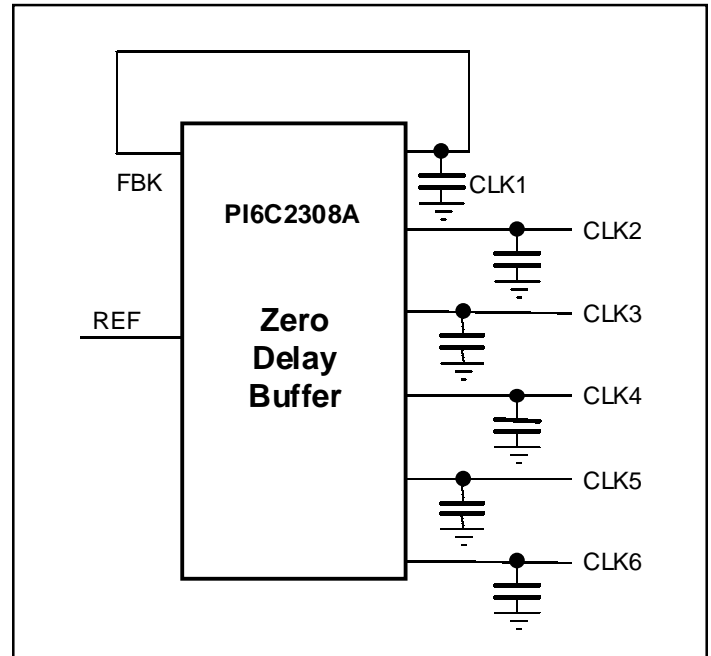

Figure 8. Zero Delay Buffer

Figure 9 shows a situation where output clock 1 has a larger load. Because the PLL adjusts itself to position the zero skew between the REF and the feedback pin, REF and CLK1 both cross Vdd/2 at the same time. But, since the other output clocks are less loaded, their rise time is faster than CLK1. Consequently, they advance the REF by a certain amount that can be controlled by the amount of the loads.
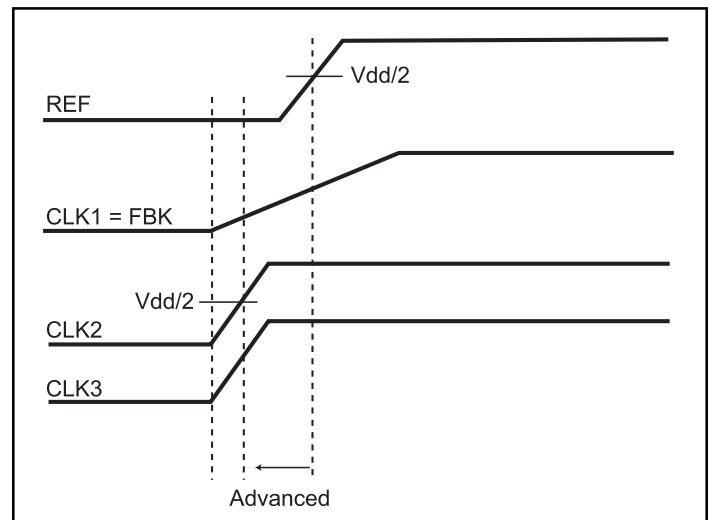

Figure 9. Output Clock

The timing diagram (see Figure 10) shows a situation where the other output clocks are loaded heavier. Notice that the PLL adjusts itself so that both REF and the feedback clock cross the VDD/2 at the same time. However, since the rest of the clocks have heavier loads, they are delayed by a certain amount that is controllable by the loads.
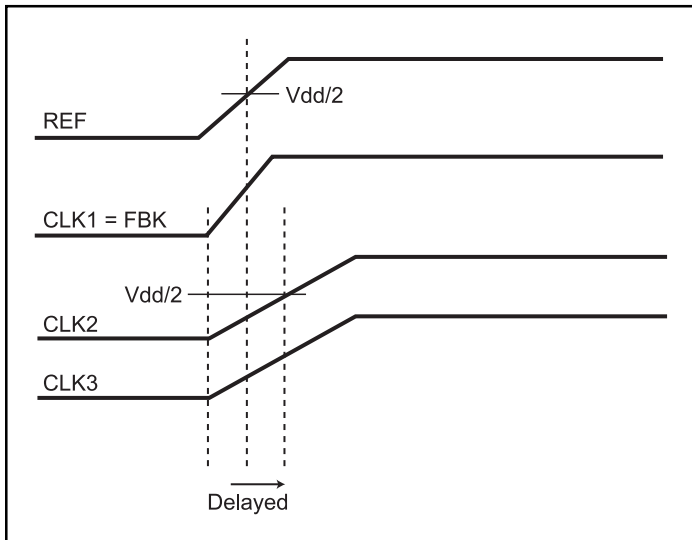

Figure 10. Timing Diagram

Many systems use both 5V and 3.3V supplies. Figure 11 shows how to make a 3.3V clock out of a 5V clock using a zero-delay clock. High-energy Electromagnetic Fields (EMF), caused by high-frequency switching signals travelling around the system, cause Electromagnetic Interference (EMI) and Electromagnetic Coupling (EMC). Long transmission lines distributing these high-frequency signals are an automatic cause of EMC and EMI. A good technique to control EMI and EMC is to reduce the actual energy of the high frequency signal. PI6C2308A can be used to accomplish this. As shown, it is used to convert 5V clock signals into 3.3V clock signals on the output. Instead of 5V signals, these 3.3V signals are distributed over long transmission lines. Hence the energy in the generated EMF is substantially reduced. The output of the PI6C2308A is 3.3V, swinging rail to rail, making it 5V TTL compliant. Hence at the load, it can be driven into a 5V device. The only requirement here is the presence of a 3.3V supply.
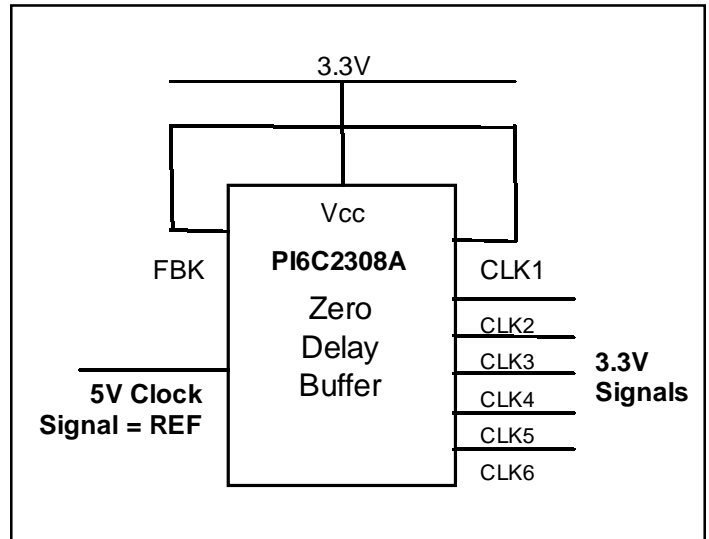

Figure 11. 5V Input Tolerant

By ganging multiple outputs together, the output skew can be dramatically reduced. This method can also increase the drive, as illustrated in Figure 12.
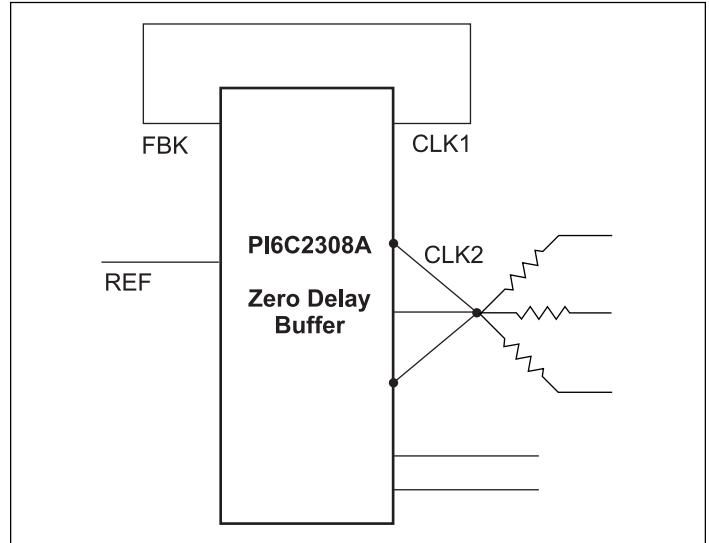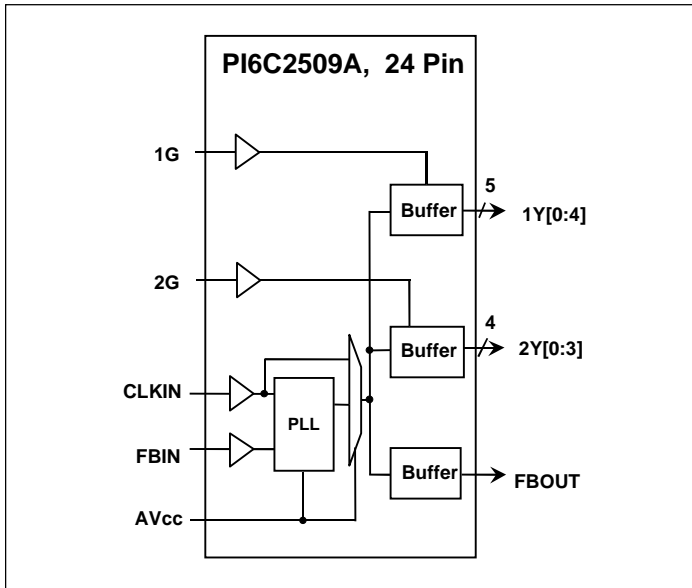

Figure 12. Ganging Outputs

Figure 13. 3.3V Zero Delay, PLL Clock Driver

PI6C2509A Product Features

- Meets Intel Specs for PC100
- Input to Output skew less than 150ps
- Skew less than 200ps
- Jitter less than 100ps
- For 100 MHz SDRAM DIMM module
- Operating Frequency up to 134 MHz
- Reference Clock Input tolerates severe undershoot/overshoot
- Multiple Vdd and Vss pins for noise reduction

The PI6C2509A/2510A allows zero phase and frequency clock distribution for PC100, and are the same PC SDRAM Registered DIMM Specification with PC bus speeds of up to 100 MHz. Zero Delay Buffers distribute multiple clock signals with very low skew between outputs and zero delay. The PLL is fed a reference input and a feedback input that is actually one of the outputs (see Figure 13). The phase detector in the PLL circuit adjusts the output frequency of the VCO so that the two inputs have no phase difference. Pericom's PI6C2509A has many modes of operation, that aid the designer to achieve power consumption reduction, to minimize EMI, and for troubleshooting.

By disabling a bank, the output clock is pulled down to a low state. The enable disable feature allows a method of disabling all or part of the clock output without PLL restoration. This feature allows preservation of signal integrity and allows reducing power consumption and radiate emissions. Additionally, the PLL can be disabled to place the chip in a bypass test mode in which the input clock is buffered directly to the output and the output clock is only delayed by the output buffer. Jitter characteristics and phase differences created by the PLL can also be analyzed by enabling and disabling the PLL and by comparing the characteristics. The PI6C2509A can generate an early clock. This allows the clock edge to arrive at the loads at the same time the clock arrives at the clock buffer input. This is achieved by matching propagation delay of the feedback line with the propagation delay of output to load.

PI6C9930 Product Features

- Seven Copies of REF Input Plus One
  REF x 2 or Seven Copies of REF Input Divided by 2
- SDRAM Timing
- Compatible with PCI 3V Interface
- Skew Less than 0.25ns
- 50 Percent Output Duty Cycle
- Low Noise Balanced Drive Outputs
- Better than 1V/ns slew rate

PI6C9930 is a 3.3V, Low-Skew Clock Buffer providing low-skew system clock distribution. This multiple-output clock driver optimizes the timing of high-performance computer systems.

The completely integrated PLL allows "zero delay" capability. External divide capability, combined with the internal PLL, allows distribution of a low-frequency clock that can be multiplied by virtually any factor at the clock destination (see Figure 14).
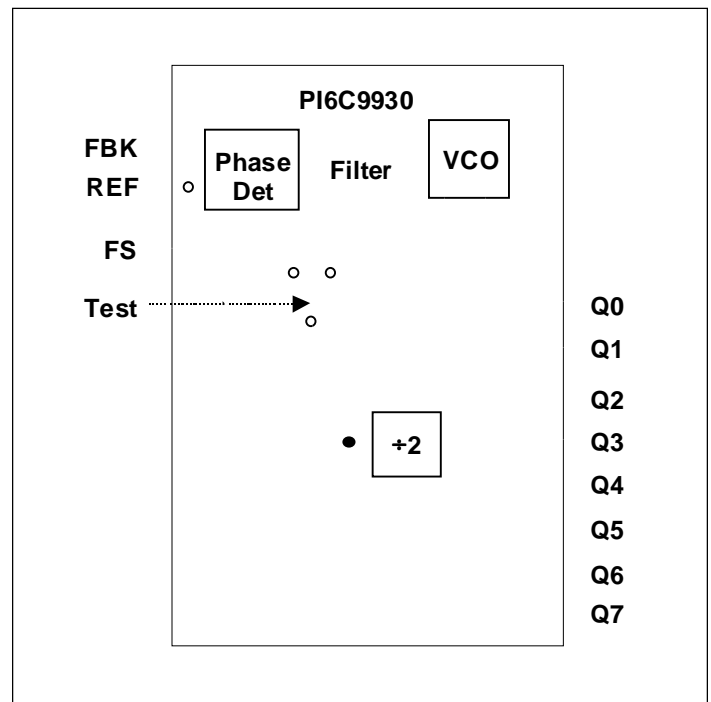

Figure 14. 3.3V Zero Delay, PLL Clock Driver
Compatible with PCI 3V Interface

The PI6C9910 provides 8 zero-delays with skew less than 250ps for clock outputs to a reference clock input (see Figure 15). Operating in the range of 15 to 80 MHz, the PI6C9910 is an excellent clock driver for high-performance computing and networking systems. At the heart of PI6C9910 is a state-of-the-art PLL that generates a clock that is completely in phase with the reference input clock. There are two devices in PI6C9910 family: the PI6C9910-5 and the PI6C9910A. The PI6C9910-5 has high-drive outputs designed to drive 30pF capacitance. Since the typical input capacitance of a CMOS device is 7pF, PI6C9910-5 is capable of driving 4 CMOS devices. The PI6C9910A's balanced drive output significantly reduces output drive currents that results in a reduction in under-shoot and overshoot. In situations where the driver output has to drive more than one receiver, the balanced drive can help. In these examples, the lines are high impedance; however they are poorly terminated. Balanced drive output also helps in situations where the lines are properly terminated and the output drives only one receiver. The PI6C9910 device is available in space-saving 24-pin SOIC and SSOP packages.
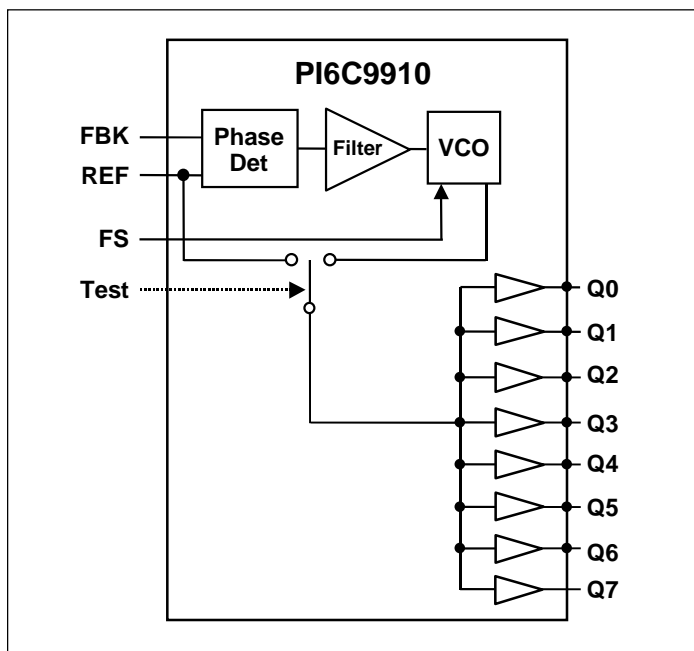

Figure 15. PI6C9910 Block Diagram

PI6C9910 Product Features

- Eight zero-delay, low-skew copies of REF input
- PCI Applications, PCI-to-PCI bridge timing
- Skew Less than 0.25ns
- 50 Percent Output Duty Cycle
- Low-Noise Balanced-Drive Outputs (PI6C9910A) and High-Drive Outputs (PI6C9910-5)
- Better than 1V/ns slew rate

The PI6C5932 provides six low-skew (<250ps) clock outputs (5Q and Q/2) to a reference clock input (see Figure 16). The PI6C5932 is an excellent clock driver for high-performance computing and networking systems. It provides features such as ±24mA Balanced Drive Outputs, a PLL bypass feature for low frequency testing, an Internal VCO/2 option for wider frequency range, and outputs for Tri-state and reset while OE LOW. The PI6C5932 extends Pericom's popular SiliconClock product line of PLL-based zero-delay clock generators to 100 MHz. PI6C5932 is pinout compatible with QS5930 designs. Both clocks, PI6C5932 and PI6C5930, accept a less than perfect clock signal, clean it and buffer it via six balanced drivers for distribution to multiple loads. They can also be configured as a frequency doubler to boost clock speed. Clock skew between any two output drivers for both devices is < 250ps.

PI6C5932 Product Features

- 100 MHz operation
- Low skew (<250ps)
- Small Footprint
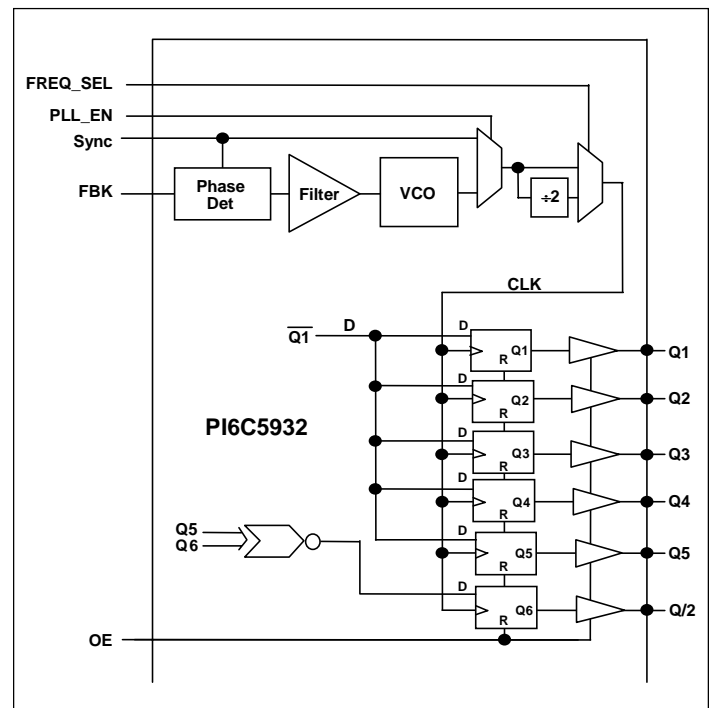 QSOP-20 Package
- Balanced drive outputs (±24mA)

Figure 16. PI6C5932 Block Diagram

5V Pericom Clock Drivers, and PLL Buffers

5V Drivers										
	Inputs	Output per Input	Inv	Skew	I2C	SDRAM CLK	3.3/5V	5V In Tol	# PLL	Package/Pin
PI49FCT804T	2	4	No	.8ns	No	NA	5	NA	NA	P16/S16
PI49FCT805T	2	5	No	.5ns	No	NA	5	NA	NA	H20/P20/S20/Q20
PI49FCT2805T	2	5	No	.5ns	No	NA	5	NA	NA	H20/P20/S20/Q20
PI49FCT806T	2	5	Yes	.5ns	No	NA	5	NA	NA	H20/P20/S20/Q20
PI49FCT807T	1	10	No	.35ns	No	NA	5	NA	NA	P20/S20/Q20/H20
PI49FCT2807T	1	10	No	.35ns	No	NA	5	NA	NA	P20/S20/Q20/H20
PI49FCT811T	1	10	Prog	.5ns	No	NA	5	NA	NA	P24/Q24/S24
5V Zero Delay Buffers										
PI6C9910	1	Q0-Q8	No	0.25ns	No	Yes	5	NA	1	S24/H24
PI6C5930	1	Q/2 & (Q0-Q4)	No	0.25ns	No	Yes	5	NA	1	Q20

3.3V Pericom Clock Driver, and PLL Buffers

3.3V Drivers									
	Inputs	Output per Input	PC/Note	Inv	Skew	3.3/5V	5V In Tol	# PLL	Package/Pin
PI49FCT3804	2	4		No	.8ns	3.3	Yes	NA	S16
PI49FCT3805	2	5		No	.5ns	3.3	Yes	NA	H20/P20/S20/Q20
PI49FCT3806	2	5		Yes	.5ns	3.3	Yes	NA	H20/P20/S20/Q20
PI49FCT3807	1	10		No	.35ns	3.3	Yes	NA	P20/S20/Q20/H20
PI6B3904	1	6		No	.35ns	3.3	Yes	NA	P20/S20/Q20/H20
PI6C3818A	1	18	PC	No	.25ns	3.3	No	NA	V48 (SSOP)
PI6C3810A	1	10	Note	No	.25ns	3.3	No	NA	H28(SSOP)
PI6C3813A	1	13	PC	No	.25ns	3.3	No	NA	H28(SSOP)
PI6C3807A	1	7	Note	No	.25ns	3.3	No	NA	Q20
PI6C3805A	1	5	Note	No	.25ns	3.3	No	NA	Q16
3.3V Zero Delay Buffers									
PI6C9930	REF	Q0 & (Q1-Q7)/2		No	.25ns	3.3	No	1	S24/H24
PI6C2509	1	1:09		No	0.2ns	3.3	No	1	24 TSSOP
PI6C2510	1	1:10		No	0.2ns	3.3	No	1	24 TSSOP
PI6C509	1	1:09		No	0.2ns	3.3	No	1	24 TSSOP
PI6C2308A	1	2x(1:4)		Yes	0.2ns	3.3	Yes	1	16 TSSOP and SOIC
PI6C2501/2	1	1:1		No	0.2ns	3.3	No	1	8 SOIC
PI6C2504	1	1:4		No	0.2ns	3.3	No	1	16 SOIC

Summary

The topology of a clock net can significantly contribute to skew if it becomes long and convoluted. Even after considering and balancing the effects of buffer delays, fanout, wire lengths, and topology, small amounts of delay variations are possible. PLL clock drivers are the best way to eliminate skew and provide synchronous designs. The PI6C2501(3V), PI6C2308A(3V), PI6C2509A/ 2510A(3V), PI6C5932(5V), PI6C9910(5V), and PI6C9930(3V) have many modes of operation that aid the designer to reduce power consumption, minimize EMI, and for troubleshooting. The enable disable feature permits disabling of all or part of the clock output without PLL restoration.

Operating in the range of 10 to 100 MHz, the PI6C180 is a high fanout Clock Buffer with 18 outputs, I^2C for disabling individual clocks, and EMI reduction support. Pericom is the leading provider of advanced interface solutions for personal computers including Bus Switches, Analog Switches, and Logic Devices. As system performance continues to expand to ever increasing frequencies and beyond, high-performance clock drivers and generators are essential to sustain improved system performance. Pericom clock technology provides new levels of price performance for PC clock systems.

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