Application of Zero Delay Buffers in Switched Ethernet

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Abstract

With the best and tightest characteristics of any PLL driver, Pericom's collection of Zero Delay Clock Drivers have found applications in high-performance networking systems providing clocking for devices such as FPGAs, CPUs, Switching Devices, and Controllers. They provide the best characteristics in terms of tight specification on skew, jitter, and phase error. The PI6C9930 (3V), PI6C2308A (3V), PI6C2501 (3V), PI6C2509A (3V), PI6C2510A (3V), PI6C5932 (5V), and PPI6C9910 (5V) provide multiple copies of a reference clock driven using state-of-the-art PLL (phase-locked loop) technology. To meet both the margins required in timing and synchronized clocking for i960 Bus and DRAM Controller FPGA in a Switched Ethernet application, the clock buffer must provide de-skewed clock signals. Pericom's PI6C2501, PI6C2308A, and PI6C2509A, for example, provide from one to nine clock outputs with less than 200ps skew between them and 150ps delay from input to output.

Introduction

Switched Ethernet versus Repeater

Before the introduction of Switching Hubs, the nature of limitation in repeaters was related to the nature of shared access; when one user talks, everyone listens. In a switching system, messages pass only to those clients who need them. The most important point about a Switch is that it only sends packets where they need to go. In contrast, a repeater forwards all packets to all links, wasting a lot of bandwidth. The main advantage of a switch is its ability to simultaneously receive multiple packets. A repeater cannot.

A repeater blocks the traffic by sending the data to all ports. While the Switch keeps the other lines clear, it can simultaneously receive data on many ports. Transferring all packets into memory inside the Switch does this. This application note discusses the use of Zero Delay PLL buffers in Switched Ethernet Systems and explains the block diagram of a Switched Ethernet system. A description of each member of the system and the use of Zero Delay PLL, in conjunction with the application, follows. This note also focuses on providing completely deskewed (zero delay) clocks for higher speed systems (80 MHz or more) using a PLL driver such as the PI6C2501 combined with a Buffer such as the PI6C3813A.

Switch Analysis

Switched Ethernet makes the hub intelligent by reducing the number of ports to which data is repeated. A switching hub is more intelligent in processing data. The hub basically buffers the data packets that are returned as a result of simultaneous transmission (collision). Although there is a delay resulting from buffering, with a switching hub, the two packets can now be transmitted in parallel. A switching hub must maintain two buffers or queues for each of its parts. These are the input buffers and output destination. The packets in a port's input buffer are analyzed and then copied to the destination port's output buffer. To rout a packet, the destination address of a packet is compared against the known device addresses. The packet is then entered in the destination port's output buffer.

The Hub can discard packets it receives when the switching hub's buffer memory is exhausted. This will cause those packets to be transmitted at a later time. When a packet is discarded, the upper layer network protocols detect a missing packet and request retransmission. A switching hub with a large buffer memory is more efficient. Figure 1 depicts the block diagram of a Switched Ethernet Hub. The design is based on Galileo Technology GT-48001 Switched Ethernet Controller and the i960 processor from Intel. While the GT-48001 provides the Ethernet Switching functions (inside the 8-port Switch), the i960 processor from Intel provides the network management and control function. The block diagram of the 8-Port Switch is shown in Figure 2.

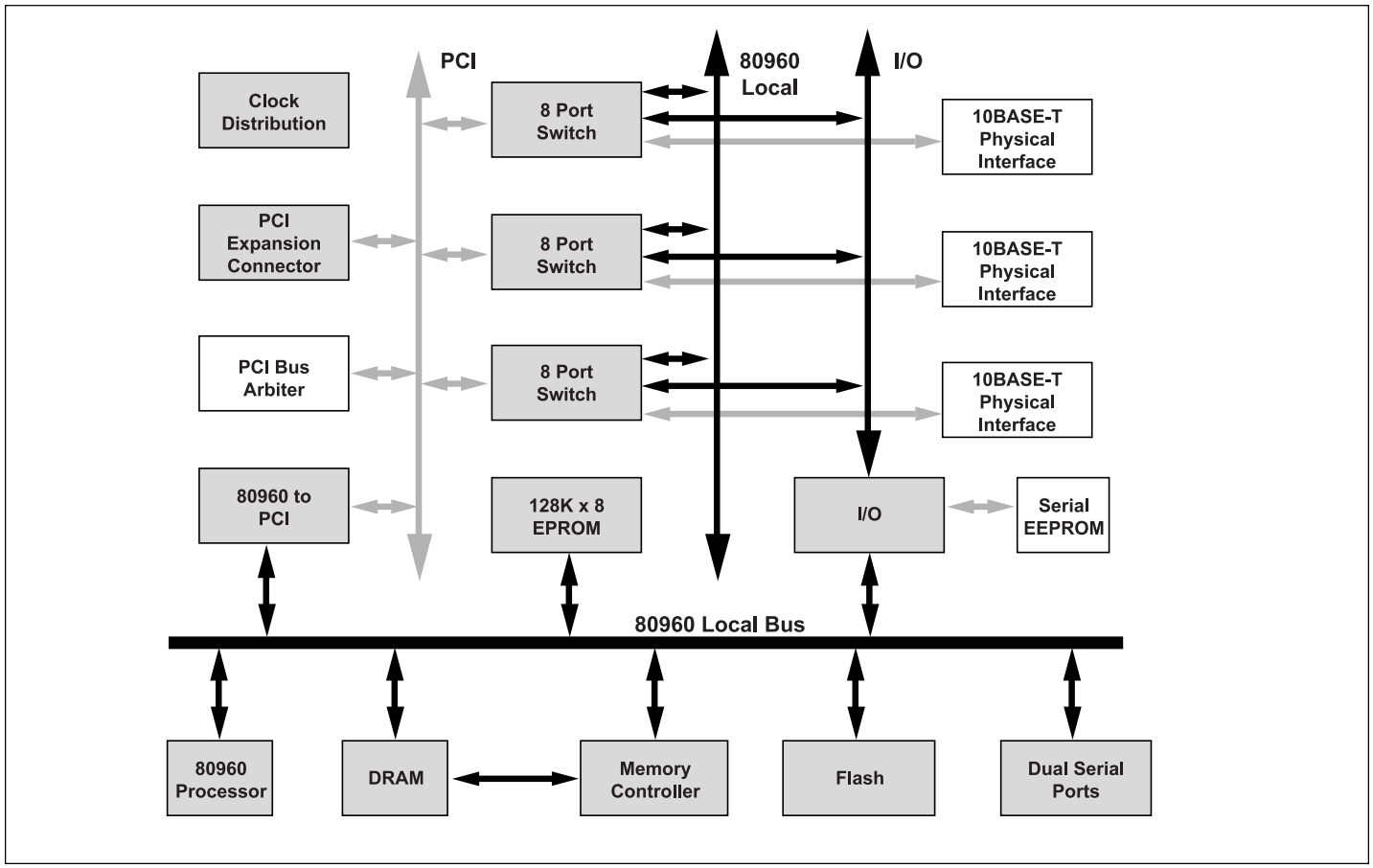

Figure 1. Switched Ethernet Hub

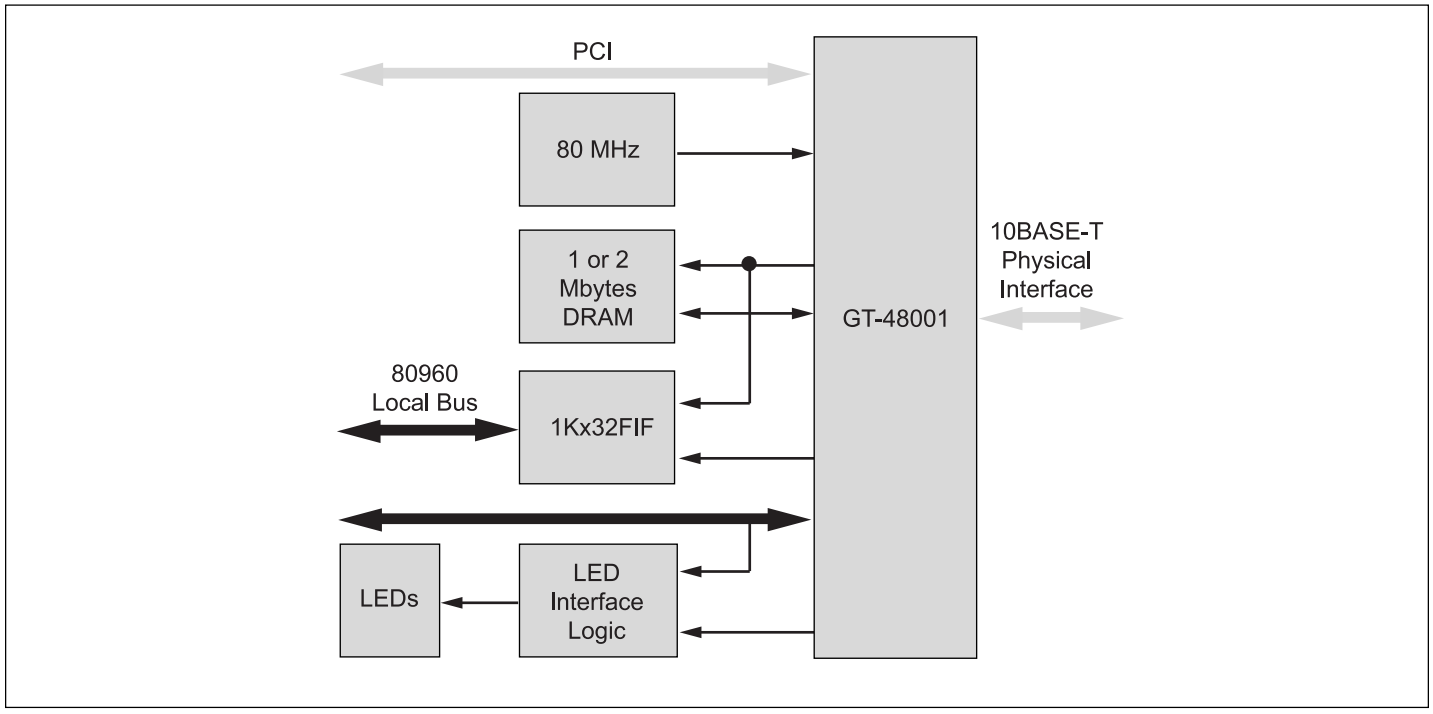

Figure 2. Eight-Port Switch Block Diagram

Description of Block Diagrams

A typical Switch Ethernet board requires clock signals for the PCI Bus, Processor Bus, DUART (AM85C30) PCLK, and DUART Bus Rate Generator. A low-skew clock driver such as the PI6C38013A provides 13 low skew outputs with a maximum output skew of 0.2ns. This is almost 1/10 of the PCI spec requirement. The PCI bus interface is used to exchange data between the SEC chips and the i960 processor. Most signal connecting devices that use a PCI interface are point-to point whose signals are request, grant, and clock.

The PCI Bridge chip allows devices on the PCI bus to access the processor bus and, for the processor, to access the PCI bus. PCI Arbiter determines which PCI device has access to the bus. Arbitration function is usually done with an FPGA device. A PCI expansion connector is provided to allow other PCI-based devices to be installed. The GT48001 is a high-performance, low-cost Switched Ethernet Controller that provides packet switching functions between eight on-chip 10/20 Mbps Ethernet ports and one Gbps PCI backplane.

The GalNet Switching Architecture is based on a proprietary messaging protocol using the industry standard PCI bus as medium. These devices are designed to connect seamlessly allowing packets to be switched between devices without process intervention. Each device acts as an intelligent agent, sharing information between all other devices in the system. When one device learns a new address, it automatically updates all other devices via the New-Address message. The 48001 integrates eight Ethernet ports. Each port works at 10 Mbps (half duplex) or 20 Mbps (full duplex) and includes the media Access Control (MAC), Manchester Encoder/decoder, link integrity logic, auto polarity logic and LED interface. The 48001 can recognize up to 8,000 different unicast MAC addresses.

Clocking at 30 MHz

Figure 3 illustrates only part of the clocking required. Switched Hub requires deskewed clock signals for the PCI Bus, Processor Bus, DUART (AM85C30) PCLK and DUART Baud rate Generator. According to PCI specification, PCI Clock must be distributed with a maximum clock skew of 2ns between any two components. To satisfy this requirement, Pericom suggest a low skew clock buffer such as PI6C38013A.

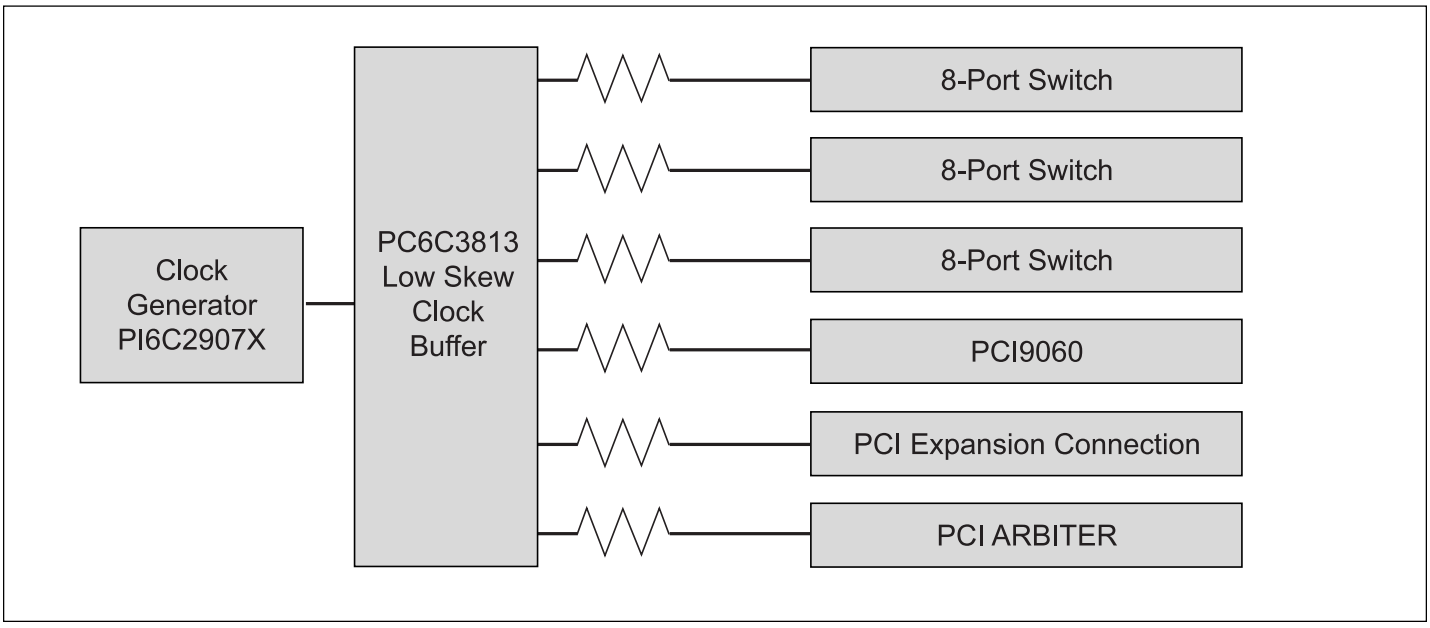

Figure 3. Clock Distribution

The PI6C3813A provides thirteen low skew clocks with maximum output skew of .2 ns. PI6C3813A already includes a series resistor, however, to further reduce ringing the design engineer may add additional damping resistors. Pericom makes a range of custom made Clock Generators (PI6C2907X) that can satisfy Switched Ethernet requirements. Please contact a Pericom Application Engineer for your requirement.

To implement the remaining clock distribution, the same PI6C3813A is used as shown in Figure 4.

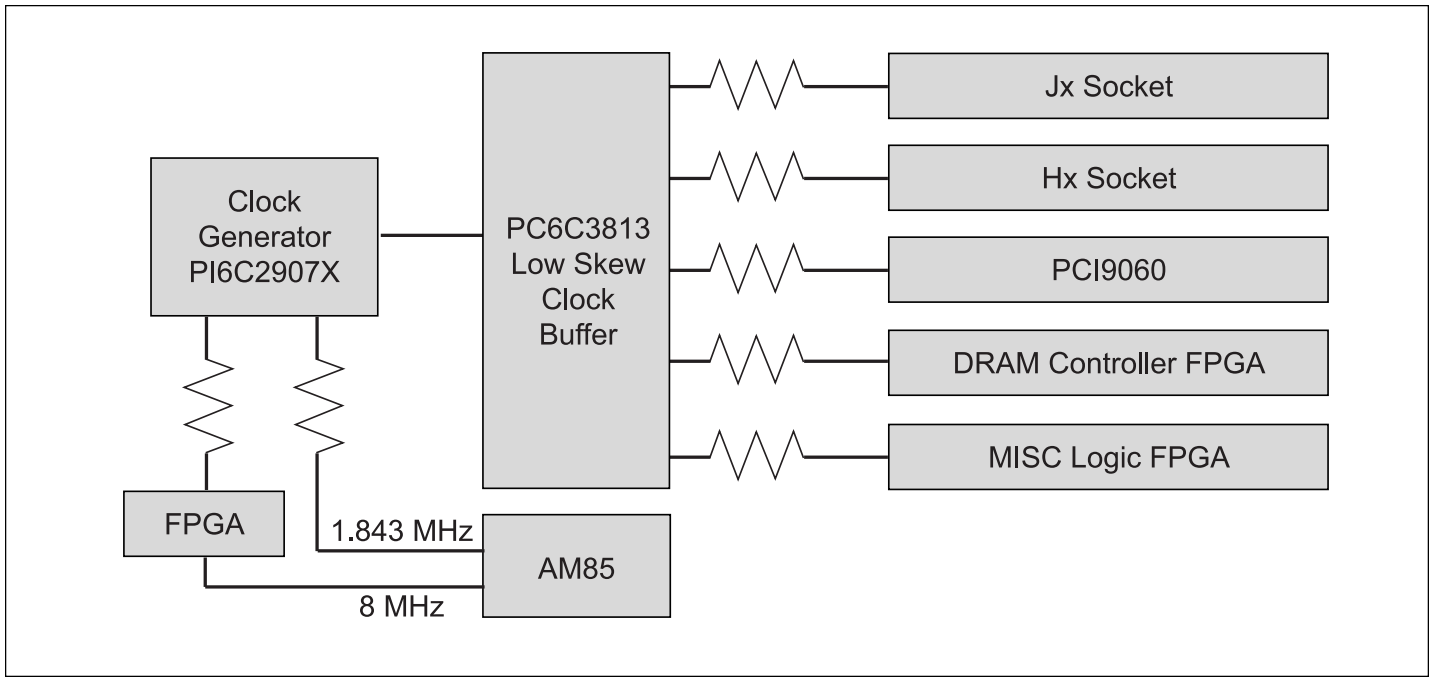

Figure 4. Clock Distribution (continued)

As shown in Figure 4, the same clock driver can be used to distribute the clock signal to the processor, PCI Bridge, and FPGA devices.

The Need for Zero Delay PLL Clock Drivers

The application described above uses a non zero delay clock buffer such as PI6C3813 for clock distribution. In higher performance systems where the clock may run at speeds exceeding 80 MHz, the clock requirement is more stringent. Because of tight timing margins, the delay through the clock driver can not be tolerated. These timing margins relates to DRAM Controller FPGA read and write, transceiver, Misc Logic FPGA, I/O port control, DUART and EPROM. Transceiver requires the tightest skew. Even at 30 MHz a margin of 1ns is very realistic.

An Example of Timing Margin Analysis

The time it takes for the transceiver outputs to be disabled is the critical timing parameter. During the address cycle, before the processor starts driving the bus, the transceiver output should be disabled. Table below shows the Bus Transceiver Timing Analysis.

Table 1. Example of Timing Margin Analysis

Parameter	Value	Units
Optimal Time (one clock cycle)	30	‘ns min
Clock Skew	2 (PCI Spec)	‘ns min
Transceiver Output Disable Delay	14	‘ns min
Input Output # Delay	13	‘ns max
Margin	1	‘ns

In addition, since the i960 bus is a synchronous bus referenced to the processor clock input, the devices interfaced to the bus (or their controllers) need to receive the clock at the same time the processor does. Zero Delay PLL drivers can provide the necessary clock for these requirements. It can be shown that by combining a very inexpensive Zero Delay Clock Driver such as PI6C2501or PI6C2502 with a non zero delay clock driver such as PI6C3813, a system designer can turn the non zero delay buffer into a Zero Delay Clock Driver.

High Speed Design Example (Clocking at 80 MHz)

PI6C2509A and PI6C2510A provide nine and ten copies of the reference clock respectively. If the design requires more than 10 zero delay clock outputs, using two or more PI6C2509A or PI6C2510A drivers is likely to be impractical. The device-to-device skew as a result of using two Zero Delay Clock Drivers can significantly reduce the performance. Pericom Application Note16 recommends using combination of a single output Zero Delay clock driver such as PI6C2501 and a non zero delay clock driver such as PI6C3813A. As shown in Figure 5, this combination provides a Zero Delay clock driver with all the signal characteristics of the original Zero Delay Clock Driver (PI6C2501), but with as many outputs as the non-zero-delay buffer part (PI6C3813). For example combined with PI6C38013A, the system designer can create a Thirteen output Zero Delay Clock driver. Another big advantage of the PLL drivers such as the PI6C2501/2 is that it allows the system designer to adjust or move the output clocks forward or backward in time with respect to the reference clock, to fine-tune a design. As depicted in Figure 5, using a capacitor C at the FB input of PLL does this. This combination will replace the single PI6C3813A in the Switched Ethernet Application described above.

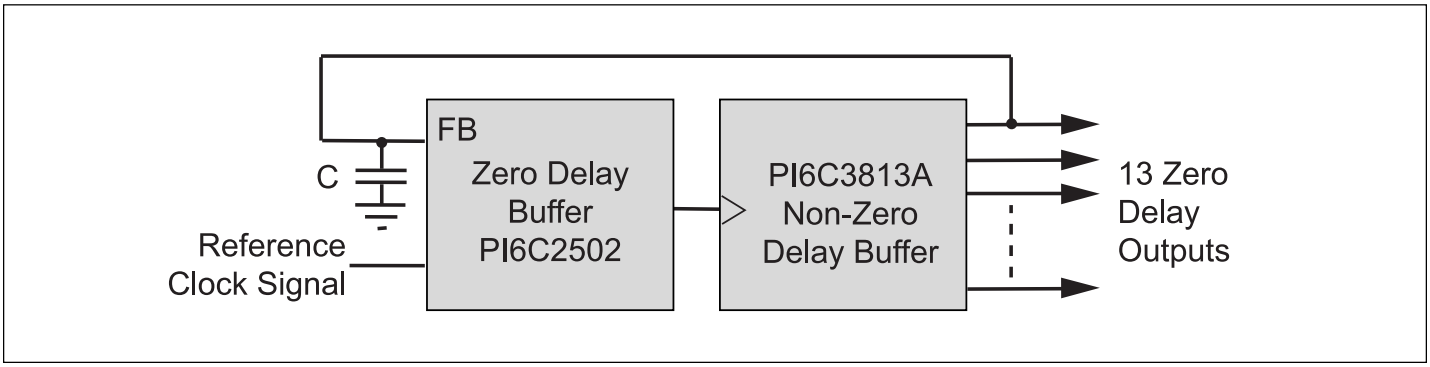

Figure 5. Combination That Provides Zero Delay Between the Reference Clock Signal and 13 Outputs

Other PLL Clocks from Pericom

2509Q/2510Q PLL Drivers

The PLL buffer needs a reference clock from main system. It then generates 9 or 10 clock signals with zero delay compared to the reference clock. The system can only provide one clock signal, which greatly reduces the number of clock signals generated to minimize EMI problems. As shown in Figure 6, the feedback output FBOUT pin is directly connected to the feedback input FBIN pin. The C1 capacitor is designed to adjust the relative timing between the Input Clock and the output clocks, if needed. C1 is typically not connected. As the C1 value increases, the timing of the output clocks will become more leading in time relative to the Input Clock.

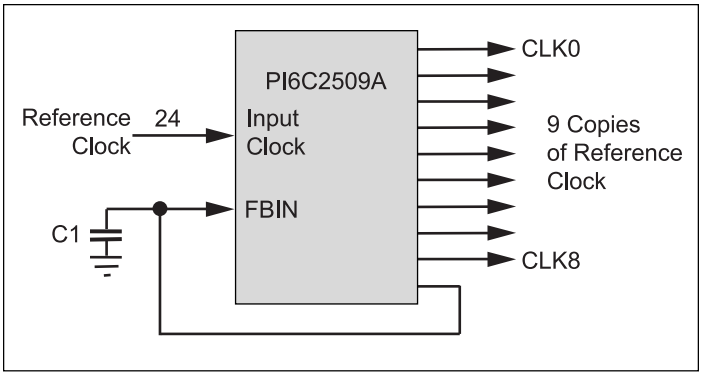

Figure 6. Block Diagram of PI6C2509Q

The output drivers of Pericom PI6C2509Q have been carefully designed to provide sufficiently heavy pull-up and pull-down drive currents such that the clock signals at SDRAM chips meet the rise/fall time requirements of the SDRAM chips. The output drivers are also designed to keep undershoot and overshoot of clock signals to a minimum.

The following AC parameters are very critical to system design engineers, when a designer selects a PLL driver chip for large SDRAM array design. Phase Error is the propagation-time between the Clock Input pin and the clock feedback input FBIN pin.

Since it is ideal to have the clock outputs exactly identical to the Clock Input, phase error should be very small. A phase error of 150ps leading or lagging is fine in 100MHz and 66MHz clock distribution circuits**.** Cycle-to-Cycle Jitter is the difference of period-time between one clock cycle to the adjacent clock cycle. A critical issue on jitter is the Clock Input with spread spectrum. Many PLL circuits will greatly increase jitter and fail to meet jitter spec when the motherboard clock generator enables spread spectrum modulation. Pericom 2509Q/2510Q parts are designed to meet the jitter spec when spread spectrum is disabled as well as enabled, also for 100MHz as well as 66 MHz. Output Skew is the time skew among all clock outputs. The output drivers of Pericom 2509Q/2510Q parts are carefully designed to meet the 200 ps spec at 100MHz as well as 66 MHz.

PI6C2308A PLL Driver

Providing two banks of four outputs, the PI6C2308A and PI6C2308 are 3.3V zero delay buffer designed to distribute clock signals in applications such as PC, workstation, datacom, telecom, and high performance systems. Figure 7 depicts the block diagram of PI6C2308.

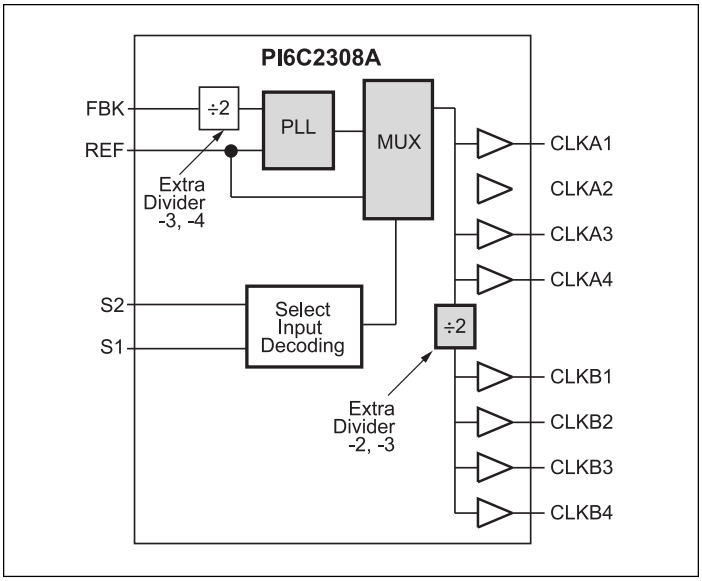

Figure 7. Block Diagram of PI6C2308A

With much better electrical characteristics, the PI6C2308A provides 8 copies of a clock signal that has 150ps phase error compared to a reference clock. The skew between the output clock signals for PI6C2308A is less than 200ps. When there are no rising edges on the REF input, the PI6C2308/A enters a power down state. In this mode the PLL is off and all outputs are three-stated which results in less than 50 μA of current draw.

The base part, PI6C2308/A-1 provides output clocks in sync with a reference clock. For designs that require faster rise and fall times, the PI6C2308/A-1H is the high drive version of the PI6C2308/A-1. Depending on which output drives the feedback pin, the PI6C2308/A-2 provides 2X and 1X clock signals on each output Bank. The PI6C2308/A-3 provides 4x and 2X clock signal on the output. The PI6C2308/A-4 provides 2X clock signal on all outputs. The PI6C2308/A allows bank B to be three-stated in the case all output clocks are not required. For testing purposes, the Select inputs connect the input clock directly to outputs.

Summary

PLL clock drivers have shown many advantages in high performance systems. In networking applications such as Switched Ethernet, PLL drivers are used to de-skew the delay through large clock buffers. They are also used in applications where the system designer needs large multiple of clock signals that are in complete sync with a reference clock. Pericom has developed an array of low skew Zero Delay Clock Drivers such as PI6C5932 (5V), PI6C9910 (5V), PI6C9930 (3V), PI6C2501 (3V), PI6C2509A (3V), PI6C2510A (3V) and PI6C2308A (3V) for both 5 and 3V applications. Lowest clock skews guarantee better designs and optimum performance. Pericom is committed to developing products that meet emerging market requirements and needs.