Interworking Controller Next Generation

The IWORX (InterWORking element neXt generation) IC controller is a multi service engine for line card applications in wireless access networks and media gateways. It transports ATM traffic over PDH and SDH based networks.
Supporting speeds of up to 155 Mbit/s, IWORX enables the adaptation of voice, video and data traffic via AAL2. Shared location of 2G and 3G mobile networks for easy network migration path is facilitated via AAL1 and Circuit Emulated Service (CES). The device allows for flexible bandwidth adjustment of the PDH ports through 4 IMA groups and implements all ATM service categories (CBR, VBR, UBR) for full Quality of Service (QoS) support.
Being a system on a chip with integrated memory and controlled via high-level command interface (API), IWORX is the optimized solution in terms of performance, ease of use, space & power economy.

Applications

- 3G base transceiver stations (Node B) and radio network controller (RNC)
- Multiservice linecards
- Multimedia Gateways

Features

General Features

- Throughput up to 155 Mbit/s
- On-chip CPU for simple protocol handling and control
- Easy configurations, maintenance and in-band communication via message based interface
- Embedded Memory; no additional memory required
- Port specific mode selection
- Time slot specific protocol selection (e.g., AAL1, G.804)
- Dedicated hardware modules for fast & reliable performance intensive communication functions such as AAL1, AAL2, G.804, OAM, IMA and traffic management
- Reduces power, board space, cost due to level of integration
- System recovery support via read-back of configuration and connection data
- Boundary scan support per IEEE 1149.1
- Power consumption less then 2 W
- Power supply 3.3 V I/Os, 1.8 V core
- Temperature range -40°C to +85°C
- Package P-BGA-388

ATM Adaptation Layer Functions

- AAL1 mode (ITU-T I.363-1) and Circuit Emulation Service (ATMF AF-VTOA 0078.000):
  - Support for up to 256 AAL1 ATM VCCs
  - Support for structured and unstructured CES mode for 8 E1/T1/J1 links
  - Support for Channel Associated Signaling (CAS)
  - Built in SRTS (selectable) and ACM clock recovery methods
- AAL2 mode (ITU-T I.363.2):
  - Support for up to 16 AAL2 ATM VCCs
  - Mux/demux of up to 255 AAL2 channels per AAL2 ATM VCC
  - Support for up to 4080 AAL2 CIDs
  - AAL2 timer_CU is adjustable from 0.1 to 10 ms with a resolution of 0.1 ms
- AAL5 support (ITU-T I.363-5)
  - Support of inband management cells over E1/T1/J1 lines and UTOPIA

ATM Layer Functions

- Address Reduction & Header Translation
  - Reduction of full VPI/VCI address range to 256 internal addresses
  - VPI/VCI translation for 256 bi-directional ATM connections
  - Support for ATM UNI/NNI mode

IWORX PXF 4225 V1.2

ATM Interworking Controller

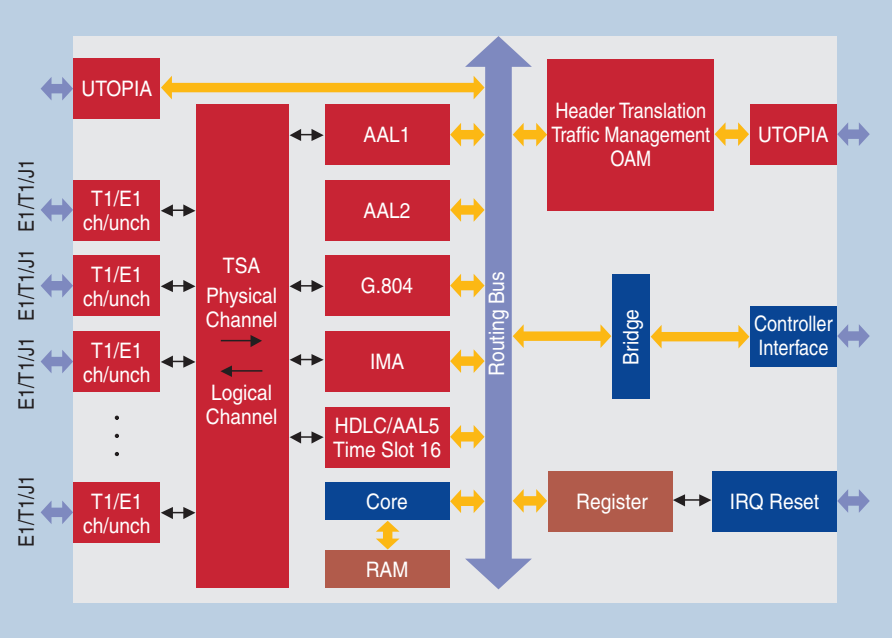
Infineon technologies

Never stop thinking.

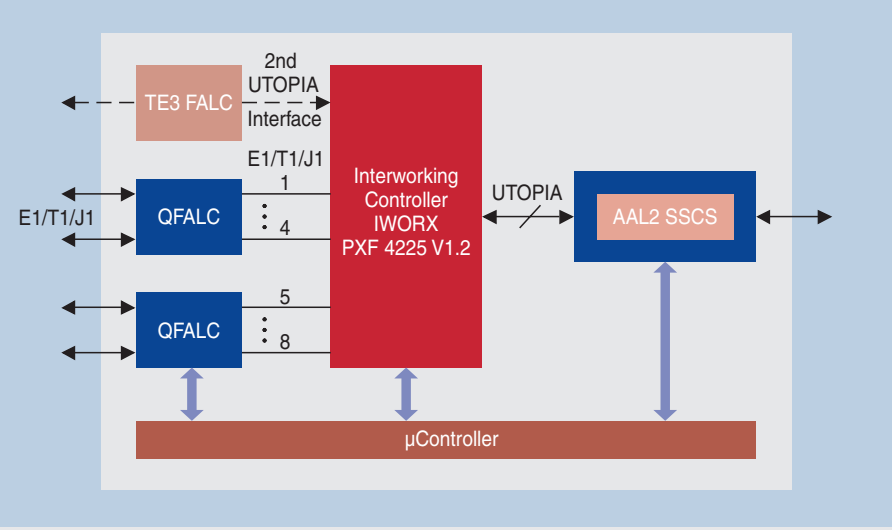
ATM Layer Functions cont.

- Traffic Management
  - Supports CBR, VBR-rt, VBR-nrt, UBR, UBR+ and GFR QoS queues
  - Per VC queuing for up to 256 connections in transmit direction
  - Provides weighted fair queuing (WFQ) scheduling
  - Early Packet Discard (EPD), Partial Packet Discard (PPD) and cell discard (CLP 0+1)
  - AAL2 traffic management: 2 queues per AAL2 ATM VCC with WFQ at AAL2 channel level

IWORX PXF 4225 V1.2 Block Diagram



Application Example: Base Transceiver Station



- Operating and Maintenance (ITU-T I.610 (99))
  - Provides OAM F4 and F5 cell insertion and extraction
  - OAM Fault Management (AIS, RDI, Loopback, CC)
  - OAM Performance Monitoring
  - Provides on-chip CRC-10 and BIP16 calculation

Transmission Convergence Sublayer Functions

- ATM TC sublayer (ITU-T G.804)
- Support for G.804 on fractional E1/T1/J1 (ATMF-FN64)
- Support of up to 8 HDLC channels for Common Channel Signaling (CCS)
- IMA (ATMF AF-PHY 0086.001):
  - Supports of up to 4 IMA groups and up to 8 links per IMA group
  - Frame length up to 256 cells
  - Support of Common and Independent Transmit Clock
  - Link differential delay compensation up to 25 ms

Interfaces

- 8 E1/T1/J1 ports
- UTOPIA Interfaces (level 1 and 2, ATMF AF-PHY 0017.000, 0039.000)
  - Line side 155 Mbit/s throughput, ATM device
  - Backplane side 622 Mbit/s throughput, Multi Phy device
- 16/32-bit Microcontroller Interface (Intel or Motorola type)

Documentation and Support

- Data Sheet and Programmers Reference Manual
- EASY 4225-R1 evaluation board
- Interworking Controller Application wizard
  - Configuration tool
  - Source code generator
- Low Level Driver

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