IBM PCI-X to InfiniBand Host Channel Adapter

Features

Highlights

- Intended to comply fully with version 1.0 of the InfiniBand™ architecture
- Dual InfiniBand 1x or 4x connections to the InfiniBand network via integrated InfiniBand serializers/deserializers (SERDESs) and PHYs
- On-device dual pipeline architecture, with independent transmit and receive IBM PowerPC® 405 (200MHz) plus dual state-machine based data movement engines, provides very high speed packet creation and processing
- High-performance HCA architecture supported with dedicated InfiniBand context memory (on-device plus up to 256MB optional off-device)

InfiniBand Interface

- Supports all transport services: UD, UC, RC, RD and raw packets
- Four data virtual lanes (VLs) plus management virtual lane support
- Supports up to 16K queue pairs (QPs), up to 16K completion queues (CQs), and up to 64K end-to-end (EE) contexts; maximum number of QPs and EEs depends on amount and configuration of context memory
- Support for up to 32K memory regions/windows
- Configurable maximum transfer unit (MTU) from 256 to 2048 bytes
- Supports default plus four configurable P_Keys
- Up to four outstanding remote direct memory access (RDMA) read requests per QP
- Up to 1K end-to-end address vectors in Host Channel Adapter (HCA) memory
- Maximum message size is 2 GBs
- Supports two configurable Global IDs
- Supports acknowledge (ACK) coalescing
- Supports 16K multicast groups

PCI Interface

- PCI v2.2 compliant
- PCI-X Addendum v1.0 compliant
- PCI/PCI-X interface at 33, 66,100 and 133MHz
- 3.3V interface
- 32 and 64-bit data and address buses
- Support for four outstanding split transactions in PCI-X mode
- Zero wait states on both master and slave data phases

Host Interface

- Separate transmit and receive data engines
- Work queue (WQ) and completion queue (CQ) access protection
- Doorbell decoding

Management Support

- Host processor implements subnet and performance management agents
- Generates traps

Software Support

- Software provided to support Linux and Windows™ operating systems
- HCA transmit and receive microcode provided which runs on dual integrated IBM PowerPC microprocessors and is upgradable
- Source code of all included software provided

Description

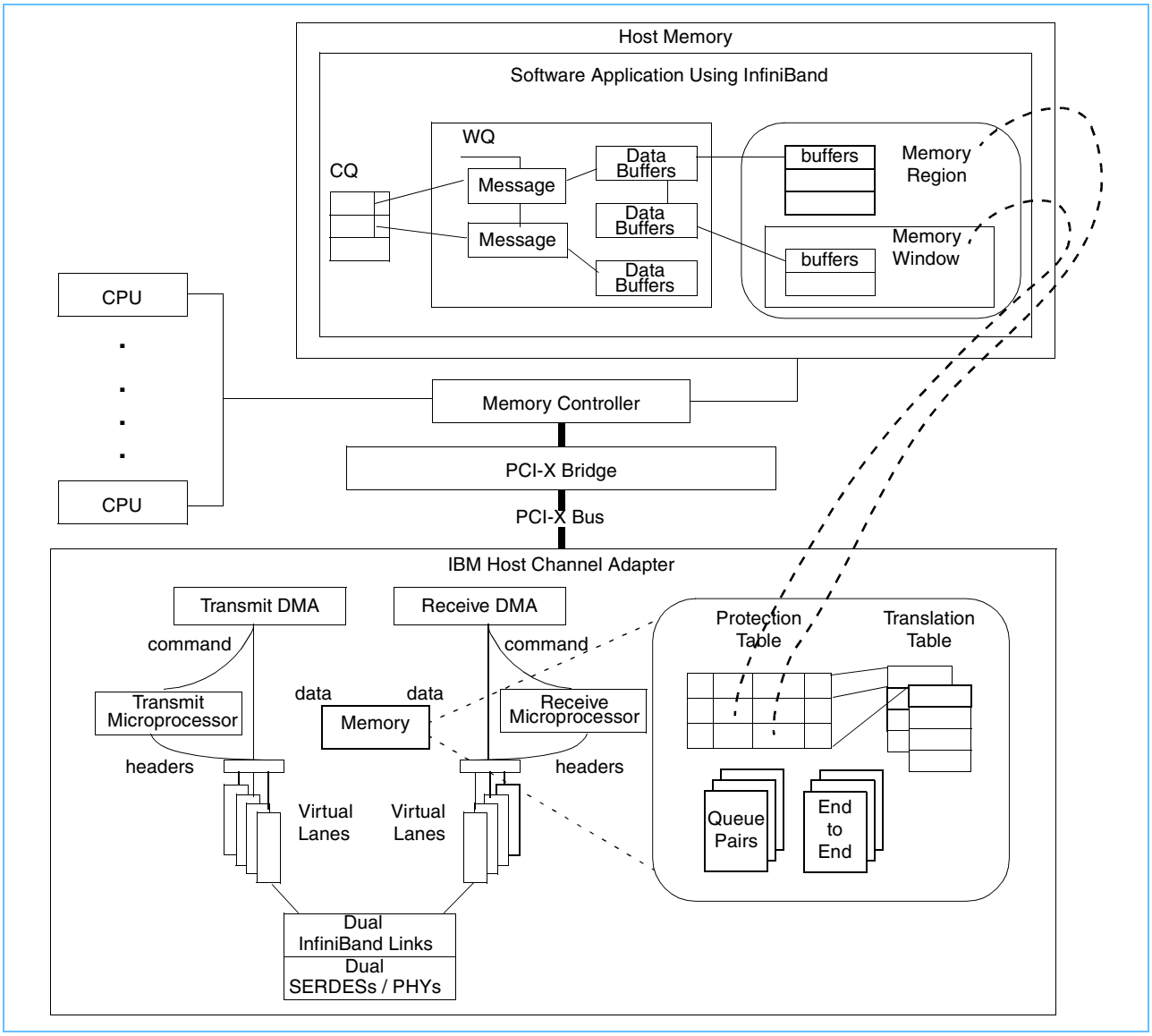
The IBM PCI-X to InfiniBand Host Channel Adapter (HCA) allows connectivity between a host's PCI-X bus and an InfiniBand network. The dual InfiniBand ports provide the capability to support autopath migration and single or multiple subnet connections with a single HCA device.

The IBM HCA, in its simplest configuration, is a single device solution that integrates the HCA function, the supporting context memory, and dual integrated 4x SERDESs and PHYs. It is capable of being used as a single device HCA that would only require an NVRAM for the HCA microcode and GUIDs.

The IBM HCA implements very high performance packet creation and processing via dedicated pipelined header and data processing units.Two IBM PowerPC 405 embedded microprocessors (running at 200MHz) plus two separate direct memory access (DMA) engines provide concurrent receive and transmit data path processing. The highly

configurable DMA engines support both physical and virtual addressing modes. The HCA also implements a layered memory structure. Connection related information is stored in on-device and also, optionally, in off-device memory attached directly to the HCA. The latter configuration allows support of up to 16K queue pairs (QPs) and eliminates the performance constraints associated with the storage of QP context information in system memory.

IBM Host Channel Adapter Overview



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Revision Log

Rev	Contents of Modification
September 8, 2000	Initial release.
October 9, 2000	First revision (01). Minor changes to wording
March 7, 2001	Second revision (02). Change to number of P_Keys supported.

Printed in the United States of America March 2001

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March 7, 2001