DATA SHEET

PCA2002

32 kHz watch circuit with programmable output period and pulse width

Objective specification
Supersedes data of 2002 Oct 25

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Philips
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32 kHz watch circuit with programmable output period and pulse width	PCA2002

FEATURES

- 32 kHz quartz oscillator, amplitude regulated with excellent frequency stability and high immunity to leakage currents
- Electrically programmable time calibration with 1 ppm resolution (stored in OTP memory)
- The quartz crystal is the only external component required
- Very low current consumption: typically 90 nA
- Output pulses for bipolar stepping motors
- 5 different programmable output periods (1 to 30 s)
- Output pulse width programmable between 1 and 8 ms
- Full or chopped motor pulse and pulse stretching, selectable
- Stop function for accurate time setting and current saving during the shelf life
- Test mode for accelerated testing of the mechanical parts of the watch.

GENERAL DESCRIPTION

The PCA2002 is a CMOS integrated circuit for battery operated wrist watches with a 32 kHz quartz crystal as the timing element and a bipolar stepping motor. The crystal oscillator and the frequency divider are optimized for minimum current consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment.

The output period and the output pulse width can be programmed. It can be selected between a full output pulse or a chopped output pulse with a duty cycle of 75%. In addition, a stretching pulse can be added to the primary driving pulse.

A RESET pin is provided which is used for stopping the motor, accurate time setting and for an accelerated testing of the watch.
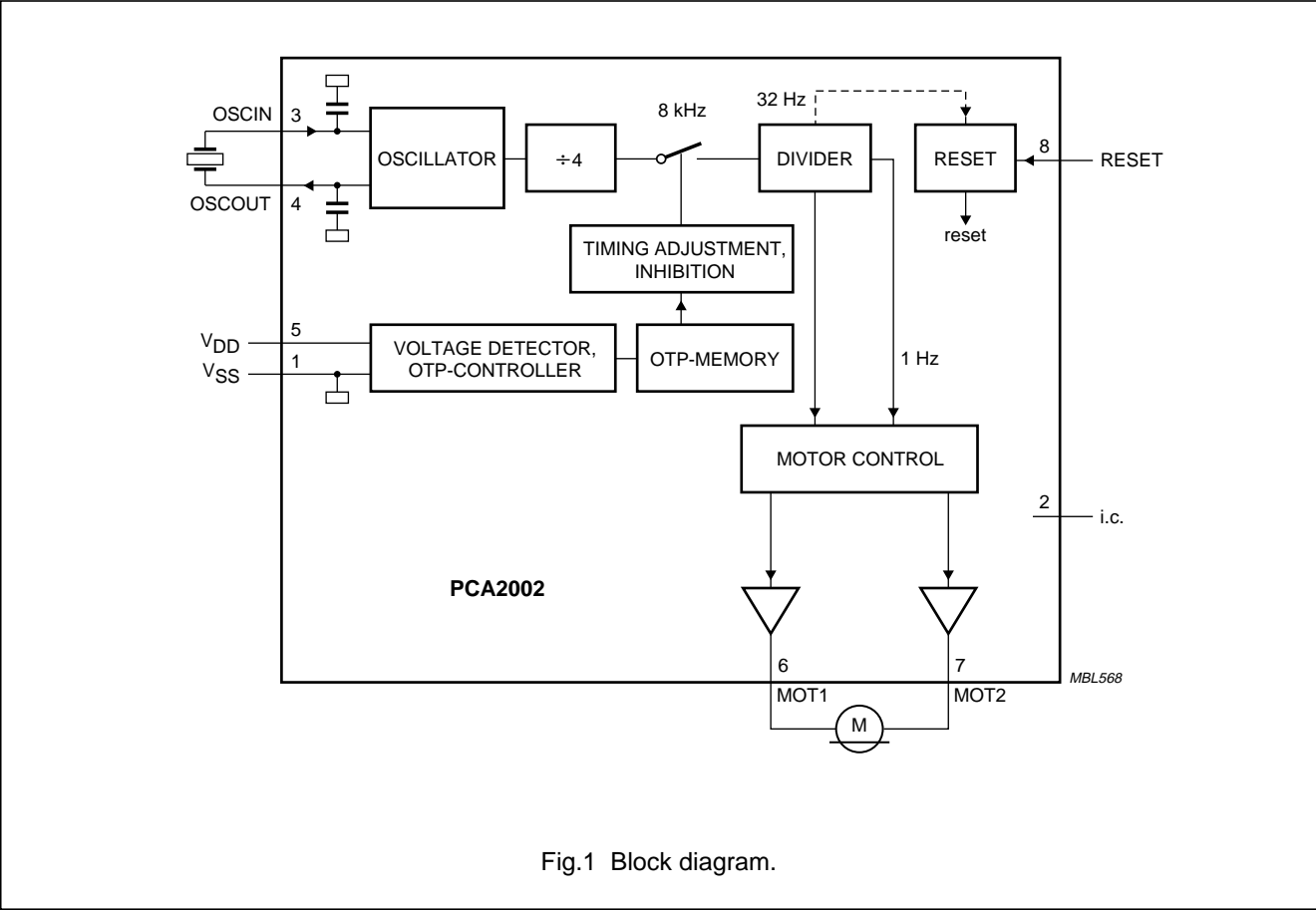
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA2002U/AA	–	bare die; chip in tray	–
PCA2002U/10AA	–	bare die; chip on film frame carrier	–
PCA2002T	PMFP8	plastic micro flat package; 8 leads (straight)	SOT144-1

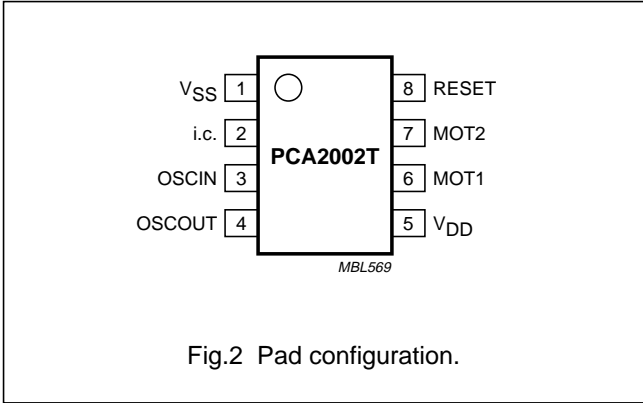## 32 kHz watch circuit with programmable output period and pulse width   PCA2002

BLOCK DIAGRAM

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V$_{SS}$	1	ground
i.c.	2	internally connected
OSCIN	3	oscillator input
OSCOUT	4	oscillator output
V$_{DD}$	5	supply voltage
MOT1	6	motor 1 output
MOT2	7	motor 2 output
RESET	8	reset input

Fig.2 Pad configuration.

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FUNCTIONAL DESCRIPTION

Motor pulse

The motor driver delivers pulses with an alternating polarity. The output waveform across the motor terminals is illustrated in Fig 3. Between the motor pulses, both terminals are connected to V_{DD} which means that the motor is short-circuited.

The following parameters can be selected and are stored in a One Time Programmable (OTP) memory:

- Output periods of 1, 5, 10, 20 and 30 s
- Pulse width (t_p) between 0.98 and 7.8 ms in steps of 0.98 ms
- Full or chopped (75%) output pulse
- Pulse stretching: an enlargement pulse is added to the primary motor pulse. This enlargement pulse has a duty cycle of 25% and a width which is twice the programmed motor pulse width.

Time calibration

The crystal oscillator has an integrated load capacitance of 5 pF, which is lower than the specified load capacitance of 8.2 pF for the quartz crystal.

It oscillates therefore, at a frequency which is typically 60 ppm higher than 32.768 Hz. This positive frequency offset is then compensated by removing, every minute or every two minutes, the appropriate number of 8192 Hz pulses (maximum 127 pulses) of the divider chain. The timing correction is given in Table 1.

After measuring the effective oscillator frequency, the number of correction pulses must be calculated and stored together with the calibration period in the OTP memory; see Section "Programming procedure".

The oscillator frequency can be measured at the RESET pin, where a square wave with the frequency $f_{osc}/1024$ is provided. It should be noted that this frequency shows a jitter every minute or every two minutes (depending on the programmed calibration period) which originates from the time calibration.

Details on how to measure the oscillator frequency and the programmed inhibition time are given in Section "Programming procedure".

Table 1   Timing correction

| CALIBRATION PERIOD (min)	CORRECTION PER STEP (N = 1)		CORRECTION PER STEP (N = 127)	
	ppm	s/day	ppm	s/day
1	2.03	0.176	258	22.3
2	1.017	0.088	129	11.15

Reset

An output frequency of 32 Hz ($f_{osc}/1024$) is provided at the RESET pin. Connecting the RESET pin to V_{DD} stops the motor drive and opens the motor switches.

After releasing the pin, the first motor pulse is generated exactly one period later with the opposite polarity to the last pulse before stopping. The debounce time for the RESET function is between 31 and 62 ms.

Connecting the RESET pin to V_{SS} activates the test mode. In this mode the motor output frequency is 32 Hz, which can be used to test the mechanical function of the watch.

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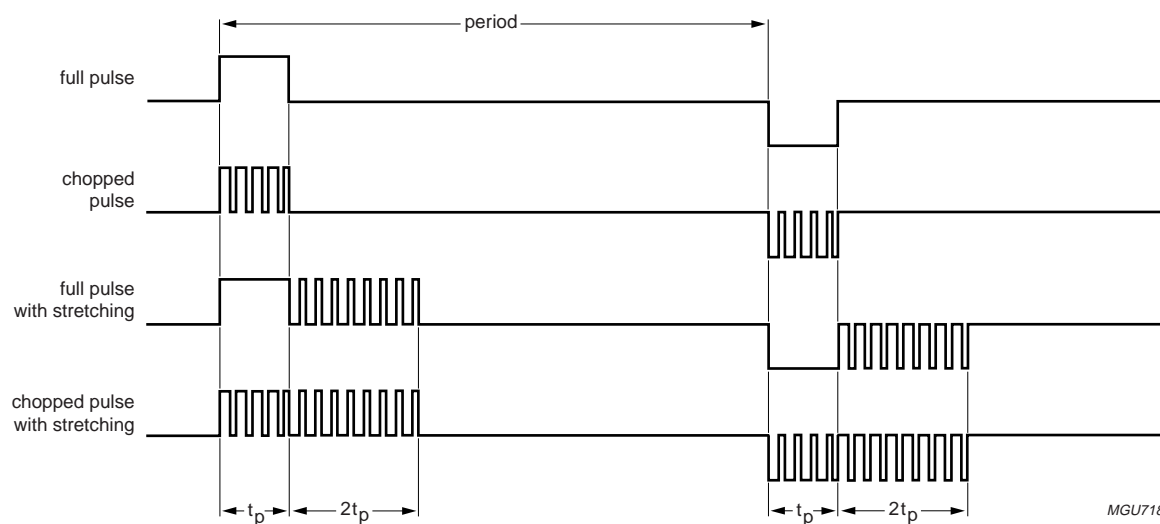
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Fig.3 Motor output waveforms.

Programming possibilities

The programming data is stored in two words; see Table 2.

Table 2   Words and bits

WORD	BIT							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	pulse width			output period			duty cycle	pulse stretching

Table 3   Description of word B bits

BIT	VALUE	DESCRIPTION
Pulse width t_p (ms)		
1 to 3	000	0.98
	001	1.95
	010	2.9
	011	3.9
	100	4.9
	101	5.9
	110	6.8
	111	7.8
Output period (s)		
4 to 6	000	1
	001	5
	010	10
	011	20
	100	30
Duty cycle of motor pulse		
7	0	75%
	1	100%
Pulse stretching		
8	0	no pulse stretching
	1	a pulse width of $2t_p$ and a duty factor of 25% is added

Table 4   Description of word A bits

BIT	VALUE	DESCRIPTION
Inhibit time		
1 to 7	–	the number of the 8192 Hz pulses to be removed (binary coded; MSB = A1, LSB = A7)
Calibration period		
8	0	1 minute
	1	2 minutes

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Programming procedure

For a watch it is essential that the timing calibration can be made after the watch is fully assembled. In this situation, the supply pads are often the only terminals which are still accessible.

Writing to the OTP cells and performing the related functional checks is achieved in the PCA2002 by modulating the supply voltage. The necessary control circuit consists basically of a voltage level detector, an instruction state counter (which determines the function to be performed) and an 8-bit shift register which allows writing the OTP cells of an 8-bit word in one step and which acts as data pointer for checking the OTP content.

There are four different instruction states:

1. State 1; measurement of the crystal oscillator frequency (divided by 1 024)
2. State 2: measurement of the inhibition time
3. State 3: write/check word A
4. State 4: write/check word B.

Each instruction state is switched on with a pulse to V_P (6 V). After this large pulse, an initial waiting time of t_0 (10 ms) is required. The programming instructions are then entered by modulating the supply voltage with small pulses [amplitude V_{mod} (0.35 V) and pulse width t_{mod} (30 μs)]. The first small pulse defines the start time, the following pulses perform three different functions, depending on the time delay (t_d) from the preceding pulse see Figs to :

$t_d = t_1$ (0.7 ms): increments the instruction counter

$t_d = t_2$ (1.7 ms): clocks the shift register with D = 0 at the input

$t_d = t_3$ (2.7 ms): clocks the shift register with D = 1 at the input.

The programming procedure requires a stable oscillator, which means that a waiting time, determined by the start-up time of the oscillator, is necessary after power-up of the circuit.

After the V_P pulse, the instruction counter is in State 1 and the data shift register is cleared. The instruction state ends with a second pulse to V_P or with the pulse to V_{store}. In any event the instruction states are terminated automatically 2 seconds after the last V_{DD} pulse.

MEASUREMENT OF THE OSCILLATOR FREQUENCY AND THE INHIBITION TIME

The output of the two measuring states can either be monitored directly at the RESET pin or as a modulation of the supply current (a modulating resistor of 30 kΩ is connected between V_{DD} and V_{SS} when the signal at the RESET pin is HIGH):

State 1: crystal oscillator frequency divided by 1 024; state 1 starts with a pulse to V_P and ends with a second pulse to V_P

State 2: inhibition time (see Fig 5); a frequency with the period of (31.25 ms + n × 0.122 ms) appears at the RESET pin and as current modulation at the supply pin.

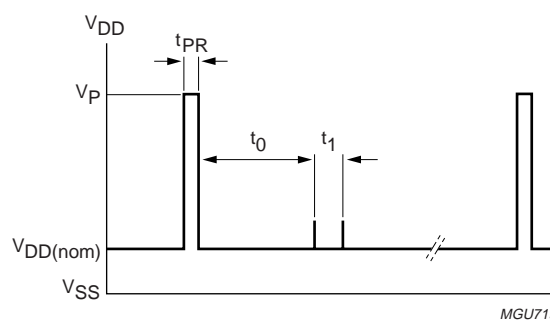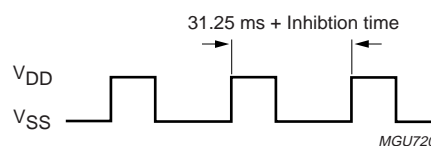Fig.4   Supply voltage modulation for start and stop of instruction State 2.

Fig.5   Output waveform at the RESET pin for instruction State 2.

PROGRAMMING THE MEMORY CELLS

The data to be stored is first written into the shift register
and then transferred to the OTP cells by raising the supply
voltage to V_{store} (11 V) for the time t_{store} (100 ms);
see Fig 6.

Programming a memory word is done using the following
sequence:

1. Start with a V_P pulse, wait for the time period t_0 and set
   the instruction counter to the word to be written ($t_d = t_1$)

2. Enter the data to be stored into the shift register ($t_d = t_2$
   or t_3), LSB first (bit 8) and MSB last (bit 1)

3. Store the word by raising the supply voltage to V_{store}
   (9.9 V for 100 ms); the delay between the last data bit
   and the store pulse is $t_d = t_4$ (0.2 ms).

The example shown in Fig 7 performs the following
functions: start, setting the instruction counter to State 4
(word B), entering data word 1101 0001 into the shift
register (sequence: LSB first and MSB last) and writing the
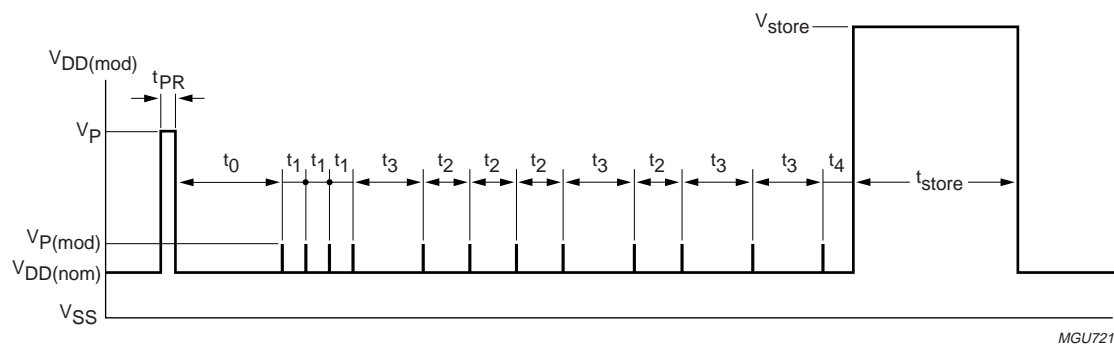OTP cells for word B.

Fig.6 Supply voltage modulation for programming.

CHECKING THE MEMORY CONTENT

The stored data of the OTP array can be checked bit-wise
by measuring the supply current. The array word is
selected by the instruction state, the bit is addressed by
the shift register. To read a word, the word is first selected
($t_d = t_1$) and a logic 1 is written into the first cell of the shift
register ($t_d = t_3$).

This logic 1 is then shifted through the entire shift register
($t_d = t_2$, so that it points with each clock pulse to the next
bit. If the addressed OTP cell contains a logic 1, a 30 kΩ
resistor is connected between V_{DD} and V_{SS}; this increases
the supply current accordingly.

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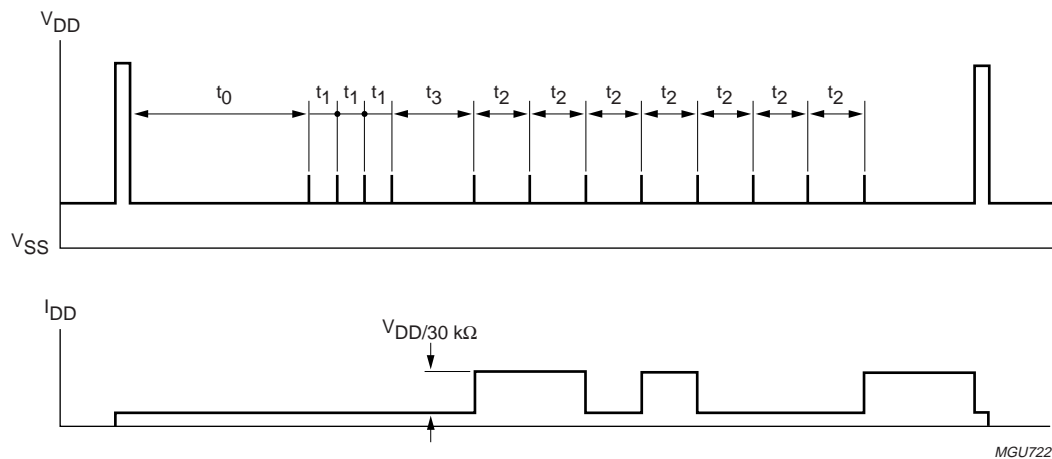
The corresponding supply current variation for B = 1101 0001 (the sequence is MSB first and LSB last).

Fig.7 Supply voltage modulation for reading word B.

Frequency tuning at assembled watch

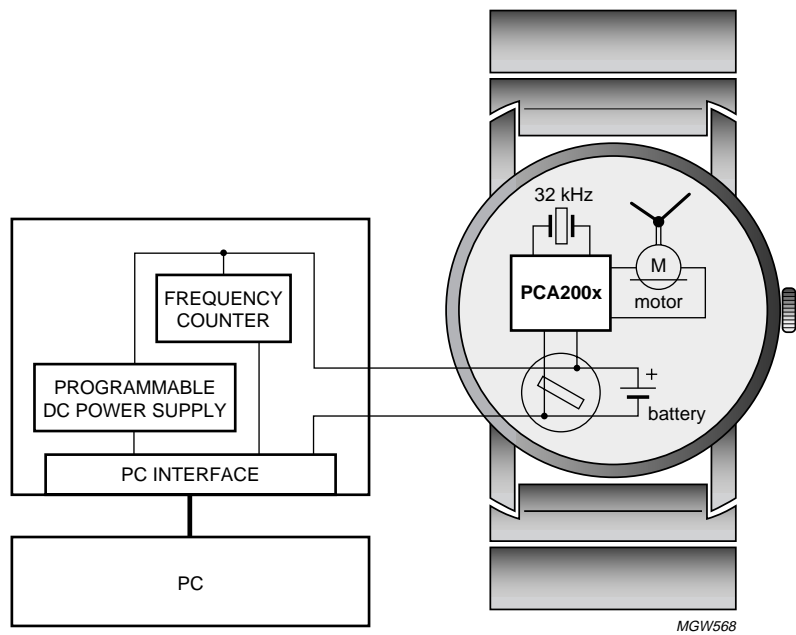Figure 8 shows the test set-up for frequency tuning the assembled watch.

Fig.8 Frequency tuning the assembled watch.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	$V_{SS} = 0$ V; notes 1 and 2	−1.8	+7	V
V_I	all input voltages		$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
t_{sc}	short-circuit duration time		indefinite		
T_{amb}	ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Notes

1. When writing to the OTP cells, the supply voltage (V_{DD}) can be raised to a maximum of 12 V for a time period of 1 s.

2. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows which rapidly discharges the battery.

HANDLING

Inputs an outputs are protected against electrostatic discharges in normal handling. However to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

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CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; quartz crystal; R_s = 40 kΩ; C_1 = 2 to 3 fF; C_L = 8.2 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	normal operating mode; T_{amb} = −10 to +60 °C	1.1	1.55	3.6	V
ΔV_{DD}	supply voltage variation	$\Delta V/\Delta t$ = 1 V/μs	–	–	0.25	V
I_{DD}	supply current	between motor pulses	–	90	120	nA
		between motor pulses at V_{DD} = 3.5 V	–	120	180	nA
		T_{amb} = −10 to +60 °C	–	–	200	nA
		stop mode; pad RESET connected to V_{DD}	–	100	135	nA
Motor output						
V_{sat}	saturation voltage $\Sigma(P + N)$	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
$Z_{o(sc)}$	short-circuit impedance	between motor pulses; I_{motor} < 1 mA	–	200	300	Ω
Oscillator						
$V_{osc(start)}$	starting voltage		1.1	–	–	V
g_m	transconductance	$V_{OSCIN} \leq 50$ mV (p-p)	5	10	–	μS
$t_{su(osc)}$	start-up time		–	0.3	0.9	s
$\Delta f/f$	frequency stability	ΔV_{DD} = 100 mV	–	0.05	0.2	ppm
C_L	integrated load capacitance		4.3	5.2	6.3	pF
R_{par}	parasitic resistance	allowed resistance between adjacent pads	20	–	–	MΩ
Reset						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R_L = 1 MΩ; C_L = 10 pF	1.4	–	–	V
t_r	rise time	R_L = 1 MΩ; C_L = 10 pF	–	1	–	μs
t_f	fall time	R_L = 1 MΩ; C_L = 10 pF	–	1	–	μs
$I_{i(av)}$	average input current	pad RESET connected to V_{DD} or V_{SS}	–	10	20	nA

OTP PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage during programming procedure	1.5	–	3.0	V
V_P	supply voltage for starting and stopping of programming procedure	6.0	6.5	7.0	V
t_P	pulse width of start and stop pulse	5	7.5	10	ms
$V_{P(mod)}$	supply voltage modulation for entering instructions	320	350	380	mV
t_{mod}	modulation pulse width	25	30	40	μs
V_{store}	supply voltage for writing to the OTP cells	9.8	9.9	10.0	V
t_{store}	pulse width for writing to the OTP cells	95	100	110	ms
I_{store}	supply current for writing to the OTP cells	–	–	10	mA
t_0	waiting time after start pulse	8	10	30	ms
t_1	pulse distance for incrementing the state counter	0.6	0.7	0.8	ms
t_2	pulse distance for clocking the data register with D = 0 at the input	1.6	1.7	1.8	ms
t_3	pulse distance for clocking the data register with D = 1 at the input	2.6	2.7	2.8	ms
t_4	waiting time for writing to the OTP cells	0.1	0.2	0.3	ms
SR	slew rate for modulation of the supply voltage	0.1	–	10	V/μs
R_{read}	read out resistor for supply current modulation	18	30	45	kΩ

Note

1. Each word should not be programmed more than once.

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BONDING PAD LOCATIONS

| SYMBOL	PAD	COORDINATES[1]	
		x	y
V_{SS}[2]	1	−480	+330
TEST[3]	2	−480	+160
OSCIN	3	−480	−160
OSCOUT	4	−480	−330
V_{DD}	5	+480	−330
MOT1	6	+480	−160
MOT2	7	+480	+160
RESET	8	+480	+330

Notes

1. All coordinates are referenced, in μm, to the centre of the die (see Fig.9).

2. The substrate (rear side of the chip) is connected to V_{SS}. Therefore, the die pad must be either floating or connected to V_{SS}.

3. Pad TEST is used for factory tests; in normal operation it should be left open-circuit, and it has an internal pull-down resistance to V_{SS}.

Table 5 Mechanical chip data; note 1

PARAMETER	VALUE
Bonding pad:	
metal	96×96 μm
opening	86×86 μm
Thickness:	
chip for bonding	200 ±25 μm
chip for golden bumps	270 ±25 μm
Bumps:	
height	25 ±5 μm

Note

1. The substrate of the chip is connected to V_{SS}. The TEST pin is used for factory test, in normal operation it should be left open-circuit. The test pin has an internal pull-down resistor connected to V_{SS}.
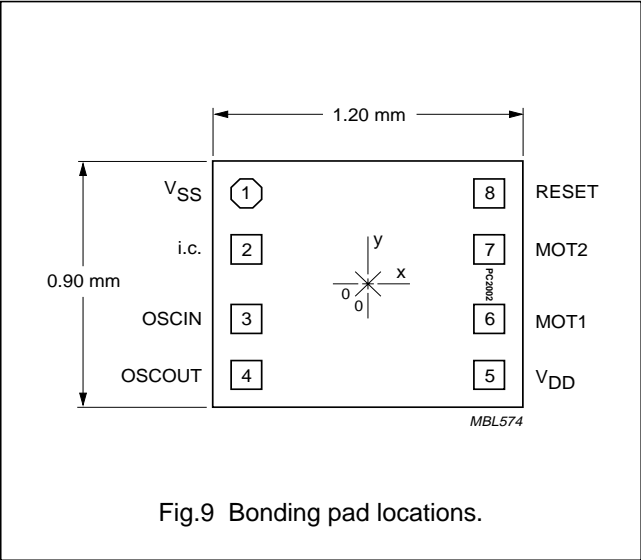
Fig.9 Bonding pad locations.

TRAY INFORMATION

Fig.10 Tray details.
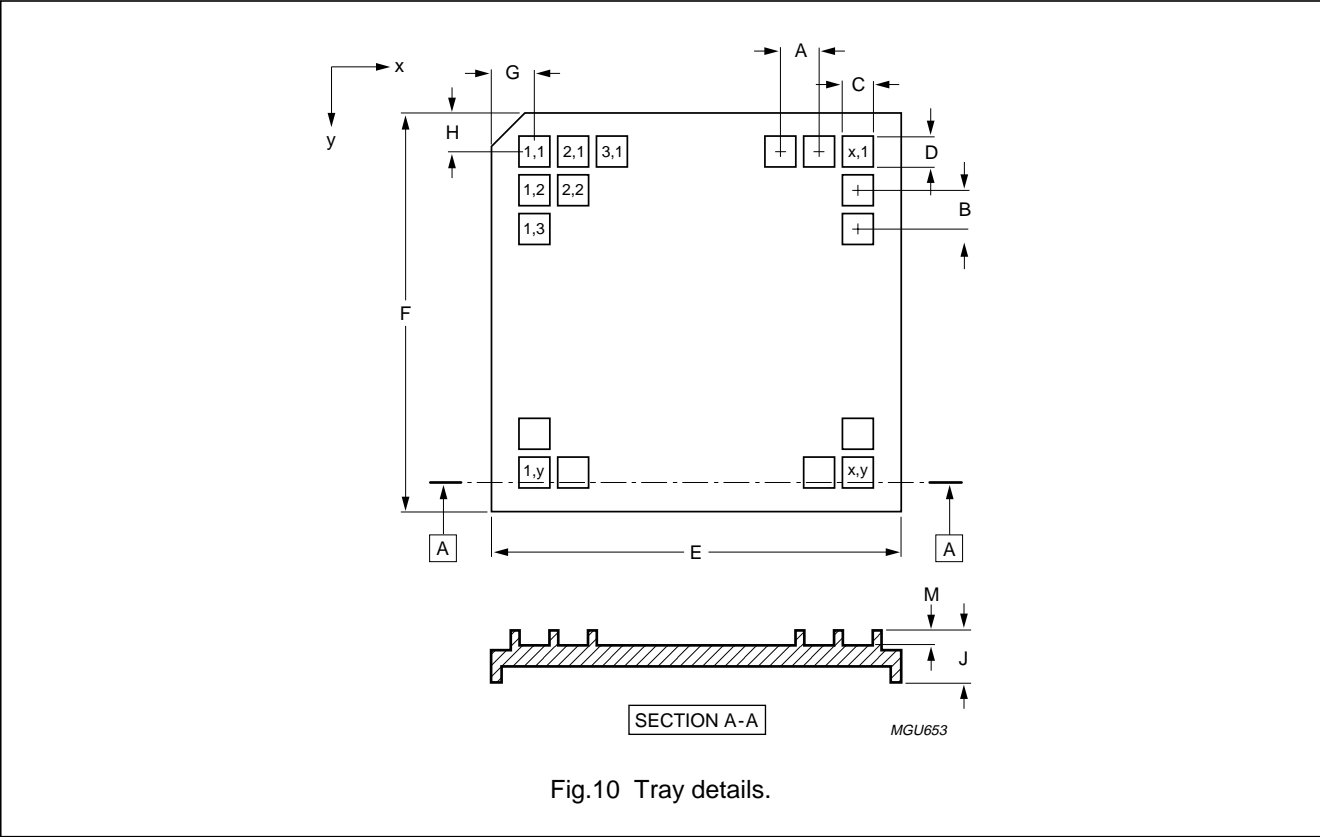
Table 6 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch; x direction	2.15 mm
B	pocket pitch; y direction	2.43 mm
C	pocket width; x direction	1.01 mm
D	pocket width; y direction	1.39 mm
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	distance from cut corner to pocket (1 and 1) centre	4.86 mm
H	distance from cut corner to pocket (1 and 1) centre	4.66 mm
J	tray thickness	3.94 mm
M	pocket depth	0.61 mm
x	number of pockets in x direction	20
y	number of pockets in y direction	18

The orientation of the IC in a pocket is indicated by the position of the IC type name on the surface of the die, with respect to the cut corner on the upper left of the tray.
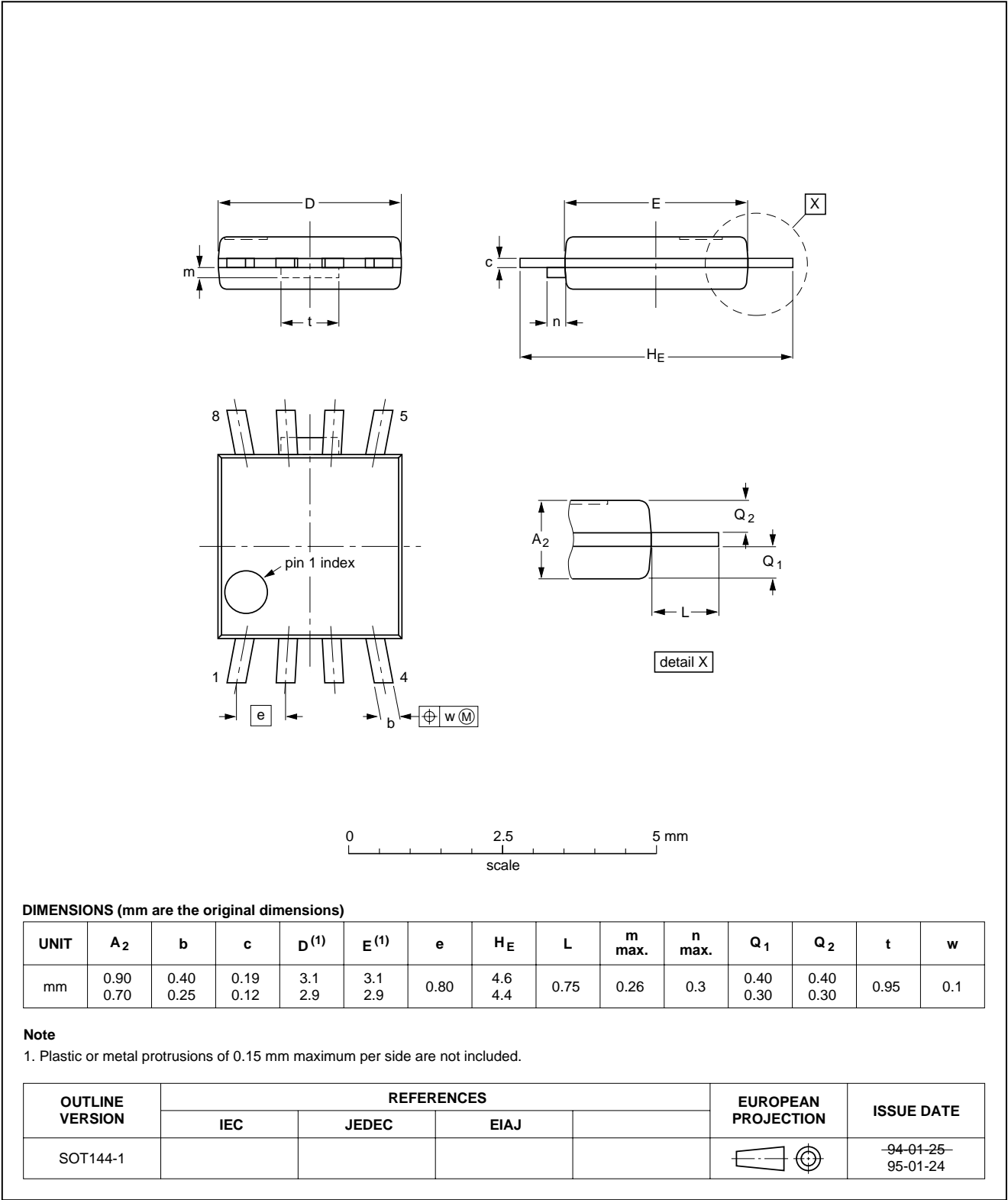
Fig.11 Tray alignment.
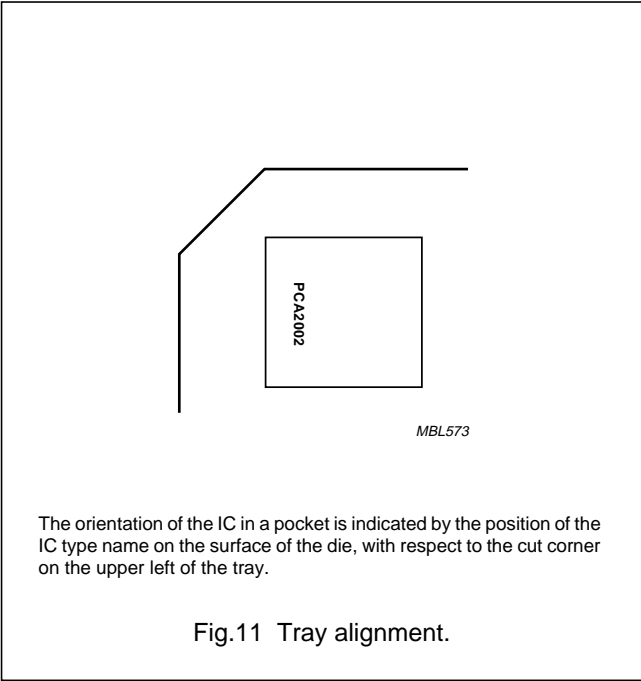
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PACKAGE OUTLINE

PMFP8: plastic micro flat package; 8 leads (straight)

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DIMENSIONS (mm are the original dimensions)

UNIT	A_2	b	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	m max.	n max.	Q_1	Q_2	t	w
mm	0.90 0.70	0.40 0.25	0.19 0.12	3.1 2.9	3.1 2.9	0.80	4.6 4.4	0.75	0.26	0.3	0.40 0.30	0.40 0.30	0.95	0.1

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT144-1						~~94-01-25~~ 95-01-24

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	**REFLOW**[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.

2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.

2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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