PCI 9610

64-bit, 66MHz PCI Bus Mastering I/O Accelerator for Motorola PowerQUICC II and MPC 603e/740/750 Processor Bus Designs

Connectivity

- 64-bit, 66MHz PCI r2.2 compliant
- Motorola PowerQUICC II and MPC 603e/740/750-compatible 64-bit, 66MHz processor bus
- 3.3V I/O, 5V tolerant bus interfaces
- PICMG 2.1 r2.0 Hot Swap Silicon
- 416-ball, 27 x 27 mm, 1.00 mm fine pitch PBGA (FPBGA)

Performance

- Zero wait state burst operation
  - PCI bus bursts to 528 MB/sec
  - Processor bus bursts to 528 MB/sec
- 4 DMA Channels
  - Block Mode
  - Scatter/Gather transfers
    - DMA descriptor ring management
  - Demand Mode & EOT H/W controls
- Direct Master data transfers
  - Generate any PCI transaction
  - Read ahead and programmable read prefetch counter
- Direct Slave data transfers
  - Access 8-, 16-, 32-, and 64-bit processor bus devices
  - Deferred reads, deferred writes, read ahead, posted writes, programmable read prefetch counter

Control

- I_2O r1.5 messaging unit
- Eight mailbox & two doorbell registers
- PCI arbiter supports 7 external masters
- Host mode reset/interrupt signal configuration
- PCI $D3_{COLD}$ Power Management Event (PME) generation support

PLX TECHNOLOGY
THE I/O INTERCONNECT SOLUTION

Optimal PCI Performance for Your 64-bit PowerPC Applications

The PCI 9610 offers unmatched flexibility, connectivity, and high performance I/O acceleration to enable leading edge 64-bit, 66MHz PowerPC-based PCI, CompactPCI, and embedded host designs.

Motorola MPC8260 PowerQUICC II Designs

The PCI 9610 is the perfect match for the Motorola® MPC8260 PowerQUICC® II, the industry's first 64-bit communication processor and a key enabler of 64-bit PCI designs. The PCI 9610 includes an enhanced 64-bit, 66MHz direct-connect interface to the MPC8260, an advanced Data Pipe Architecture™ with four DMA channels, and a 64-bit, 66MHz PCI bus interface.

Motorola MPC 603e/740/750 Designs

The PCI 9610 also directly connects to other PowerPC 603e bus compliant processors such as the MPC 603e/740/750. These processors are very popular choices for embedded host applications. The PCI 9610, with its support of embedded host control signal configuration, a PCI arbiter, and PCI Type 0 and 1 Configuration cycles is the perfect companion chip for these processors.

Move Your 32-bit PowerPC Designs Up To 64-bit, 66MHz PCI and Processor Bus Operation

As both the PCI bus and PowerPC processors evolve to meet the ever increasing I/O demands of leading edge embedded systems, PLX continues to provide leading edge, high performance PCI I/O acceleration solutions for PowerPC processors. Based upon the architecture of the industry-leading PCI 9054, the PCI 9610 offers a variety of technological advances designed to serve the needs of today's PowerPC-based telecom, networking, and I/O adapter designs:

- 64-bit, 66MHz PCI operation
- 64-bit, 66MHz PowerPC processor bus operation
- 4 DMA channels supporting DMA descriptor list ring management
- PICMG 2.1 r2.0 Hot Swap silicon, including Bias Voltage, Early Power, 64-bit Initialization, and Initially Not Responding Support
- PCI Power Management r1.1 $D3_{COLD}$ Power Management Event (PME) generation
- PCI arbiter supporting 7 external masters
- Reset and interrupt pins configurable for embedded host applications
- JTAG Boundary Scan
- Register compatibility with the PCI 9054 for easy software migration.

PCI 9610 Features

The PCI 9610 64-bit, 66MHz bus mastering I/O Accelerator is a high performance, general-purpose bus master device available for Motorola MPC8260 PowerQUICC II and MPC 603e/740/750 processor bus based designs. The PCI 9610 incorporates PLX's industry leading Data Pipe Architecture technology, featuring DMA engines, programmable Direct Master and Direct Slave data transfer modes, and PCI messaging functions.

Interfaces

PCI

- 64-bit, 66MHz r2.2 operation
  - Zero wait state bursts to 528 MB/s
  - Dual Address Cycle (DAC) support as a PCI bus master
  - Vital Product Data (VPD)
  - 3.3V I/O, 5V tolerant
- PCIMG 2.1 r2.0 Hot Swap Silicon
  - Programming Interface 0 (PI=0)
  - Bias Voltage Support
  - Early Power Support
  - Initially Not Responding Support
- PCI Hot Plug r1.0
- PCI Power Management r1.1
  - Supports D0, D1, D2, $D3_{HOT}$, & $D3_{COLD}$ power states
  - $D3_{COLD}$ Power Management Event (PME) generation to meet PC 2001 Windows 98/2000 communication adapter logo certification requirements

Processor Bus

- 64-bit, 66MHz operation
  - PowerPC 603e bus compatible
  - Supports direct connection to Motorola MPC8260 PowerQUICC II and MPC 603e/740/750 processors
  - Zero wait state bursts to 528 MB/s
  - 3.3V I/O, 5V tolerant
  - Asynchronous clock inputs to PCI and processor bus

Serial EEPROM

- Store configuration register power on, reset values
- An alternative to expansion ROM for storing Vital Product Data (VPD)
- Supports 2 Kbit/4 Kbit microwire devices with sequential read

Data Pipe Architecture

DMA

Service DMA descriptors, mastering on both bus interfaces during data transfer

- Four independent channels provide flexible prioritization scheme
- Each channel has its own bi-directional 32 Qword (256 byte) deep FIFO
- Block Mode services a single DMA descriptor in PCI 9610 registers
- Scatter/Gather Mode services DMA descriptor linked lists in memory
  - Burst descriptors from PCI or processor bus memory
  - Descriptor lists either linear (static) or circular (dynamic) with Valid bit semaphore control
- Direct Hardware DMA controls
  - Demand Mode to pause/resume
  - End of Transfer (EOT) to abort
- Programmable processor bus burst length, including infinite burst
  - Enhanced 603e interface supports bursts beyond PowerQUICC II 32 byte limit

Direct Master

Service processor bus masters by mastering on the PCI bus

- Two processor bus address spaces map to PCI bus: one to memory; one to I/O
- Generate all PCI memory and I/O transaction types, including Memory Write and Invalidate (MWI)
- Independent 16 Qword (128 byte) read and 32 Qword (256 byte) write FIFOs
- Read ahead and programmable read prefetch counter
- PowerQUICC II deferred reads and IDMA

Direct Slave

Service PCI bus masters by mastering on the processor bus

- Two general-purpose and one expansion ROM PCI address spaces map to processor bus memory
  - Each address space may specify 8-, 16-, 32-, or 64-bit processor bus data transfer
- Independent 16 Qword (128 byte) read and 32 Qword (256 byte) write FIFOs
- Deferred reads, deferred writes, posted writes, read ahead, and programmable read prefetch counter

Advanced Performance Features Common to DMA, Direct Master, and Direct Slave

- Zero wait state PCI & processor bus bursts
- Deep FIFOs prolong bursts
- Unaligned PCI and processor bus transfers of any byte length
- On-the-fly Endian conversion
- Programmable processor bus wait states
- Parity checking on both buses

Messaging

- Provides industry standard I_2O r1.5 messaging unit
- Supports general-purpose messaging for proprietary message schemes
  - Eight 32-bit mailbox registers for polled environments
  - Two 32-bit doorbell register for interrupt driven environments

Embedded Host Features

- PCI arbiter supports 7 external masters
- Reset and interrupt signals configurable for embedded host operation
- Type 0/1 Configuration support allows processor bus master to configure PCI bus and devices

Package

- 416-pin PBGA
  - 27 mm x 27 mm, 1.00 mm ball pitch
  - Low power 2.5V CMOS core
  - 3.3V I/O, 5V tolerant
  - Industrial temperature range operation
  - IEEE 1149.1 JTAG Boundary Scan

Compatibility

- The PCI 9610 register set is backward compatible with the PCI 9054, with new registers added for the new functionality enhancements

Related PLX Products

- Support for the Motorola MPC 850/860 PowerQUICC or generic 32-bit local buses is provided by the PCI 9054, PCI 9056, and the PCI 9656
  - See the PCI 9054, PCI 9056, and PCI 9656 product briefs for details

PCI 9610 Applications

Motorola PowerQUICC II Designs

The PCI 9610 is ideal for MPC8260-based PowerQUICC II designs. Targeted datacom and telecom applications include high-speed routers/switches, Frame Relay adapters, WAN/LAN controllers, and modem cards.

The PCI 9610 simplifies these designs by providing an enhanced direct-connect interface to the PowerQUICC II processor family. The flexible 3.3V, 5V tolerant I/O buffers, combined with 64-bit processor bus operation up to 66MHz, are ideally suited for current and future PowerQUICC II processors.

The PCI 9610 supports the PowerQUICC II IDMA channels for data transfers between the integrated PowerQUICC II communication channels and PCI.

In addition, the PCI 9610 makes use of PLX's leading edge Data Pipe Architecture technology, allowing unlimited bursts, as illustrated in the figure below.

❶ For PowerQUICC II IDMA operation, the PCI 9610 transfers data to the PCI bus under the control of the IDMA handshake protocol using Direct Master transfers.

❷ Simultaneously, the four PCI 9610 DMA channels run as masters on both buses to perform bi-directional data transfers between the processor bus and the PCI Bus.

This is a prime example of how the PCI 9610 gives PowerQUICC II designers greater flexibility in implementing multiple simultaneous I/O transfers.

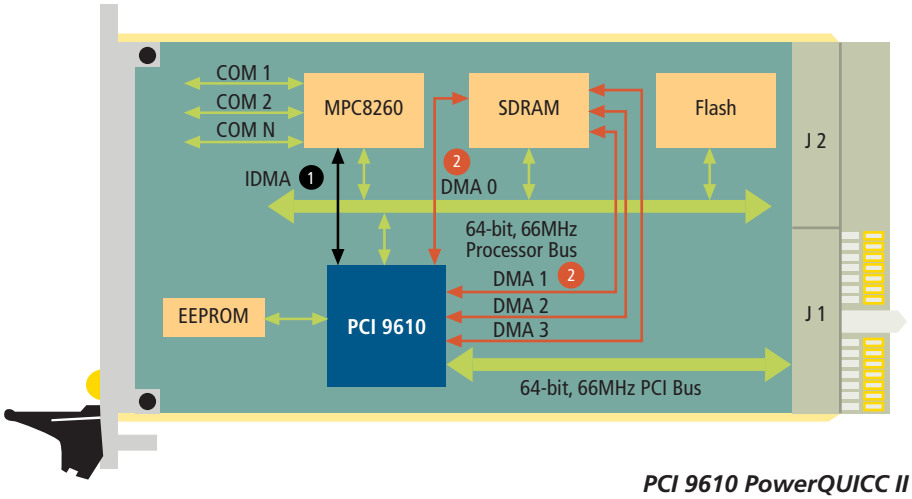
The PCI 9610 also supports any PowerPC 603e bus compliant processor such as the MPC 603e/740/750.

CompactPCI Adapters

Another key application for the PCI 9610 is CompactPCI adapters in industrial, telecom, and networking applications. These applications include WAN/LAN controllers, modem cards, Frame Relay adapters, and telephony cards for telecom switches and remote-access systems.

The PCI 9610 has integrated key features to enable live insertion and extraction of CompactPCI Hot Swap Adapters. The PCI 9610 is PICMG 2.1 r2.0 Hot Swap Silicon, supporting Programming Interface 0 (PI=0). It includes Bias Voltage and Early power support for ease of Hot Swap board design. Further, the PCI 9610 includes an option to suppress PCI target retries during chip initialization, providing the optimal behavior for live insertion in Hot Swap systems.

The PCI 9610, with its internal PCI arbiter, reset signal direction control, and Type 0/1 PCI configuration support, is also an ideal choice for CompactPCI system cards.



PCI 9610 PowerQUICC II CompactPCI Adapter

PCI Adapters

The PCI 9610 is also designed for traditional PCI adapter card applications requiring 64-bit, 66MHz PCI operation and bandwidth. Specific applications are high performance communications, networking, disk control, RAID, and data encryption adapters.

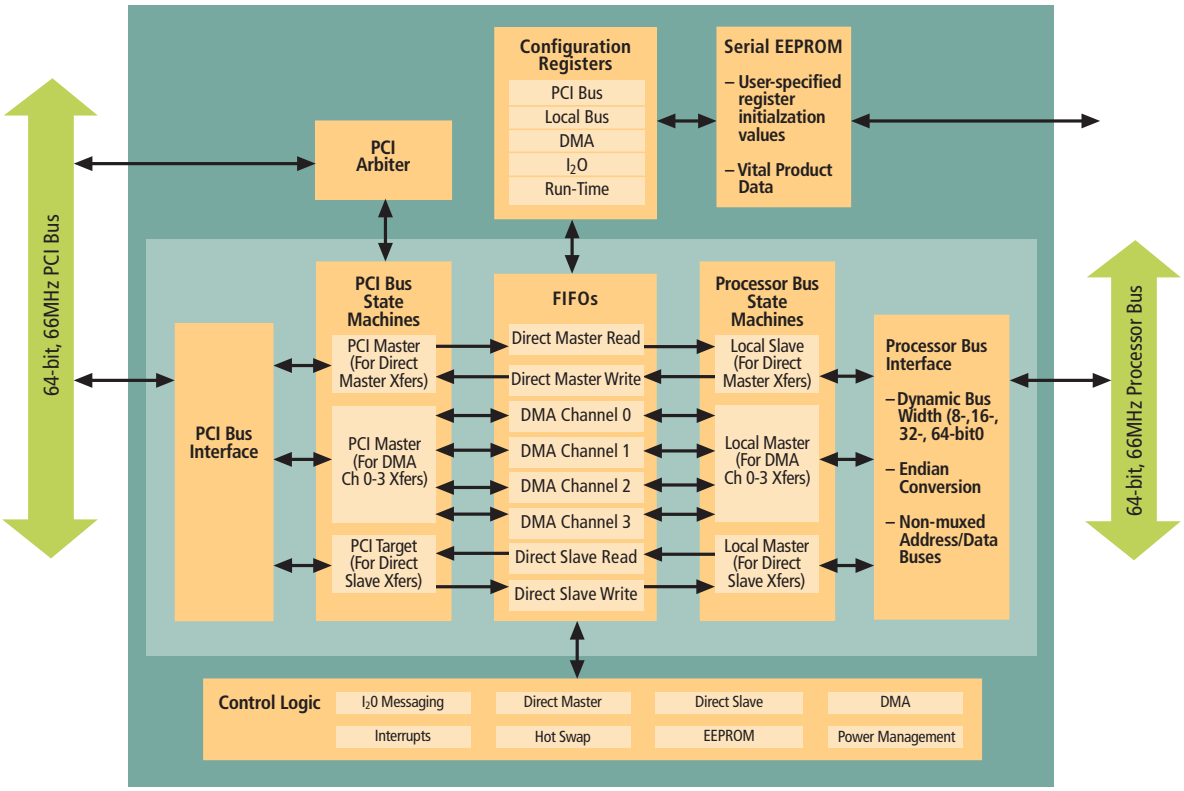
Today, Power Management and Green PCs are major initiatives in traditional PCI applications. The PCI 9610 supports PCI power management, including generation of PME in the $D3_{COLD}$ state. This is becoming a requirement for modem and communications adapters in Windows desktop and server systems.

Embedded Hosts

I/O intensive embedded host designs are another major application of the PCI 9610. These applications include network switches and routers, printer engines, set-top boxes, CompactPCI system cards, and industrial equipment.

While the support requirements of these embedded host designs share many similarities with peripheral card designs, there are three significant differences:

- A host must configure the PCI bus. The PCI 9610 supports PCI Type 0 and Type 1 configuration cycles to accomplish this.
- A host must provide a PCI bus arbiter. The PCI 9610 PCI arbiter supports seven external PCI masters, enough for a standard CompactPCI backplane with 7 peripheral slots.
- For hosts, the directions of the reset and interrupt signals reverse. The PCI 9610 includes a strapping option for reversing the directions of the PCI and processor bus reset and interrupt signals. In one setting, the directions are appropriate for a peripheral. In the other setting, they are appropriate for a host.



PCI 9610 Internal Block Diagram

Development Tools Support

To minimize risk and lower your product development costs, PLX offers Software Development Kits (SDKs) and Rapid Development Kits (RDKs) that support the PCI 9610. These kits enable designers to quickly bring new designs to production.

PLX recognizes that software often represents the largest investment in development. The PCI 9610 is fully compliant with PLX's SDK-LITE and SDK-PRO which enable quick and easy development of high performance local processor and host PCI software through standard APIs, I_2O messaging protocols, PCI debug tools, and sample drivers.

PCI 9610 design support is provided through RDKs that include a robust PCI development platform, complete with OrCAD schematics, documentation, a PCI 9610 chip sample, and software.

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Product Ordering Information

Part Number	Description
PCI 9610-AA66BI	64-bit, 66MHz PCI Bus Mastering I/O Accelerator for PowerQUICC II and MPC 603e/740/750 Processor Bus Designs
SDK-LITE	Windows Host-Side Software Development Kit for PLX I/O Accelerators and I/O Processors
SDK-PRO	Windows Host-Side and Processor Bus-Side Software Development Kit for PLX I/O Accelerators and I/O Processors