Product Features

- 2X CLK_IN on CLK_OUT
- High-Performance Phase-Locked-Loop Clock Distribution for Networking, ATM, 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/ PC applications
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Wide range of Clock Frequencies
- Package:
  Plastic 8-pin SOIC Package (W)

Product Description

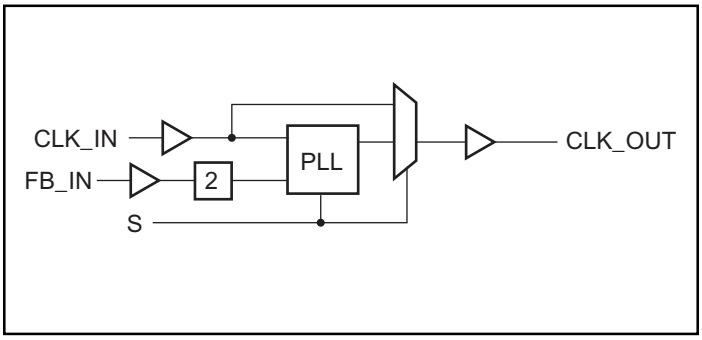
The PI6C2302 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the feedback CLK_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. The PI6C2302 provides 2X CLK_IN on CLK_OUT output.

Application

If the system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as PI6C2509Q, and PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

Notice: *This device is subject to import restriction. Please refer to the Import Restriction Notice under the Ordering Information section.*

Logic Block Diagram



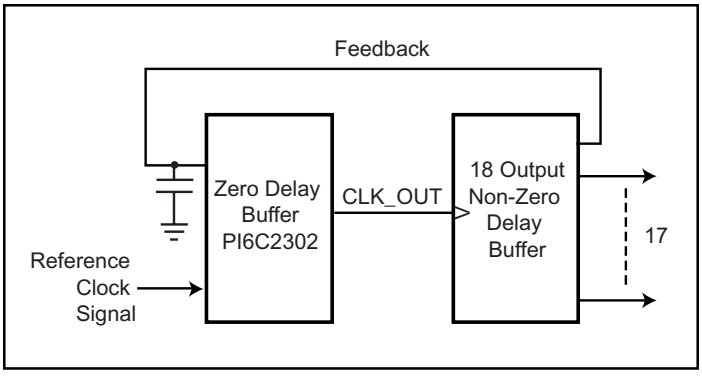
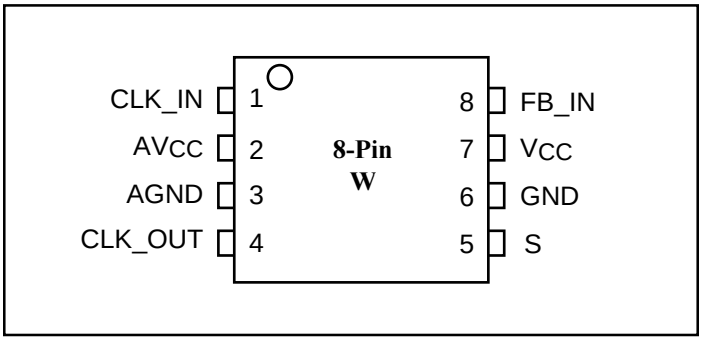


Figure 1. This Combination Provides Zero-Delay Between the Reference Clocks Signal and 17 Outputs

Product Pin Configuration



Control Input

S	Output Source	PLL Shutdown
1	PLL	N
0	CLK_IN	Y

Pin Functions

Pin Name	Pin Number	Type	Description
CLK_IN	1	I	Reference Clock input. CLK_IN allows spread spectrum clock input
AV_{CC}	2	Power	Analog power.
AGND	3	Ground	Analog ground.
CLK_OUT	4	O	Clock output. The output provides low-skew copies of CLK_IN and has an embedded series-damping resistor.
S	5	I	Control Input S. S is used to bypass the PLL for test purposes. When S is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
GND	6	Ground	Ground.
V_{CC}	7	Power	Power supply.
FB_IN	8	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.

Absolute Maximum Ratings (Over operating free-air temperature range, see Note 1)

Symbol	Parameter	Min.	Max.	Units
V_I	Input voltage range	–0.5	V_{CC} + 0.5	V
V_O	Output voltage range	–0.5	V_{CC} + 0.5	
VI_DC	DC input voltage	–0.5	+5.0	
IO_DC	DC output current		100	mA
Power	Maximum power dissipation at T_A= 55°C in still air		1.0	W
T_{STG}	Storage temperature	–65	150	°C

Note:
1. Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Recommended Operating Conditions

Symbol	Parameter	Temperature	Min.	Max.	Units
V_{CC}	Supply voltage	Commercial	3.0	3.6	V
	Supply voltage	Industrial	3.135	3.465	
V_{IH}	High level input voltage		2.0		
V_{IL}	Low level input voltage			0.8	
V_I	Input voltage		0	V_{CC}	
T_A	Operating free-air temperature	Commercial	0	70	°C
	Operating free-air temperature	Industrial	–40	85	

Electrical Characteristics

(Over recommended operating free-air temperature range)

Symbol	Test Condition	Temperature	V_{CC}	Min.	Typ.	Max.	Units
I_{CC}	$V_I = V_{CC}$ or GND; $I_O = 0$(2)	Commercial	3.6V			10	µA
	$V_I = V_{CC}$ or GND; $I_O = 0$(2)	Industrial	3.465V			10	
C_I	$V_I = V_{CC}$ or GND		3.3V		4		pF
C_O	$V_O = V_{CC}$ or GND				6		
I_{OH}	V_{OUT} = 2.4V					–18	mA
	V_{OUT} = 2.0V					–30	
I_{OL}	V_{OUT} = 0.8V			25			
	V_{OUT} = 0.55V			17			

Note:

2. Continuous Output Current

AC Specifications Timing Requirements

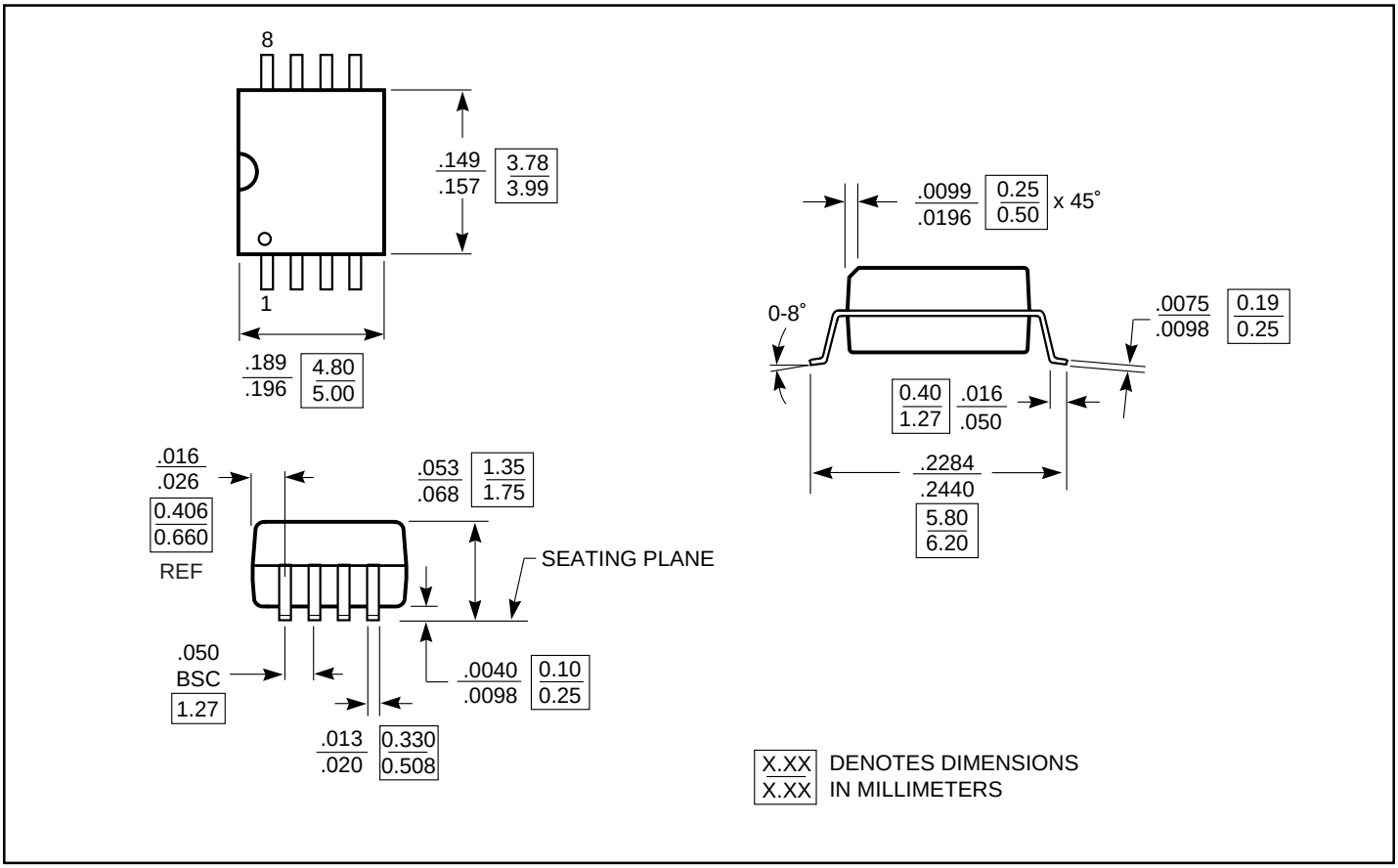
(Over recommended ranges of supply voltage and operating free-air temperature, C_L = 25pF)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
F_{CLOCK}	Clock frequency	Commercial	25		134	MHz
	Clock frequency	Industrial	25		100	
D_{CYI}	Input clock duty cycle		40		60	%
	Stabilization time after power up				1	ms
t_p	Phase error without jitter(3)	CLK_IN↑ at 100MHz and 66MHz	–150		+150	ps
tj	Jitter, cycle-to-cycle	At 100MHz and 66MHz	–100		+100	
	Duty cycle		45		55	%
t_r	Rise-time, 0.4V to 2.0V			1.0		ns
t_f	Fall-time, 2.0V to 0.4V			1.1		

Note:

3. This switching parameter is guaranteed by design.

8-pin Plastic SOIC (W) Package



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2302W	W8	8-pin 150-mil SOIC	Commercial
PI6C2302-WI	W8	8-pin 150-mil SOIC	Industrial

Import Restriction Notice:

Due to an agreement to settle a patent dispute, this device is only available for sale outside of the US and may not be subsequently re-imported into the US as an individual component or as incorporated into equipment. Any sale is expressly conditioned on the customer's agreement not to export the device or any product or equipment containing the device to the United States. Pericom disclaims any liability for indemnity or other obligation or warranty if the devices or any product or equipment containing the devices are imported in violation of this agreement.