CATALINA RESEARCH INCORPORATED
A PARAVANT COMPANY

Pathfinder-2
ASIC

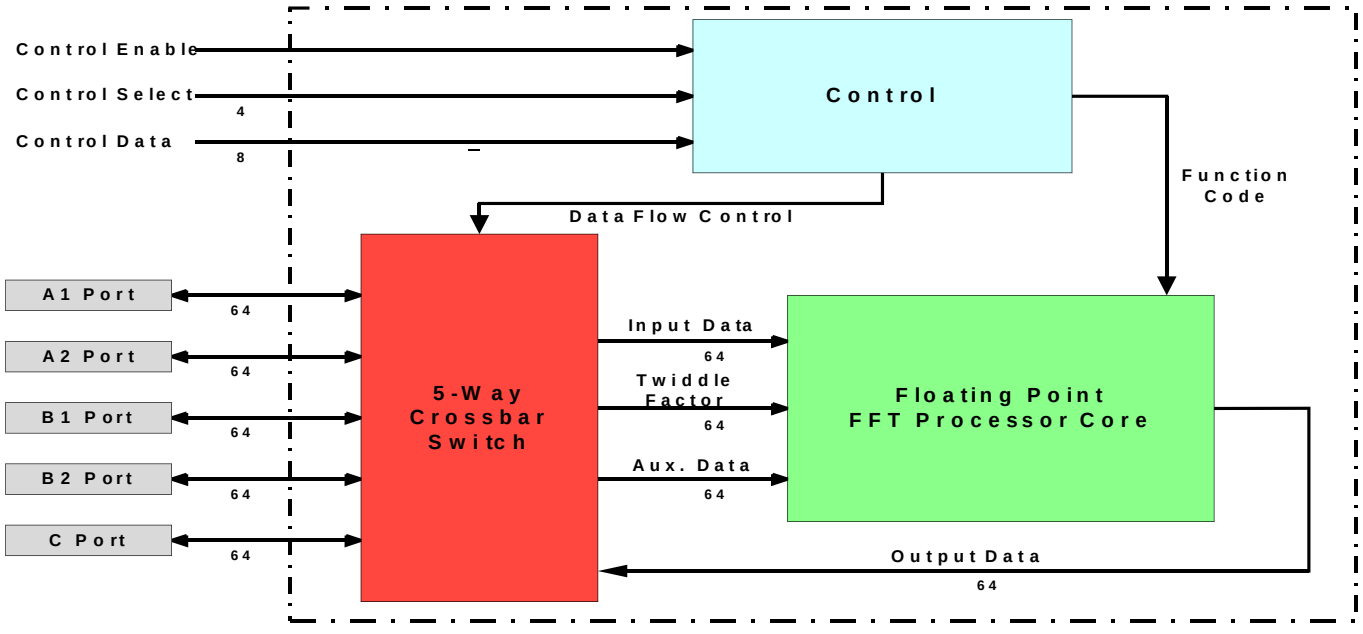
Applications

- Communications
- Digital filtering
- Correlations and convolutions
- Imaging processing
- Instrumentation
- Polyphase filtering
- Pulse compression
- Radar/sonar signal processing
- SAR processing
- Signal intelligence
- Spectrum analysis

Key Features

- 133 MHz clock
- 5.3 GFLOPS
- 4.26 GByte/sec sustainable memory bandwidth
- 3.3V I/O, 2.5V core
- Synchronous system design 0.25 micron CMOS four-layer metal process
- 32-Bit IEEE floating point arithmetic
- Distributed internal scaling minimizes round-off errors
- Five 64-bit data ports
- Internal twiddle factor generator
- Five-way crossbar switching
- Radix 16, 32, 64, 128, 256 for real and complex data
- Free window or filter multiplications with the first pass or an FFT or IFFT for all radix sizes, real or complex
- Designed in VHDL
- 576-Pin SBGA package
- Compatible with CRI's Sojourner-3 address generator (AG)

Pathfinder-2 Block Diagram



General Description

Pathfinder-2 is optimized for computing general-purpose frequency-domain functions such as FFTs, IFFTs, real and complex multiplies, correlations, fast convolutions, and polyphase filters. Its high precision and handling of internal scaling enables Pathfinder-2 to process large vector sizes (up to 1 million complex samples) with dynamic range unmatched by any other commercially-available FFT processing integrated circuit.

Pathfinder-2 provides a multi-port data flow structure designed to support concurrent I/O and processing, making the chip an excellent match for applications requiring very fast data throughput rates. Multiple Pathfinder-2 DSPs can be cascaded to support continuous data rates of 133 million complex samples per second or 240 million real samples per second for up to one million point transfers.

The Pathfinder-2 integrated circuit is built up from multiple complex multiplication stages and four radix-four cores. Pathfinder-2 can accept and produce data in either 32-bit integer or IEEE floating point format. Pathfinder-2's internal arithmetic elements use floating point adders and multipliers for increased dynamic range and precision. The internal floating point element's word width has been optimized for speed, area and precision. Pathfinder-2 also incorporates an internal sine/cosine (twiddle) generator. The generator enables Pathfinder-2 to compute up to 1 million point complex or 2 million point real FFTs with no external twiddle factor required. External twiddle factors or coefficients may also be supplied for windowing, fast convolution, etc.

Pathfinder-2 provides five bi-directional I/O ports. The chip allows full cross-bar multiplexing on all five ports, enabling very flexible system designs and algorithm implementation. One benefit of the five port architecture is that cascaded processor designs become straightforward to implement. Another benefit of the port architecture is that no port needs to be designated exclusively as a coefficient port. Windows and filters may be stored in any memory bank connected to any of the five ports, and may be accessed at any time during processing.

The results from any processing pass may be broadcast simultaneously to up to two separate ports. This feature is useful for implementing algorithms where the intermediate results of a vector operation need to be stored and used later in the process, as it cuts down on the number of processing passes required. For example, previous FFT chip architectures required that results of a process pass flow into specific memories. Additional processing passes were necessary to move an intermediate result to other memory banks so it could be used later in the process. Since Pathfinder-2 has full cross-bar multiplexing on all five bidirectional ports, the need for extra move passes is eliminated thus increasing the performance of these types of algorithms.

Specifications

Power:

Max. current at 3.3V	0.15 A
Max. current at 2.5V	2.0 A

Processing Speed:
133 MHz clock rate

Performance:
The table below lists the performance of a single Pathfinder-2 running at 133 MHz for FFT sizes from 16 points to 1 million points (complex). For even greater performance than the unstacked FFT times shown below, FFTs with 256 points or less can be stacked for dramatic increases in throughput. Multiple Pathfinder-2 chips may be cascaded to support continuous data rates of 133 million complex samples per second or 240 million real samples per second for up to one million point transforms.

Complex FFT Size	FFT Time (microseconds)	Complex MSPS
16	1.1	14.4
32	1.4	23.1
64	1.9	34.3
128	2.9	44.8
256	4.6	55.4
512	9.8	52.1
1024	17.7	57.9
2048	33.3	61.5
4096	64.4	63.6
8192	126.5	64.8
16384	250.2	65.5
32768	497.3	65.9
65536	990.9	66.1
131072	2960.4	44.3
262144	5917.2	44.3
524288	11830.7	44.3
1048576	23657.3	44.3

Environment:

Junction temperature:	0 - 90 degrees C
Power dissipation:	6W at 133 MHz

Part Numbers:
Contact CRI for ordering information.

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