APPLICATION NOTE

AN258

PTN3310/3311 board

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PTN3310/3311 board

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PTN3310/3311 BOARD

The PTN3310/3311 board utilizes two logic translator from the PTN product portfolio– the PTN3311, a PECL to LVDS translator, and the PTN3310– a LVDS to PECL translator. For more information on the ICs, please, refer to their corresponding data sheets.

The board is designed for an optimum evaluation of both parts. With the assemble or dissemble of some resistors, the board could operate in the following modes— PTN3311 driving PTN3310, PTN3310 driving PTN3311, or both parts operating independently.

For the PTN3311 to drive the PTN3310, the input signal from the pattern generator must be connected to SMA J1 and SMA J2, and resistors R5 & R6, R13 & R14, and R15 & R16 must be mounted on the board, while resistors R21 & R22, R7 & R9, and R8 & R10 should be disassembled. The output signal could be taken to the oscilloscope via SMAs J7 and J8.

For the PTN3310 to drive PTN3311, the input signal must be connected to SMA J5 and SMA J6, with resistors R7 & R9, R8 & R10, and R21 and R22 assembled on the board, whereas R5 & R6, R13 & R14, and R15 & R16 should be dismounted. The output signal could be viewed via SMAs J3 and J4.

For the two parts to be evaluated independently, all resistors, except R8 and R10 should be mounted on the board. In this case the input signal for the PTN3310 will be provided via SMAs J5 and J6, and for the PTN3311 it will be via SMAs J1 and J2. The corresponding outputs of the parts could be connected to oscilloscope through SMAs J7 & J8 and J3 & J4 for PTN3310 and PTN3311 respectively.

In the following appendix, attached are:

- Bill of materials

- Schematic

- Top layer layout and silk screen

SUPPORT

For further information, please, check www.philipslogic.com/networking or e–mail to PTN–Support@philips.com

To inquire about the availability of this board, please visit http://www.philipslogic.com/products/ptn/evalboards/rqstptn

To learn about other PTN boards, please visit http://www.philipslogic.com/products/ptn/evalboards

APPENDIX

BILL OF MATERIAL

Item	Quantity	Reference	Part
1	2	BN2,BN1	Banana–Plug
2	1	C1	Capacitor, 10 μF
3	8	C2,C3,C4,C5,C10,C11,C12, C13	Capacitor, 0.01 μF
4	4	C6,C7,C8,C9	Capacitor, 0.1 μF
5	8	J1,J2,J3,J4,J5,J6,J7,J8	SMA Connector
6	3	R4,R1	Resistor, 100 Ω
7	4	R2,R3,R17,R19	Resistor, 82.5 Ω
8	12	R5,R6,R7,R8,R9,R10,R13, R14,R15,R16,R21,R22	Resistor, 0 Ω
9	4	R11,R12,R18,R20	Resistor, R127 Ω
10	1	U1, PTN3311	PECL–LVDS Translator
11	1	U2, PTN3310	LVDS–PECL Translator
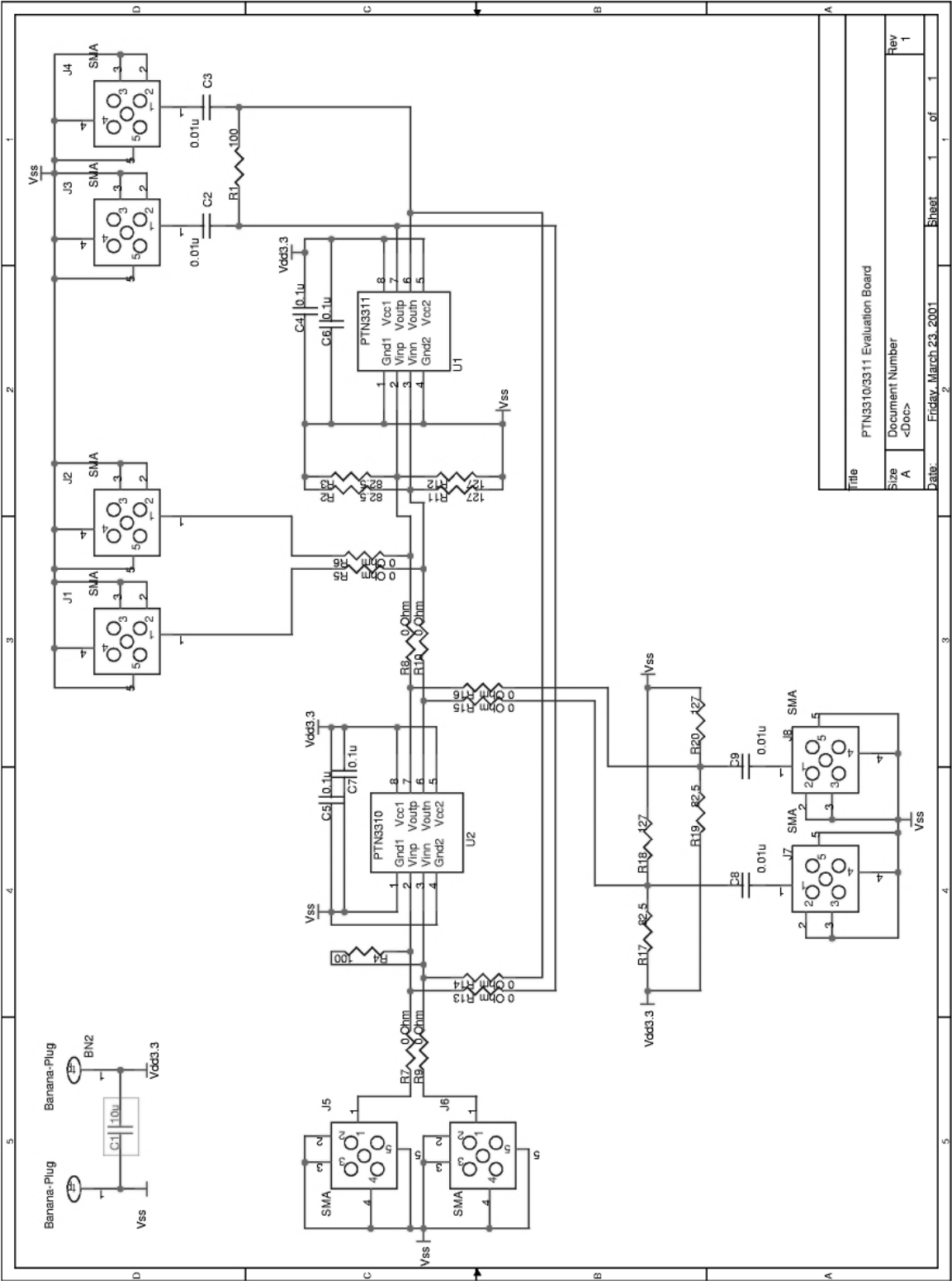
SCHEMATIC

TOP LAYER LAYOUT AND SILK SCREEN
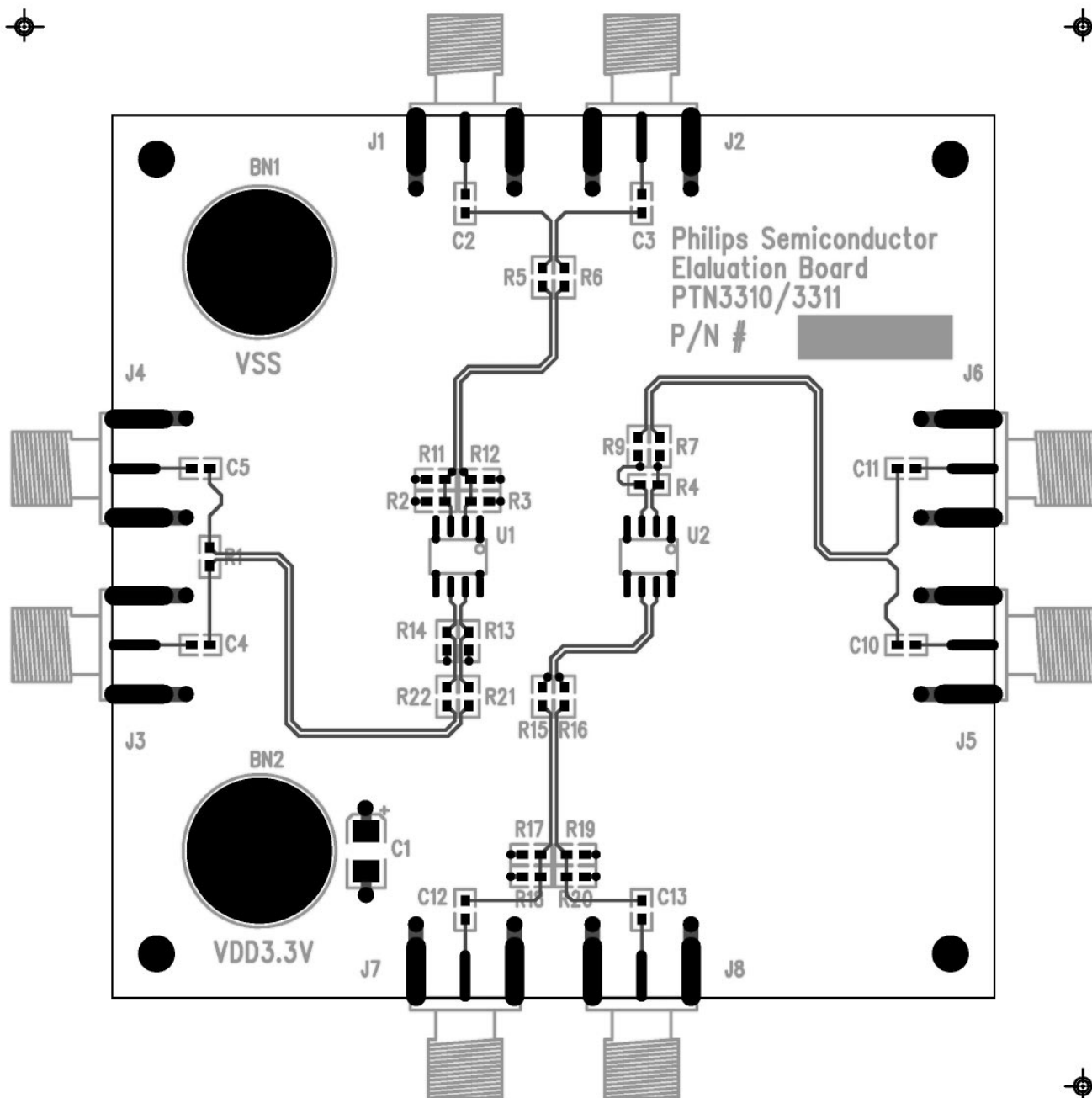
Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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