

MTSI and HTSI(M-mode)

Switching IC

PEF 20450/20470/24470

PEF 20451/20471/24471

Switch from MTSX Family to SWITI  
Family

Wired  
Communications



**PEF 20450/20470/24470**

**PRELIMINARY**

**Revision History:**            **2001-11-23**

**DS1**

Previous Version:            <Date of last issue>

Page	Subjects (major changes since last revision)

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at <http://www.infineon.com>

<b>Table of Contents</b>		<b>Page</b>
<b>1</b>	<b>Introduction</b>	<b>1</b>
<b>2</b>	<b>Overview of MTSI and HTSI (M-mode) Family</b>	<b>2</b>
<b>3</b>	<b>Basic Differences between MTSX and SWITI Family</b>	<b>3</b>
3.1	Subchannel Switching	3
3.2	Clock Considerations	4
3.3	Message Mode	4
3.4	Connection Management	5
3.5	Software	5
<b>4</b>	<b>Specific Differences between MTSX and MTSI/HTSI Family</b>	<b>6</b>
4.1	General Overview	6
4.2	MTSS (PEB 2046) and MTSI (PEB 20450)	7
4.3	MTSC (PEB 2045) and MTSI (PEF 20450)	8
4.4	MTSL (PEB 2047) and MTSI (PEF 20470)	9
4.5	MTSXL (PEB 2447) and MTSI-XL (PEF 24470), HTSI-XL (PEF 24471) M-Mode.	10
<b>5</b>	<b>Available Tools</b>	<b>12</b>
5.1	SMART 24471 Evaluation Board	12
5.2	DAvE Configurator	13

## 1 Introduction

Compared to the MTSX the SWITI family offers extended functions like subchannel switching, constant delay, etc. In general the product family can be divided into 2 groups: the MTSI devices for standard switching and the HTSI devices for computer telephony integration (CTI) applications. The HTSI devices can again be operated in 2 different modes: the H-mode and the M-mode. In M-mode the HTSI devices operate equivalent to the MTSI devices, but have extended PCM interface (extended number of PIN). The HTSI and MTSI devices are offered in different packages.

The following application note gives an overview of the features of MTSI and HTSI (M-mode) devices and compares with conventional switching devices like MTSX and MTSI. In this application note MTSX stands for MTSS, MTSC, MTSL or MTSXL devices.

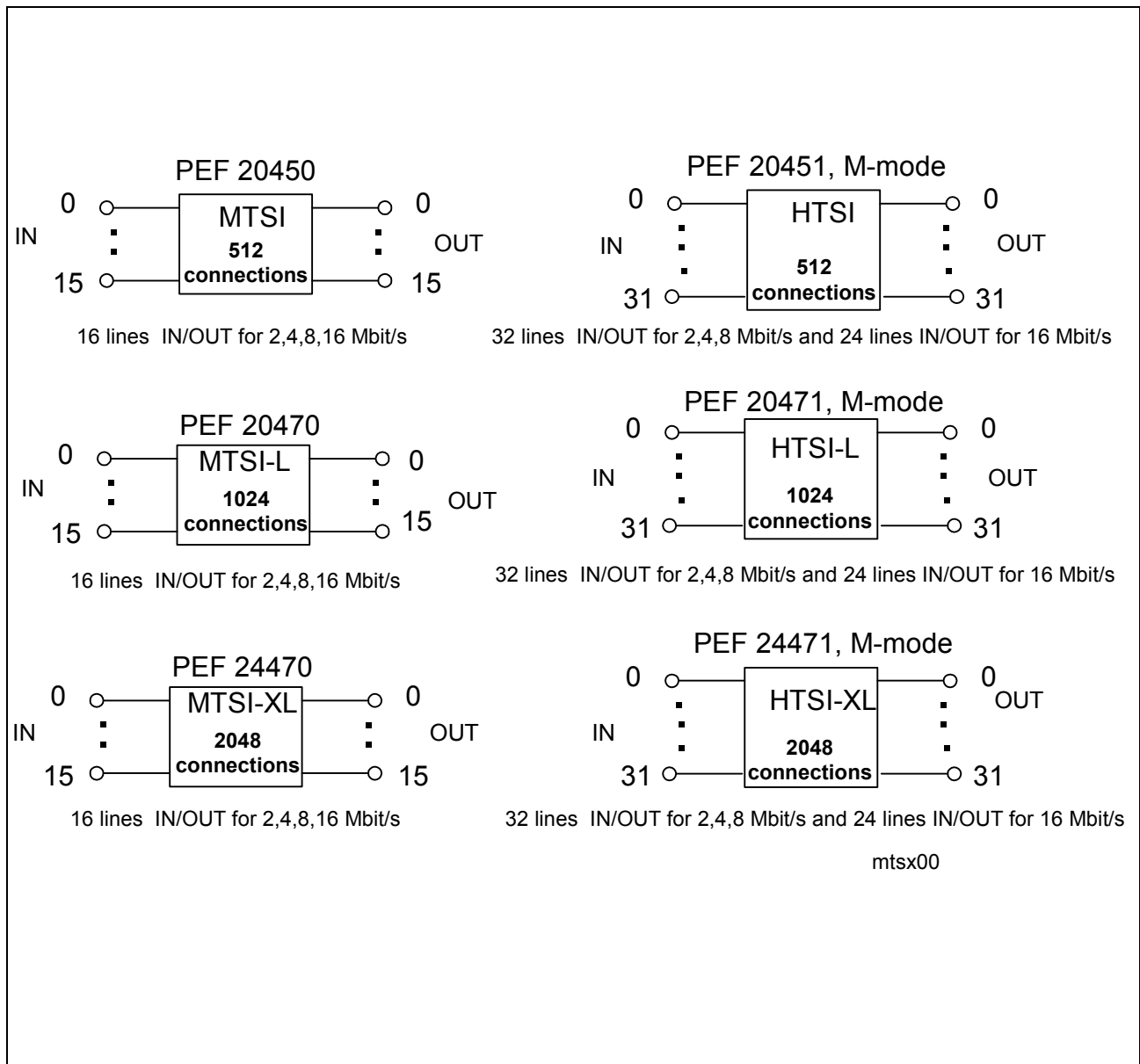
*Note: The MTSX devices are not recommended for new designs and will be discontinued after September 30th, 2002.*

**Table 1 SWITI Family Tree**

Name	Package	Sales code	Connections	Local bus IN/OUT	H-Bus IO
HTSI-XL (H-Mode)	P-BGA-217-1	PEF24471 HTSI-XL	2048	16/16	32
HTSI-XL (M-Mode)		PEF24471 HTSI-XL		32/32	-
HTSI-L (H-Mode)	P-BGA-217-1	PEF20471 HTSI-L	1024	16/16	32
HTSI-L (M-Mode)		PEF20471 HTSI-L		32/32	-
HTSI (H-Mode)	P-BGA-217-1	PEF20451 HTSI	512	16/16	32
HTSI (M-Mode)		PEF20451 HTSI		32/32	-
MTSI-XL	P-MQFP-100-2	PEF24470 MTSI-XL	2048	16/16	-
MTSI-L	P-MQFP-100-2	PEF20470 MTSI-L	1024	16/16	-
MTSI	P-MQFP-100-2	PEF20450 MTSI	512	16/16	-

## 2 Overview of MTSI and HTSI (M-mode) Family

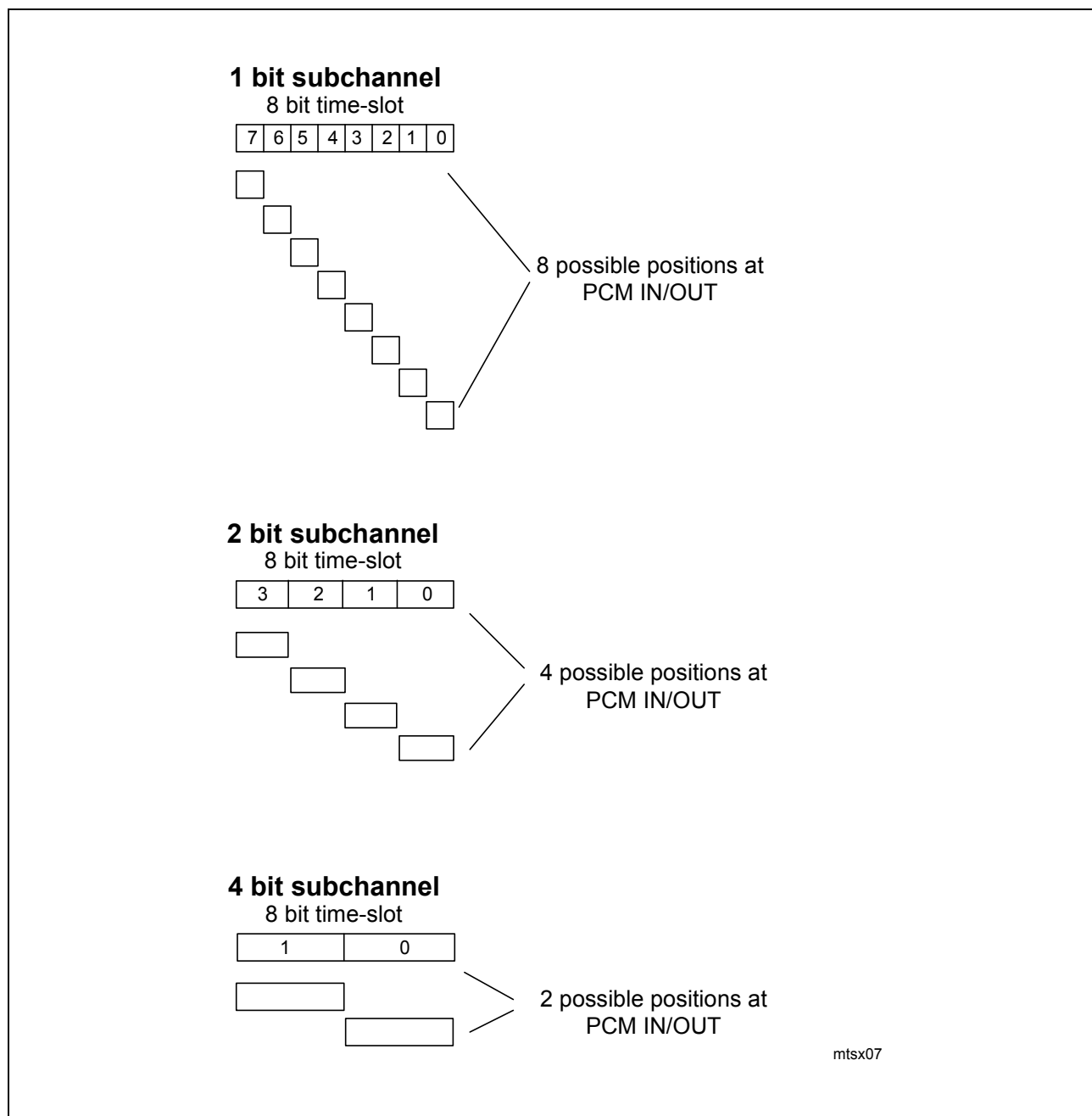
Figure 2 shows the SWITI MTSI and HTSI product family with its device types, the switching capability and the number of PCM lines. Here all HTSI devices are operated in M-mode



**Figure 1 Overview of SWITI MTSI and HTSI (M-mode) devices**

## 3 Basic Differences between MTSX and SWITI Family

### 3.1 Subchannel Switching



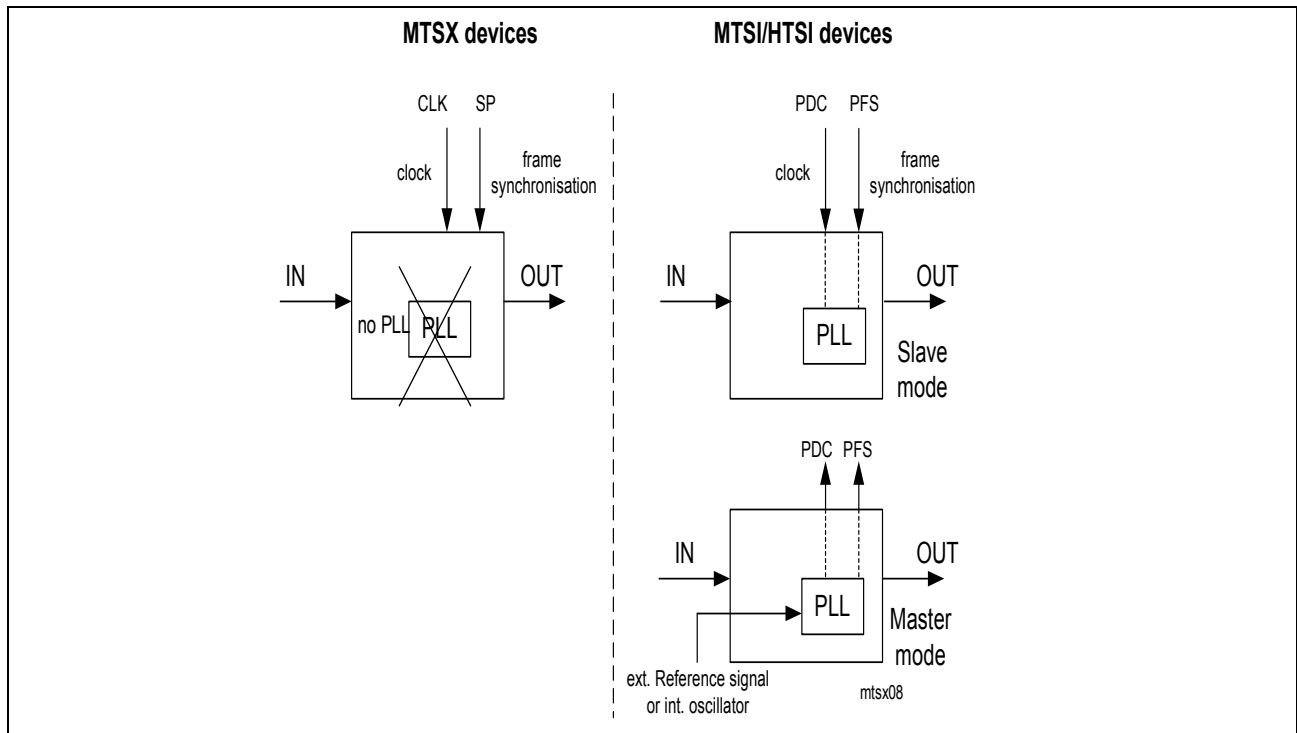
**Figure 2 Possible Subchannel positions on PCM IN and PCM OUT**

The MTSX family switches all time-slots as 8-bit channels. The MTSI/HTSI devices additionally offer subchannel switching of 1-, 2-, or 4-bit channels.

PRELIMINARY

Basic Differences between MTSX and SWITI Family

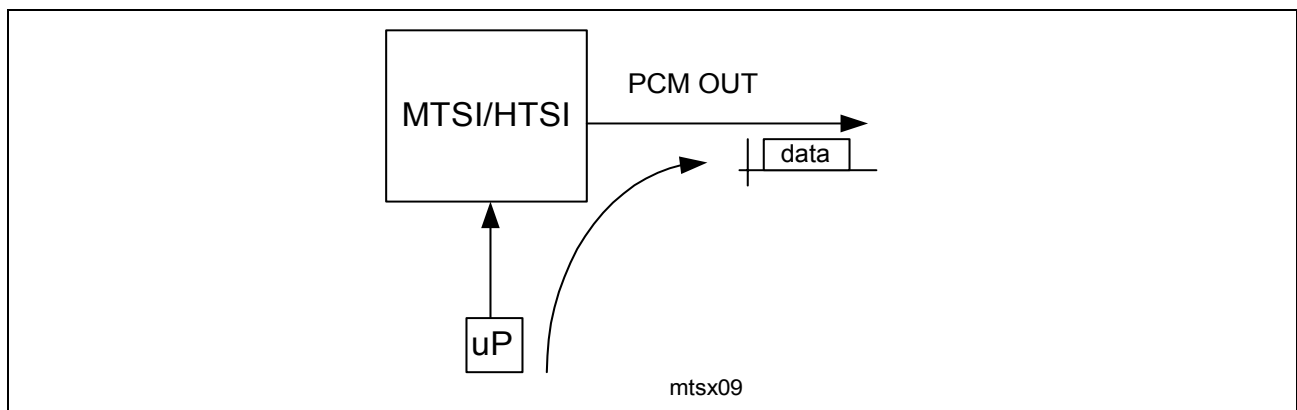
### 3.2 Clock Considerations



**Figure 3 Comparison of the Clocking Principle**

In case of MTSI/HTSI family master and slave mode has to be distinguished. Data rate vs PDC clock frequency relations are possible where even lower clock rates are possible.

### 3.3 Message Mode



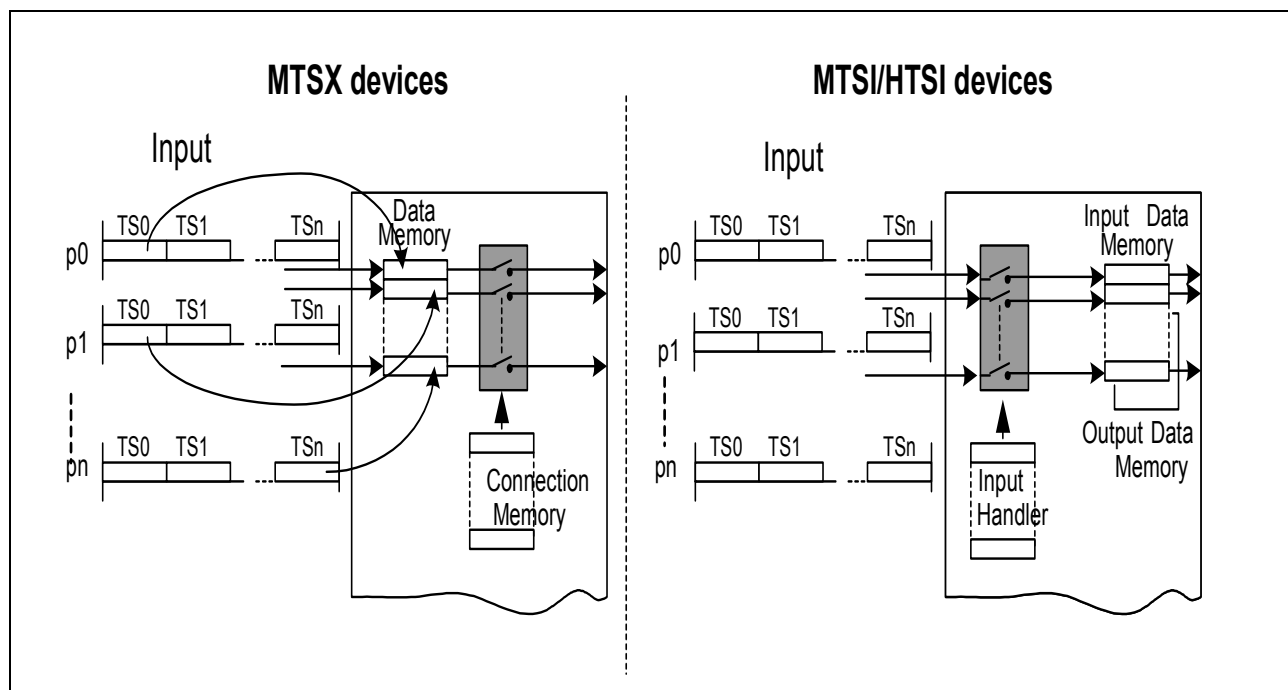
**Figure 4 Message Mode with MTSI/HTSI Devices.**

Data, which should be sent via the PCM line can be written directly through the  $\mu$ C interface into the data memory.

PRELIMINARY

Basic Differences between MTSX and SWITI Family

### 3.4 Connection Management



**Figure 5 Contrasts of Connection Management for MTSX and MTSI/HTSI Family**

In case of MTSX devices first of all incoming data are stored sequentially in a data memory. The content of the connection memory then decides which data is supposed to be switched. The advantage of this principle is the simplicity of realization. The disadvantage is the limited size of the data memory.

The MTSI/HTSI family is based on a different principle. Only those data are stored, which are to be switched. This is based on the principle of linked lists. The advantage of this method is the extended connection possibilities of PCM input data. The disadvantage is the increased complexity of this realization and increased time to establish or delete a connection and the necessity of a “handshake” for writing into the connection memory.

### 3.5 Software

Programming of the MTSX devices is based on a three step access such as write data, address and control word. The time-slots and ports are encoded in one or two bytes.

With the new MTSI family, connections are quite easy to establish. There are special registers for input time-slot, input port, output time-slot, output port and with the Connection Command Register the connection is executed.



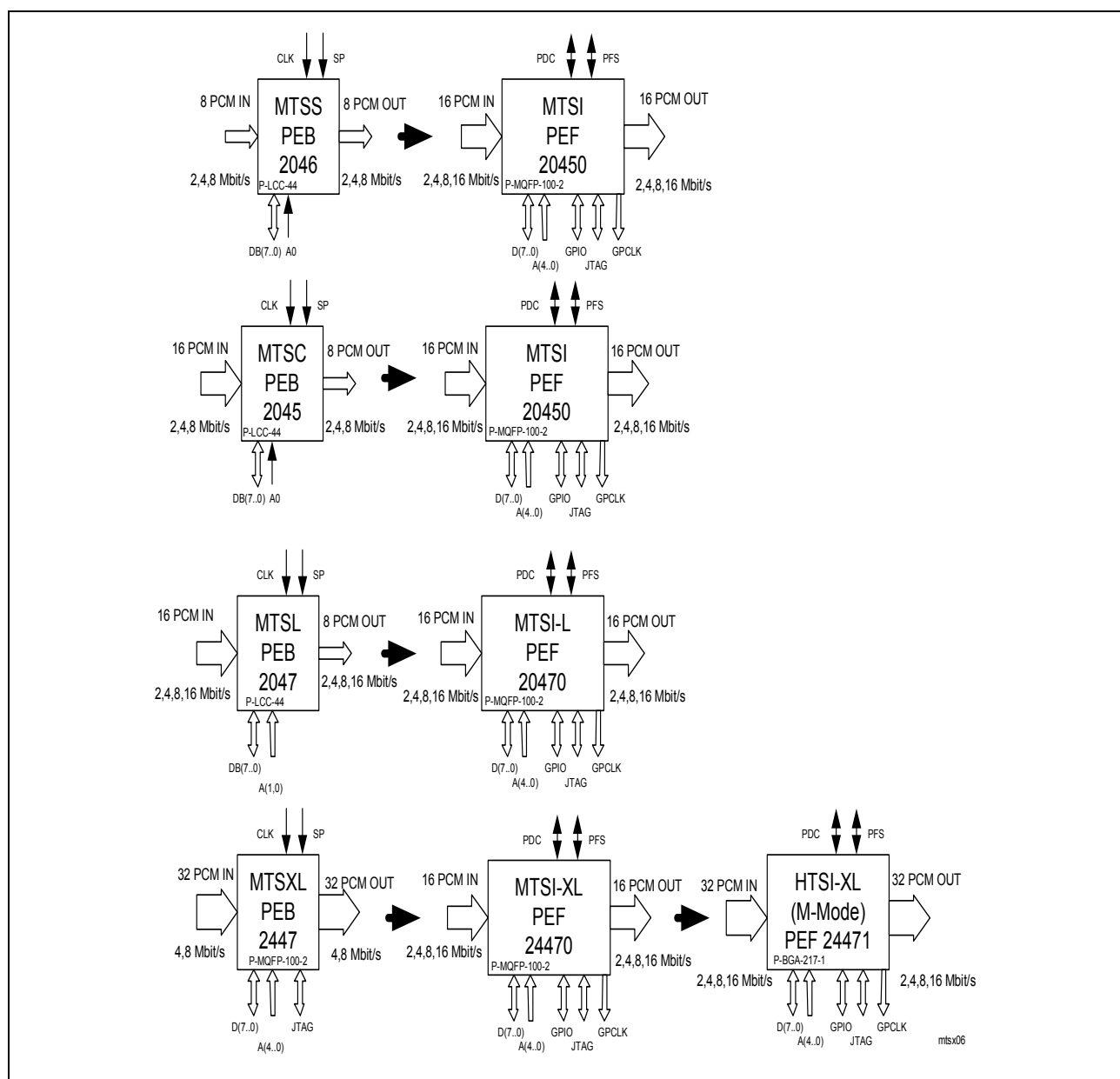
PRELIMINARY

Specific Differences between MTSX and MTSI/HTSI Family

## 4 Specific Differences between MTSX and MTSI/HTSI Family

### 4.1 General Overview

The picture gives a review of the relation between the devices MTSS, MTSC, MTSL, MTSXL and the new MTSI/HTSI (M mode) devices.

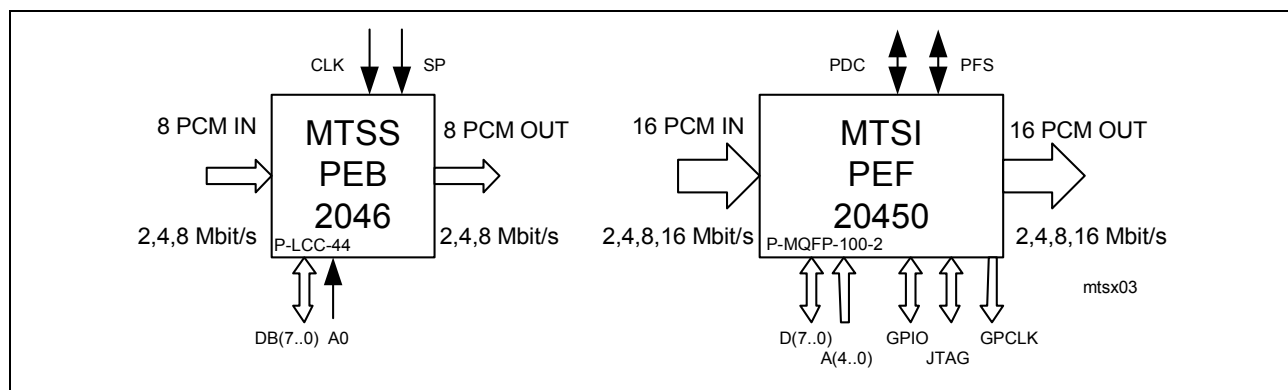


**Figure 6 Relation between MTSX devices and MTSI/HTSI (M-Mode) family**

The choice in MTSI/HTSI case is not dependent on the data rate or number of lines but on the number of necessary active connections in the system.

**PRELIMINARY**      **Specific Differences between MTSX and MTSI/HTSI Family**

## 4.2 MTSS (PEB 2046) and MTSI (PEF 20450)



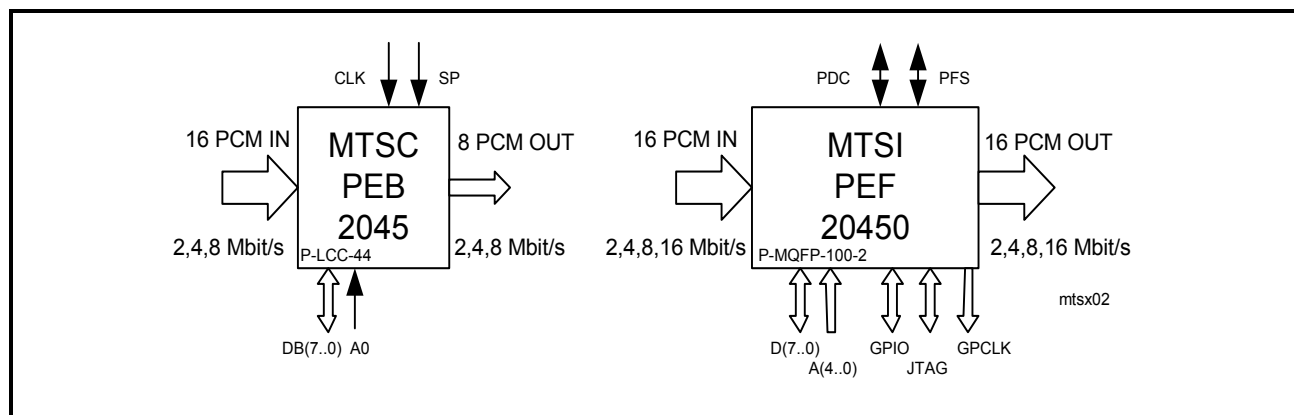
**Figure 7**      **Logic Symbol PEB 2046 and PEF 2045**

**Table 2**      **Comparison of MTSS (PEB 2046) and MTSI (PEF 20450)**

Feature	MTSS PEB 2046	MTSI PEF 20450
Package	P-LCC-44	P-MQFP-100-2
PCM line	8 PCM IN, 8 PCM OUT	16 PCM IN, 16 PCM OUT
Switching capacity	256 time-slot PCM IN 256 time-slot PCM OUT	512 time-slot PCM IN 512 time-slot PCM OUT
Possible data rates	2.048/4.096/8.192 Mbit/s	2.048/4.096/8.192/16.384 Mbit/s
Clock Master/Slave	Slave (CLK,SP are inputs)	Master (PDC,PFS are outputs) or Slave (PDC,PFS are inputs)
Subchannels	no	1,2,4-bit
Min. delay	yes	yes
Const. delay	no	yes
Read and write to all time-slots (data memory)	no	yes
Programmable clock/data shift with half clock step resolution	Programmable clock shift in half clock step resolution	Bit shift with half bit resolution
uP interface	8-bit	8 or 16-bit
Supply voltage	5 V	3.3 V
I/O Voltage compatibility	5 V	5 V/3.3 V
Power consumption	approx. 50 mW	approx. 300 mW

**PRELIMINARY**      **Specific Differences between MTSX and MTSI/HTSI Family**

### 4.3 MTSC (PEB 2045) and MTSI (PEF 20450)



**Figure 8**      **Logic Symbol PEB 2045 and PEF 20450**

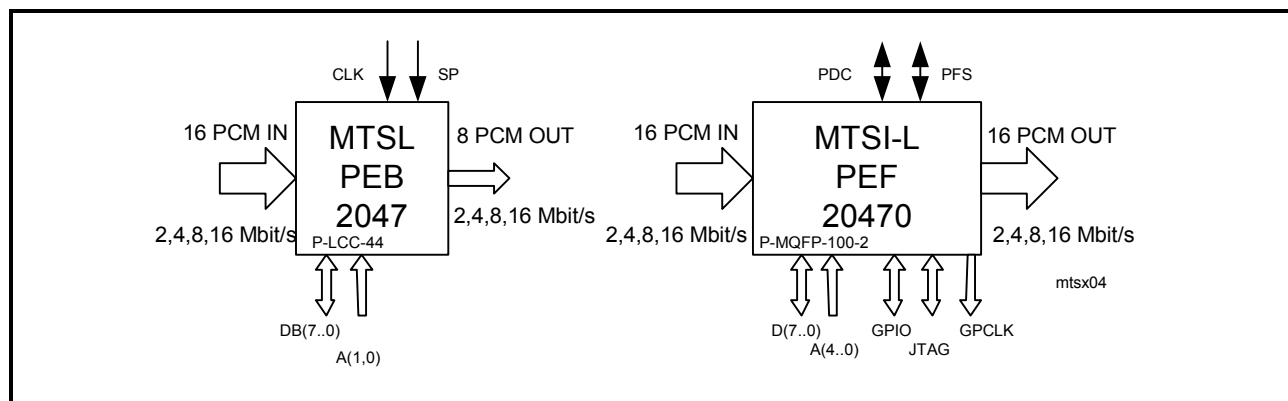
**Table 3**      **Comparison of MTSC (PEB 2045) and MTSI (PEF 20450)**

Feature	MTSC PEB 2045	MTSI PEF 20450
Package	P-LCC-44	P-MQFP-100-2
PCM line	16 PCM IN, 8 PCM OUT	16 PCM IN, 16 PCM OUT
Switching capacity	512 time-slot PCM IN 256 time-slot PCM OUT	512 time-slot PCM IN 512 time-slot PCM OUT
Possible data rate	2.048/4.096/8.192 Mbit/s	2.048/4.096/8.192/16.384 Mbit/s
Clock Master/Slave	Slave (CLK,SP are inputs)	Master (PDC,PFS are outputs) or Slave (PDC,PFS are inputs)
Subchannels	no	1,2,4-bit
Min. delay	yes	yes
Const. delay	no	yes
Read and write to all time-slots (data memory)	no	yes
Programmable clock/ data shift with half clock step resolution	Programmable clock shift in half clock step resolution	Bit shift with half bit resolution
uP interface	8-bit	8 or 16-bit
Supply voltage	5 V	3.3 V
I/O Voltage compatibility	5 V	5 V/3.3 V
Power consumption	approx. 30 mW	approx. 300 mW

PRELIMINARY

Specific Differences between MTSX and MTSI/HTSI Family

#### 4.4 MTSL (PEB 2047) and MTSI (PEF 20470)



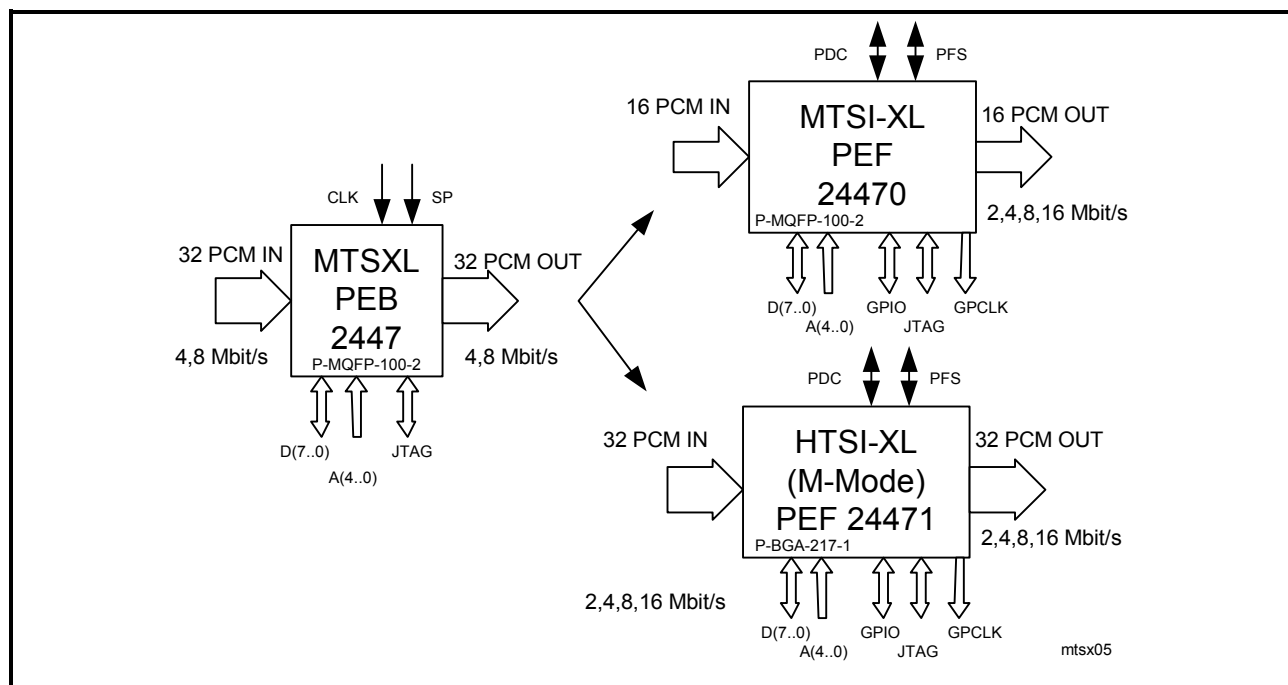
**Figure 9 Logic Symbol PEB 2047 and PEF 20470**

**Table 4 Comparison of MTSL(PEB 2047) and MTSI-L (PEF 20470)**

Feature	MTSL PEB 2047	MTSI-L PEF 20470
Package	P-LCC-44	P-MQFP-100-2
PCM line	16 PCM IN, 8 PCM OUT	16 PCM IN, 16 PCM OUT
Switching capacity	1024 time-slot PCM IN 1024 time-slot PCM OUT	1024 time-slot PCM IN 1024 time-slot PCM OUT
Possible data rate	2.048/4.096/8.192/16.384 Mbit/s	2.048/4.096/8.192/16.384 Mbit/s
Clock Master/Slave	Slave (CLK,SP are inputs)	Master (PDC,PFS are outputs) or Slave (PDC,PFS are inputs)
Subchannels	no	1,2,4-bit
Min. delay	yes	yes
Const. delay	yes, limited	yes
Read and write to all time-slots (data memory)	read-access	yes
Programmable clock/ data shift with half clock step resolution	input: range is 32 steps after SP puls output: range is 16 steps after SPpuls	Bit shift with half bit resolution
uP interface	8-bit	8 or 16-bit
Supply voltage	5 V	3.3 V
I/O Voltage compatibility	5 V	5 V/3.3V
Power consumption	approx. 50 mW	approx. 400 mW

**PRELIMINARY**      **Specific Differences between MTSX and MTSI/HTSI Family**

**4.5      MTSXL (PEB 2447) and MTSI-XL (PEF 24470), HTSI-XL (PEF 24471) M-Mode.**



**Figure 10      Logic Symbol PEB 2447 and PEF 24470, PEBF 24471**

**Table 5      Comparison of MTSXL (PEB 2447) and MTSI-XL (PEF 24470)/HTSI-XL (PEF 24471)**

Feature	MTSXL PEB 2447	MTSI-XL PEF 24470 HTSI-XL PEF 24471
Package	P-MQFP-100-2	P-MQFP-100-2 P-BGA-217-1
PCM line	32 PCM IN, 32 PCM OUT	16 PCM IN, 16 PCM OUT 32 PCM IN, 32 PCM OUT
Switching capacity	2048 time-slots PCM IN 2048 time-slots PCM OUT	2048 time-slots PCM IN 2048 time-slots PCM OUT
Possible data rate	4.096/8.192 Mbit/s	2.048/4.096/8.192/16.384 Mbit/s
Clock Master/-Slave	Slave (CLK, SP are inputs)	Master (PDC, PFS are outputs) or Slave (PDC, PFS are inputs)
Subchannels	no	1, 2, 4-bit
Min. delay	yes	yes

**PRELIMINARY**      **Specific Differences between MTSX and MTSI/HTSI Family**

**Table 5**      **Comparison of MTSXL (PEB 2447) and MTSI-XL (PEF 24470)/HTSI-XL (PEF 24471) (cont'd)**

<b>Feature</b>	<b>MTSXL PEB 2447</b>	<b>MTSI-XL PEF 24470 HTSI-XL PEF 24471</b>
Const. delay	no	yes
Read and write to all timeslots (data memory)	read-access only	yes
Programmable clock/ data shift with half clock step resolution	input: range is 32 steps after SP puls. output: range is 32 steps after SPpuls	Bit shift with half bit shift resolution
uP interface	8-bit	8 or 16-bit
Supply voltage	5 V	3.3 V
I/O Voltage compatibility	5 V	5 V/3.3 V
Power consumption	approx. 500 mW	approx. 500 mW

## 5 Available Tools

### 5.1 SMART 24471 Evaluation Board

The Switching IC (SWITI) of course is the core of this Evaluation Board. It is controlled and programmed via the microcontroller interface. The PCM interface connects SWITI with QuadFALC and the ARCOFIs. For CT Bus a special H.100 connector is provided. All functional pins of the SWITI are accessible at header pins for measurement purposes.

With the Mainboard Connector the Evaluation Board is connected to the SMART 2000 Mainboard. Together with the WinEASY-Software the SMART 2000 is an evaluation platform for different Add-On Modules (AOM). Device Driver Software can be downloaded to the SMART 2000 Mainboard and runs on a Siemens C165 microcontroller.

Two Audio Ringing Codec Filter (ARCOFI) are integrated in the system and connected to the PCM-Highway. Their Analog Front End (AFE) is used to connect handsets to the board, thus a "real" phone call is possible.

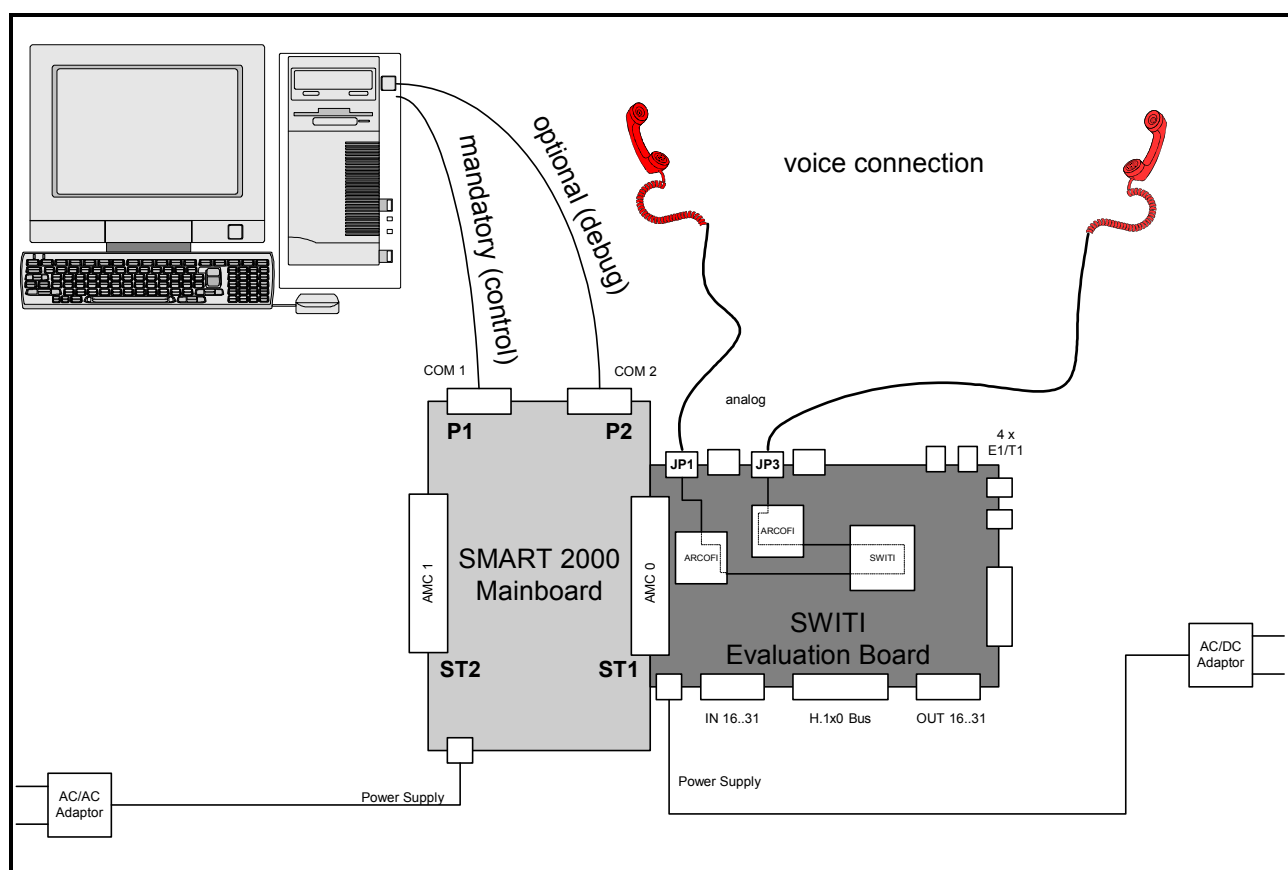


Figure 11 Setup of Switi Evaluation Board and SMART 2000 Mainboard

## **5.2 DAvE Configurator**

The DAvE Configurator for SWITl has been designed to assist engineers in software development for our SWITl device family. The DAVE Configurator is a software tool for generating executable software moduls very fast. The devices can be configured in a very easy way by clicking in a graphical user interface (GUI). DAvE generates C-code skeleton, which can be included in the customers host software.

For further informations please refer to the “DAvE Configurator for SWITl” CD-ROM. On the CD you will also find a readme.txt document with further informations about DAvE.



## Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.

Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

<http://www.infineon.com>