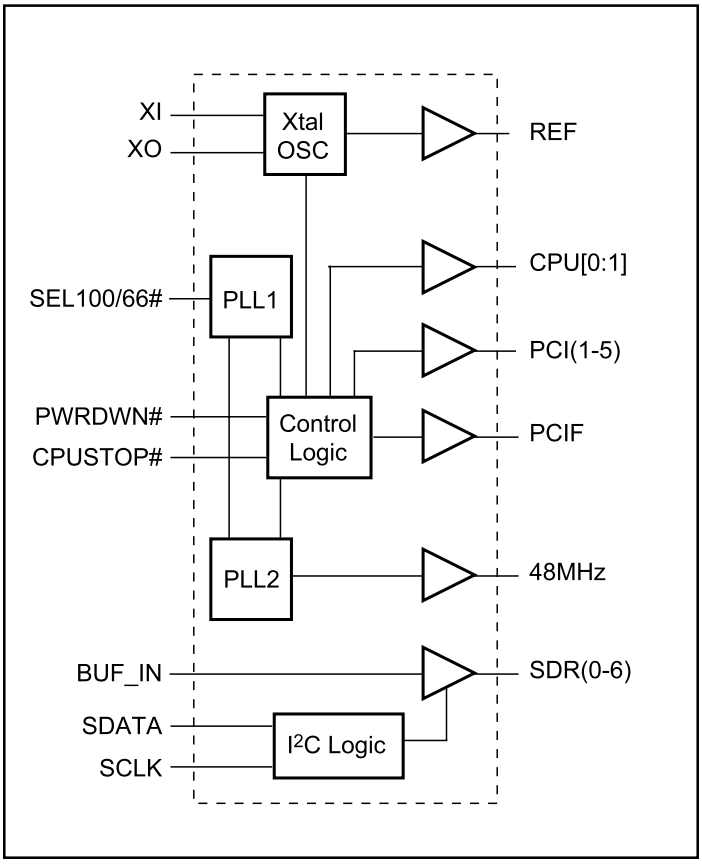
Integrated Clock Generator for Mobile PC's

Features

- Integrated clock generator and SDRAM clock drivers for mobile PC's
- Two 2.5V CPU clock outputs, with enhanced drive
- Spread Spectrum is enabled at power up for EMI suppression
- 66.6 and 100 MHz CPU frequency
  - Separate 100/66 MHz select pin
- Seven integrated SDRAM drivers with low skew of <250ps
- Six 33.3 MHz PCI clocks
- Power management controls
- 48 MHz clock
- Reference clock output
- I^2C control for SDRAM clock outputs, for power saving
- Low power consumption
- 48-pin 240-mil TSSOP package(A)

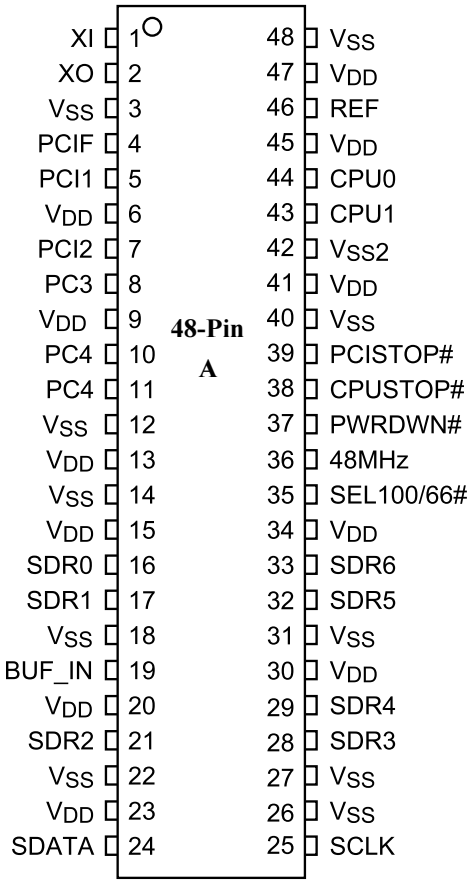
Block Diagram



Description

PI6C674 is an integrated clock generator and SDRAM drivers for 66.6 and 100 MHz SDRAM-based mobile systems. Power management controls are realized with standard control signals such as PWRDWN#, CPUSTOP#, PCISTOP#, and I^2C enable/disable control for individual SDRAM outputs. Generous power supply pins ensure low noise and high performance.

Pin Configuration



Select Functions

SEL100/66#	CPUCLK,SDRAM (MHz)	PCICLK(MHz)
Low	66.6	33.3
High	100	33.3

Purchase of I^2C components from Pericom conveys a license to use them in an I^2C system as defined by Philips.

Select Functions

Pin	Signal Name	I/O	Qty.	Description
1	XI	I	1	14.318 MHz xtal in.
2	XO	O	1	14.318 MHz xtal out.
4	PCIF	O	1	Free running 33.3 MHz PCI clock output, not controlled by PCISTOP#. Spread spectrum enabled.
5,7,8,10,11	PCI[1-5]	O	5	33.3MHz PCI clock outputs, controlled by PCISTOP#. Spread spectrum enabled.
16,17,21,28, 29,32,33	SDR[0-6]	O	7	SDRAM clock outputs, controlled by I^2C registers.
19	BUF_IN	I	1	Input clock to SDR[0-6] buffer, normally driven by the chipset.
24	SDATA	I/O	1	Serial Data for I^2C, internally pulled up.
25	SCLK	I	1	Serial Clock for I^2C, internally pulled up.
35	SEL100/66#	I	1	Selects CPU[0-1] frequency. "H"=100 MHz, "L"=66.6 MHz.
36	48MHz	O	1	48MHz output, no spread spectrum.
37	PWRDWN#	I	1	Active low: PLLs are off, all outputs, except SDR[0-6] and SDATA, are inactive low.
38	CPUSTOP#	I	1	CPUSTOP#=0 : CPU[0 - 1] are inactive low. With internal pull up.
39	PCISTOP#	I	1	PCISTOP#=0 : PCI[1 - 5] are inactive low. With internal pull up.
43,44	CPU[1 - 0]	O	2	CPU clock outputs, controlled by CPUSTOP#. Spread spectrum enabled.
46	REF	O	1	Reference clock output, 14.318MHz. No spread spectrum.
3,12,14, 18,22,26,27, 31,40,48	V_{SS}	—	10	Ground for 3.3V power supplies
6,9,13, 15,20,23,30, 34,41,47	V_{DD}	—	10	3.3V power supplies.
42	V_{SS2}	—	1	2.5V ground for CPU[0 - 1] power supply.
45	V_{DD2}	—	1	2.5V power supply for CPU[0 - 1].

Power Management: Clock Enable Configuration

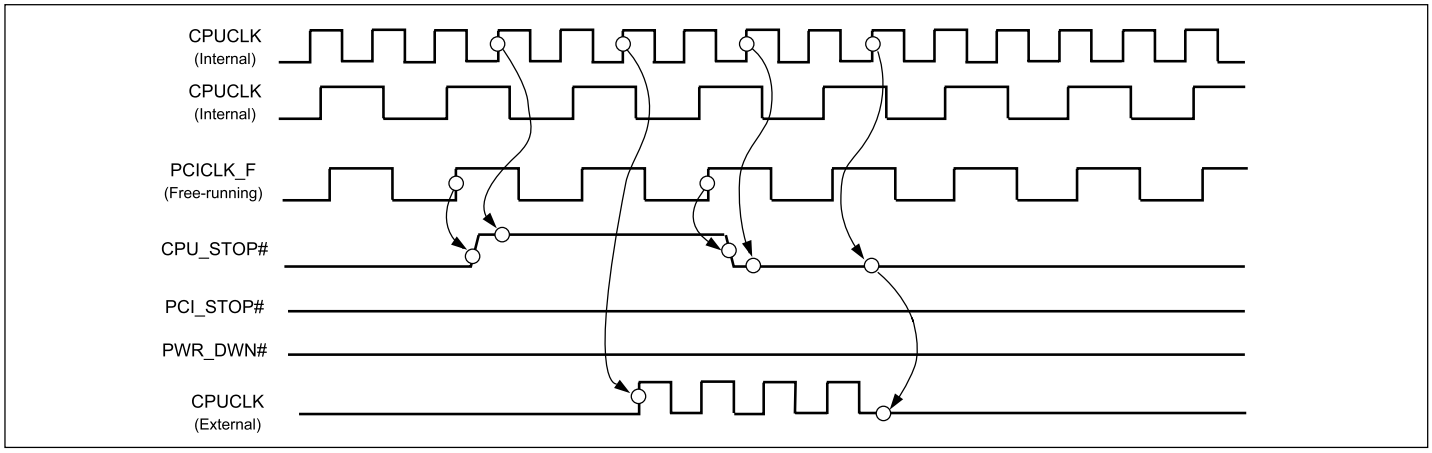
CPU_STOP#	PCI_STOP#	PWR_DWN#	CPU[0-1]	PCI[1-5]	PCIF	REF	48MHz	Crystal	VCO's
X	X	0	Low	Low	Low	Stopped	Off	Off	Off
0	0	1			33.3MHz	Running	Running	Running	Running
0	1	1		33.3MHz					
1	0	1	100/66.6MHz	Low					
1	1	1		33.3MHz					

Power Management Timing

Signal	Signal State	Latency: No. of rising edges of free running PCICLK
CPU_STOP#	1 (enabled)(1)	1
	0 (disabled)(2)	1
PCI_STOP#	1 (enabled)(1)	1
	0 (disabled)(2)	1
PWR_DWN#	1 (normal operation)(3)	3ms
	0 (power down for CPUCLK, SDRAM, PCICLK)	2 max

Notes:
1. Clock on latency is defined from when the clock enable goes high to the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes low to the last clock is driven low out of the device.
3. Power up latency is when PWR_DWN# goes inactive (high) to when the first valid clocks are driven from the device.

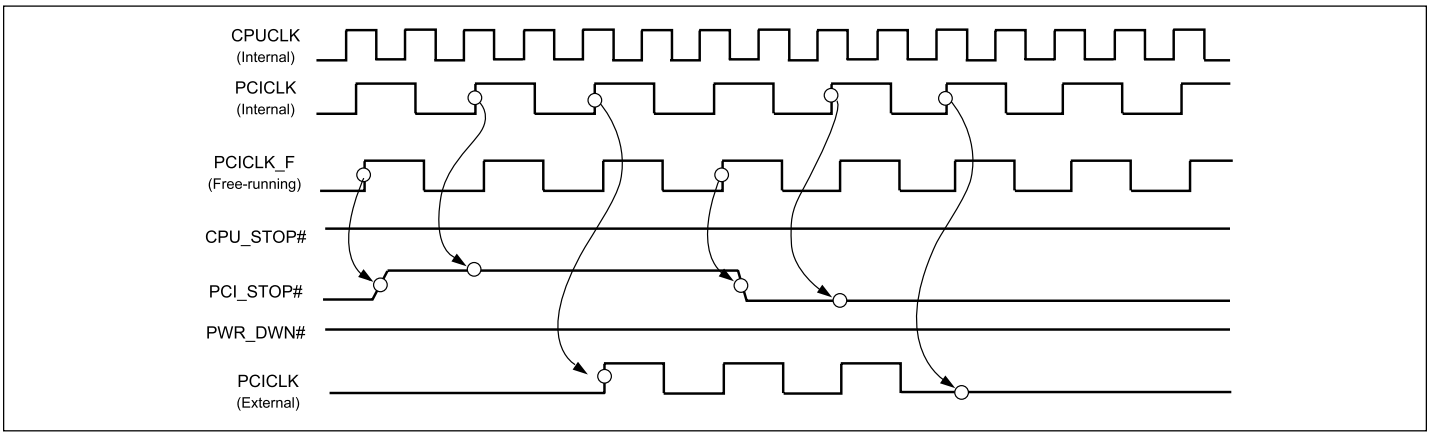
CPU_STOP#, which is an input signal used to turn off the CPU clocks for low power operation, is asserted asynchronously by the external clock control logic with the rising edge of the free running PCI clock and is internally synchronized to the external PCICLK_F output. All other clocks continue to run while the CPU clocks are disabled. The CPU clocks are always stopped in a LOW state and started guaranteeing that the high pulse width is a full pulse. The CPU clock on latency is 2 or 3 CPU clocks and the CPU clock off latency is 2 or 3 CPU clocks.



CPU_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only.
3 CPU_STOP# is an input signal that must be made synchronous to the free running PCI_F.
4. ON/OFF latency shown in the diagram is 2 CPU clocks.
5. All other clocks continue to run undisturbed.
6. PWR_DWN# and PCI_STOP# are shown in a HIGH state.
7. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

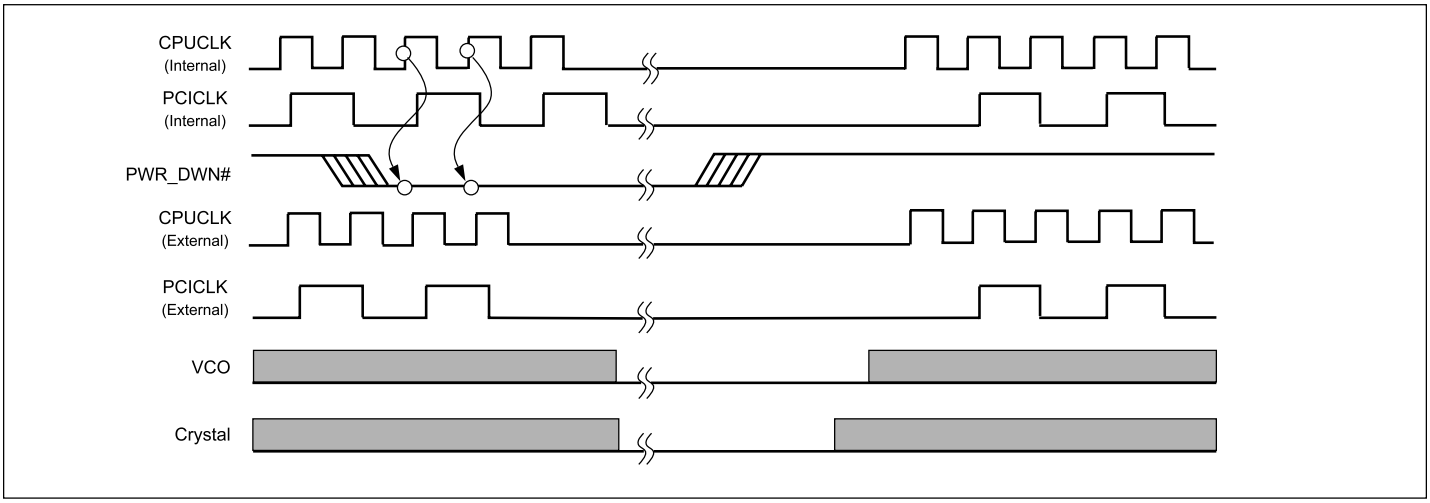
PCI_STOP# is an input signal used to turn off PCI clocks for low power operation. PCI clocks are stopped in the LOW state and started with a guaranteed full high pulse width. There is ONLY one rising edge of external PCICLK after the clock control logic.



PCI_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCI_F output.
3 Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 66MHz. Similar operation as CPU = 100 MHz.

The PWR_DWN# is used to place the device in a very low power state. PWR_DWN# is an asynchronous active low input. Internal clocks are stopped after the device is put in power-down mode. The power-on latency is less than 3ms. PCI_STOP# and CPUSTOP# are "don't cares" during the power-down operations. The REF clock is topped in the LOW state as soon as possible.



PWR_DWN# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only.
3. PWR_DWN# is an asynchronous input and metastable conditions could exist. The signal is synchronized inside the part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown wth respect to 66 MHz. Similar operation as CPU = 100 MHz.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
2.5V Supply Voltage to Ground Potential	–0.5V to +3.6V
DC Input Voltage	–0.5V to +4.6V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (V_{DD} = +3.3V ± 5%, V_{DD2} = +2.5V ± 5%, T_A = 0°C to +70°C)

PI6C102-16 Condition	Max. 2.5V Supply Consumption Max. discrete cap loads, V_{DDQ2} = 2.625V All static inputs = V_{DDQ3} or V_{SS}	Max. 3.3V Supply Consumption Max. discrete cap loads, V_{DDQ3} = 3.465V All static inputs = V_{DDQ3} or V_{SS}
Powerdown Mode (PWRDWN# =0)	100µA	500µA
Active 66 MHz SEL 100/66# = 0	TBD	TBD
Active 100 MHz SEL 100/66# = 1	TBD	TBD

DC Operating Specifications

Symbol	Parameters	Conditions	Min.	Max.	Units
V_{DD} = 3.3V ± 5%					
V_{IH}	Input high voltage	V_{DD}	2.0	V_{DD} +0.3	V
V_{IL}	Input low voltage		V_{SS} -0.3	0.8	
I_{IL}	Input leakage current	0 < V_{IN} < V_{DD}	-5	+5	µA
V_{DD} = 2.5V ± 5%					
V_{OH2}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL2}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{OH}	Output high voltage	I_{OH} = -1mA	2.4		V
V_{OL}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{POH}	PCI Bus output high voltage	I_{OH} = -1mA	2.4		V
V_{POL}	PCI Bus output low voltage	I_{OL} = 1mA		0.55	
C_{IN}	Input pin capacitance			5	pF
C_{XTAL}	Xtal pins capacitance	13.5	18.0	22.5	
C_{OUT}	Output pin capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No airflow	0	70	°C

Buffer Specifications

Buffer Name	V_{DD} Range(V)	Impedance (Ω)	Buffer Type
CPU	2.375 -2.625	13.5 - 45	Type 1
REF, 48 MHz	3.135 - 3.465	20 - 60	Type 3
PCI	3.135 - 3.465	12 - 55	Type 5

Type 1: CPU Clock Buffers (2.5V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	54			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			54	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	54			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			54	
t_{RH}	2.5V Type 1 output rise edge rate	2.5V ± 5% @ 0.4V-2.0V	1		4	V/ns
t_{FH}	2.5V Type 1 output fall edge rate	2.5V ± 5% @ 2.0V-0.4V	1		4	

Type 3: REF, 48MHz Buffers (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-29			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-23	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	29			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			27	
t_{RH}	3.3V Type 3 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	0.5		2	V/ns
t_{FH}	3.3V Type 3 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	0.5		2	

Type 5: PCI Clock Buffers (3.3V)

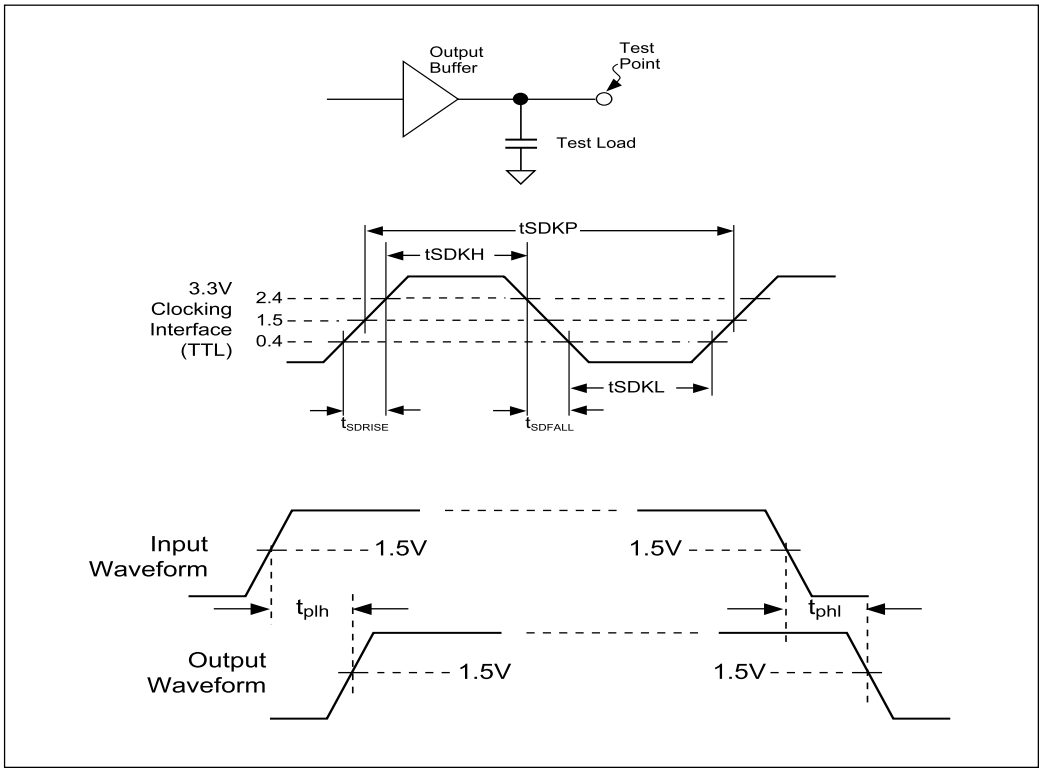
Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-33			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-33	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.95V	30			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	
t_{RH}	3.3V Type 5 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	1		4	V/ns
t_{FH}	3.3V Type 5 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	1		4	

AC Timing

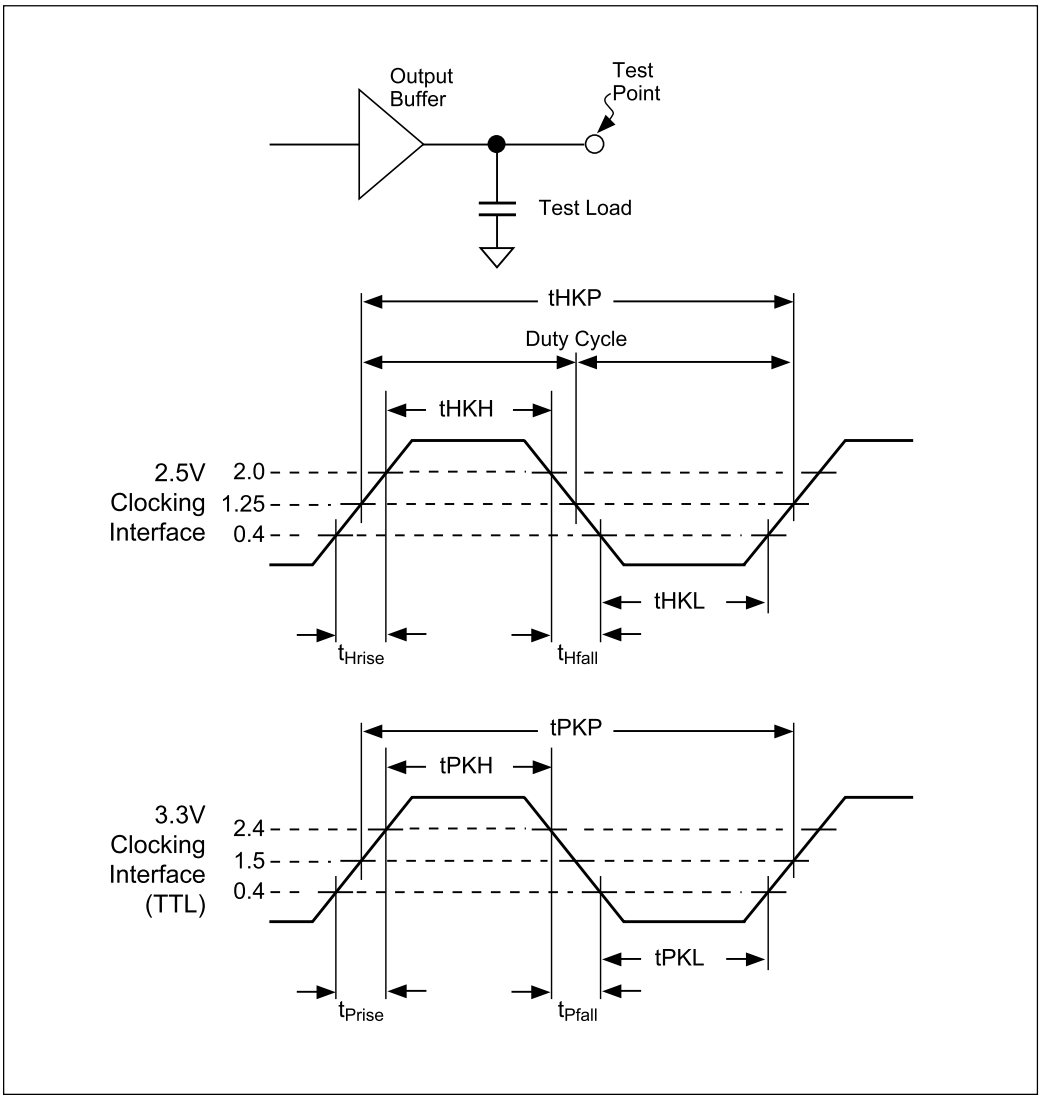
Symbol	Parameters	66 MHz		100 MHz		Units
		Min.	Max.	Min.	Max.	
t_{HKP} (2.5V)	Host CLK period	15.0	15.5	10.0	10.5	ns
t_{HKH} (2.5V)	Host CLK high time	5.2		3.0		
t_{HKL} (2.5V)	Host CLK low time	5.0		2.8		
t_{HRISE} (2.5V)	Host CLK rise time	0.4	1.6	0.4	1.6	
t_{HFALL} (2.5V)	Host CLK fall time	0.4	1.6	0.4	1.6	
t_{JITTER} (2.5V)	Host CLK Jitter		250		250	ps
Duty Cycle (2.5V)	Measured at 1.25V	45	55	45	55	%
t_{HSKW} (2.5V)	Host Bus CLK Skew		175		175	ps
t_{PZL}, t_{PZH}	Output enable delay	1.0	8.0	1.0	8.0	ns
t_{PLZ}, t_{PHZ}	Output disable delay	1.0	8.0	1.0	8.0	
t_{HSTB}	Host CLK Stabilization from power-up		3		3	ms
t_{PKP}	PCI CLK period	30.0	∝	30.0	∝	ns
t_{PKPS}	PCI CLK period stability		500		500	ps
t_{PKH}	PCI CLK high time	12.0		12.0		ns
t_{PKL}	PCI CLK low time	12.0		12.0		
t_{PSKW}	PCI Bus CLK Skew		500		500	ps
$t_{HPOFFSET}$	Host to PCI Clock Offset	1.5	4.0	1.5	4.0	ns
t_{PSTB}	PCI CLK Stabilization from power-up		3		3	ms
t_{SDKP}	SDRAM CLK period	15.0	15.5	10.0	10.5	ns
t_{SDKH}	SDRAM CLK high time	5.6		3.3		
t_{SDKL}	SDRAM CLK low time	5.3		3.1		
t_{SDRISE}	SDRAM CLK rise time	1.5	4.0	1.5	4.0	V/ns
t_{SDFALL}	SDRAM CLKfall time	1.5	4.0	1.5	4.0	
t_{PLH}	SDRAM Buffer LH prop delay	1.0	5.0	1.0	5.0	ns
t_{PHL}	SDRAM BufferHL prop delay	1.0	5.0	1.0	5.0	
t_{PZL},t_{PZH}	SDRAM Buffer Enable delay	1.0	8.0	1.0	8.0	
t_{PLZ},t_{PHZ}	SDRAM Buffer Disable delay	1.0	8.0	1.0	8.0	
Duty Cycle	Measured at 1.5V	45	55	45	55	%
t_{SDSKW}	SDRAM Output-to-Output Skew		250		250	ps

Type 4 SDRAM Clock Buffer (3.3V)

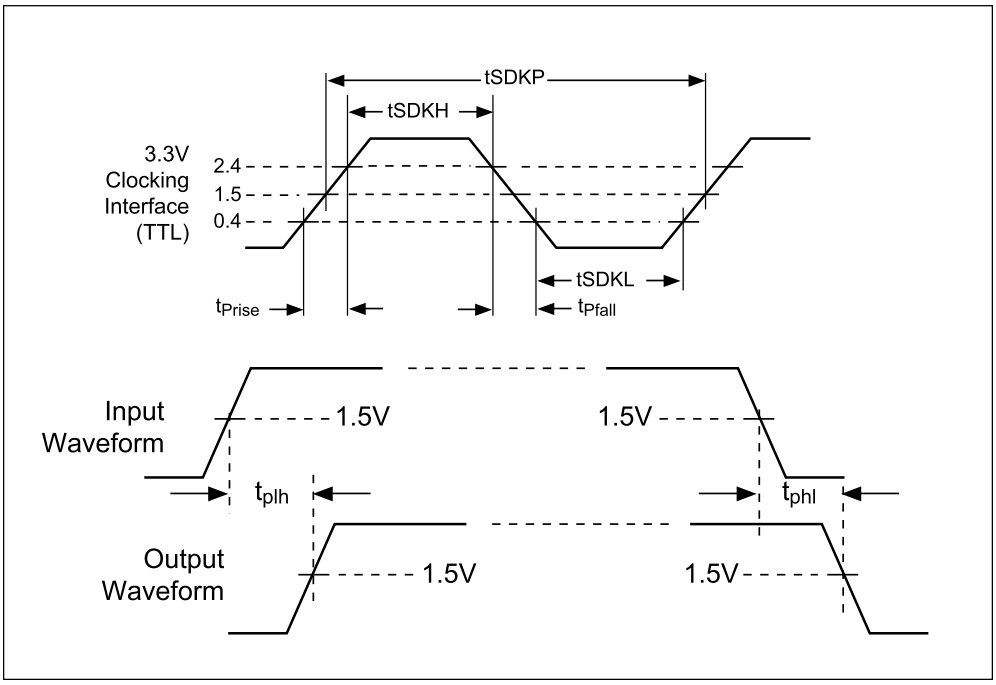
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 2.0V	-54			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-46	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.0V	54			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			53	
t_{rh}SDRAM	Output rise edge rate SDRAM only	3.3V ±5% @04V-2.4V	1.5		4	V/ns
t_{th}SDRAM	Output fall edge rate SDRAM only	3.3V ±5% @2.4V-0.4V	1.5		4	



Host Clock and PCI CLK Timing



Clock Output Waveforms



Minimum and Maximum Expected Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads
PCI Clocks (PCLK)	30	30		Meets PCI 2.1 requirements
REF, 48MHz	10	20		1 device load
SDRAM	20	30		SDRAM DIMM Specification

Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load.
2. Minimum rise/fall times are guaranteed at minimum specified load.
3. Rise/fall times are specified with pure capacitive load as shown.
   Testing is done with an additional 500Ω resistor in parallel.

I²C Serial Interface

Address Assignment

A6	A5	A4	A3	A2	Al	A0	R/W
1	1	0	1	0	0	1	-----

Data Protocol

1 bit	7 bits	1	1	8 bits	1	
Start Bit	Slave Address	R/W	Ack	Command Code	Ack	Byte Count =N

→

1 bit	8 bits	1	8 bits	1		8 bits	1	1
ACK	Data Byte 1	ACK	Data Byte 2	ACK	—	Data Byte N	ACK	STOP

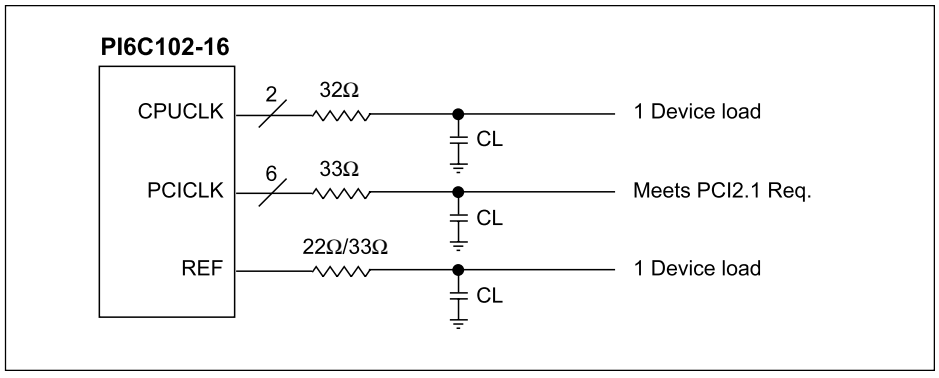
Byte 0: SDRAM Active/Inactive Register

(1 = Enabled, 0 = Disabled, Output Held Low)

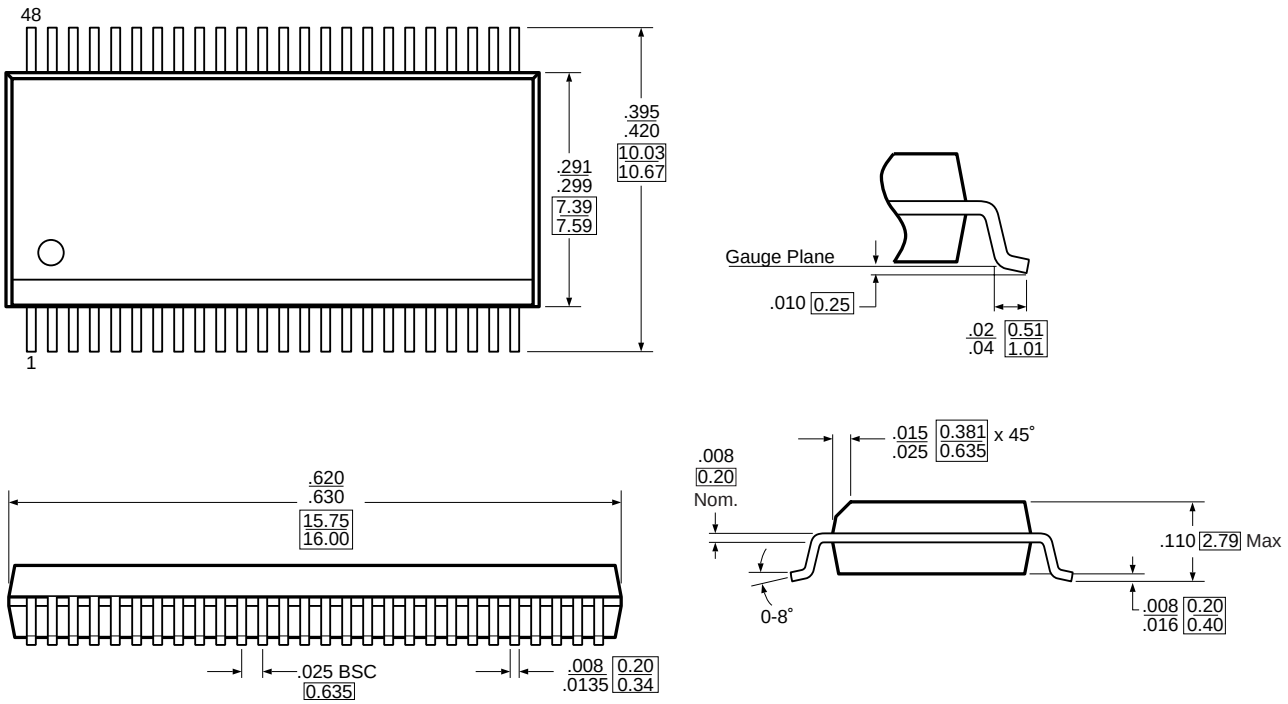
Bit	PI6C674 Pin #	Power-Up Default	Description
Bit 7	29	1	SDR4 (Active/Inactive)
Bit 6	28	1	SDR3 (Active/Inactive)
Bit 5		0	NC
Bit 4	21	1	SDR2 (Active/Inactive)
Bit 3		0	NC
Bit 2		0	NC
Bit 1	17	1	SDR1 (Active/Inactive)
Bit 0	16	1	SDR0 (Active/Inactive)

Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.



48-Pin SSOP Package Data



Package Mechanical Information

Plastic 48-pin 240-mil Thin Shrink Small-Outline Package (TSSOP, Pericom A48)

Ordering Information

P/N	Description
PI6C674A	48-pin TSSOP Package