Low-Noise Phase-Locked Loop Clock Driver with 9 Clock Outputs

Product Features

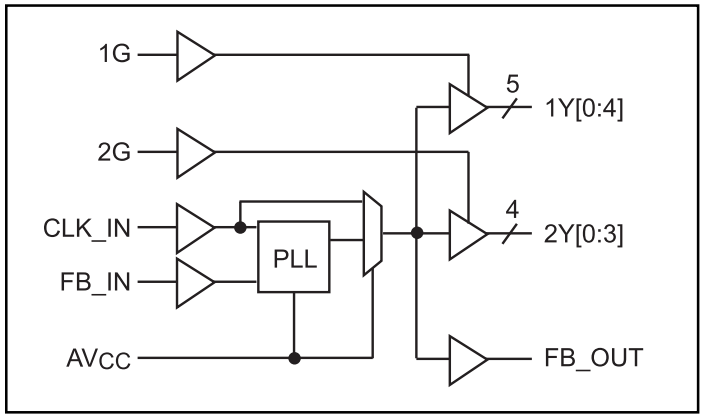
- Operating Frequency up to 125 MHz
- Low-Noise Phase-Locked Loop Clock Distribution to meet Registered DIMM Synchronous DRAM module specifications for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-output delay: Distribute One Clock Input to one bank of five and one bank of four outputs, with separate output enables
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Packaged in Plastic 24-pin Thin Shrink Small-Outline Package (L)

Product Description

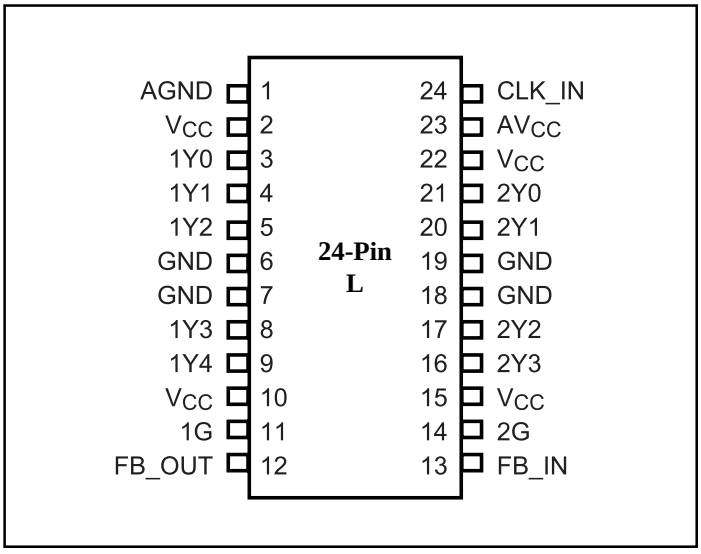
The PI6C2509C is a "quiet," low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing low-noise clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK_IN input clock to be distributed, providing 5 clocks for the first bank, and an additional 4 clocks for the second bank.

For testing, the PLL can be bypassed by strapping AV_{CC} to ground. The PI6C2509C has the same pinout as TI's CDC2509x, with enhanced rise/fall times, allowing a Spread Spectrum clock input with a 30-ohm on-chip series damping resistor. PI6C2509C1 is similar to PI6C2509C, except that it has a zero-Ohm damping resistor.

Logic Block Diagram



Product Pin Configuration



Functional Table

Input Control	Outputs	
1G,2G	**1Y[0:4] ,2Y[0:3]**	**FB_OUT**
L	L	CLK_IN
H	CLK_IN	CLK_IN

Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	24	I	Clock input. CLK_IN allows spread spectrum.
FB_IN	13	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
1G	11	I	Output bank enable. When 1G is LOW, outputs 1Y[0:4] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:4] are enabled.
2G	14	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled.
FB_OUT	12	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Yx, 2Yx.
1Y[0:4]	3,4,5,8,9	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
2Y[3:0]	16,17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} can be also used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK_IN. is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2,10,15,22	Power	Power supply.
GND	6,7,18,19	Ground	Ground.

DC Specifications

Absolute maximum ratings over operating free-air temperature range.

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CC}, AV_{CC}	Supply voltage			4.6	V
V_I	Input voltage	$I_{IK} < I_{IK\_MAX}$	–0.5	6.5	
V_{OX}	Voltage applied to any output	V_O = low/high, $I_{OK} < I_{OK\_MAX}$		4.6	
I_{IK_MAX}	Output clamp current	$V_I < 0$			mA
I_{OK_MAX}	Input clamp current	$V_O < 0$, or $V_O > V_{CC}$	–50	50	
I_{OC}	Continuous output current	V_O = 0 to V_{CC}		50	
I_{XX}	Continuous current though V_{CC}/GND		–100	100	
P_D	Power dissipation	T_A = 55°C, still air		0.7	W
T_{STG}	Storage temperature range		–65	150	°C

Note:
Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}, AV_{CC}	Supply voltage	3.0	3.6	V
V_{IH}	Low input voltage	2.0		
V_{IL}	High input voltage		0.8	
V_I	Input voltage	0.0	V_{CC}	
I_{OH}	High output current	–12		mA
I_{OL}	Low output current		12	
T_A	Operating free air temperature	0	85	°C

Note:
1. All unused inputs must be held high or low.

Electrical characteristics over recommended operating conditions

Symbol	Parameter	Test Conditions	V_{CC}, AV_{CC}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	I_I = –18mA	3V			–1.2	V
V_{OH}	High Output Voltage	I_{OH} = –100uA	Min. – Max.	V_{CC}–0.2			
		I_{OH} = –12mA	3V	2.1			
		I_{OH} = –6mA	3V	2.4			
V_{OL}	Low Output Voltage	I_{OL} = 100uA	Min. – Max.			0.2	
		I_{OL} = 12mA	3V			0.8	
		I_O = 6mA	3V			0.55	
I_{OH}	High Output Current	V_O = 1.0V	3.135V	–32			mA
		V_O = 1.65V	3.3V		–36		
		V_O = 3.135V	3.465V			–12	
I_{OL}	Low Output Current	V_O = 1.95V	3.135V	34			
		V_O = 1.65V	3.3V		40		
		V_O = 0.4V	3.465V			14	
I_I	Input Current	V_I = V_{CC}/GND	3.6V	–5		5	µA
I_{CC}	Supply Current	V_I = V_{CC}/GND, I_O = 0, V_O = low/high	3.6V			10	
C_I	Input Capacitance	V_I = V_{CC}/GND	3.3V		4		pF
C_O	Output Capacitance	V_O = V_{CC}/GND	3.3V		6		

AC Specifications

Timing requirements over recommended ranges of supply voltage and operating free-air temperature.

Symbol	Parameter	Min.	Max.	Units
F_{CLK}	Clock frequency	25	125	MHz
D_{CYI}	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

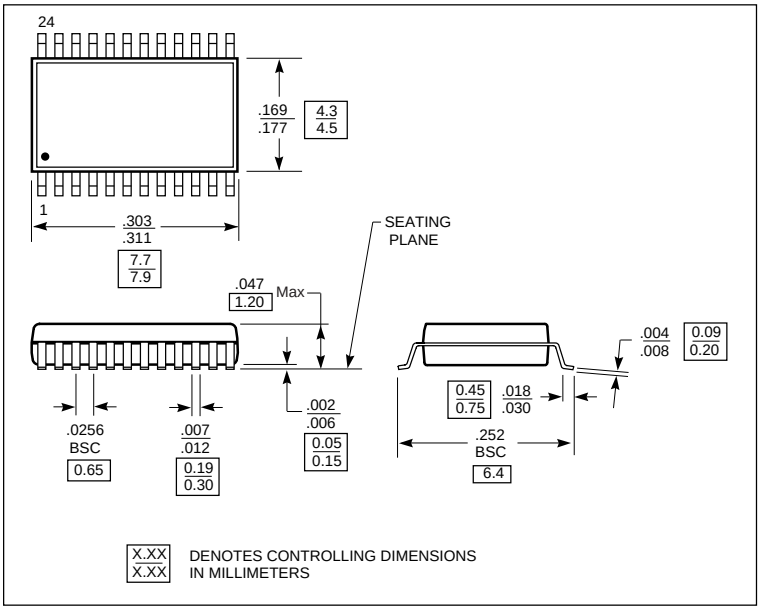
Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L=30pF

Parameter	From	To	V_{CC} = 3.3V ±0.165V			Units
			Min.	Typ.	Max.	
tphase error, with and without Spread Spectrum	CLK_IN↑ at 100 MHz	FB_IN↑	–150		+150	ps
Jitter, cycle-to-cycle with and without Spread Spectrum	Any Output or FB_OUT in CLK_n at 100 MHz	Output or FB_OUT in CLK_{n+1}	–100		100	ps
Skew	Any Y or FB_OUT	Any Y or FB_OUT			200	ps
Duty cycle	CLK_IN >66 MHz	Any Y or FB_OUT	45		55	%
t_r, rise-time	V_O = 1.2 – 1.8V, IBIS Simulation	Any Y or FB_OUT	2.5		1.0	ns
t_f, fall-time	V_O = 1.2 – 1.8V, IBIS Simulation	Any Y or FB_OUT	2.5		1.0	ns

Note: These switching parameters are guaranteed, but not production tested.

Package Mechanical Information

Plastic 24-pin Thin Shrink Small-Outline Package (L package).



Ordering Information

Part Number	Series Damping Resistor	Ordering P/N
PI6C2509C	30 Ohms	PI6C2509CL
PI6C2509C1	Zero Ohms	PI6C2509C1L