

Phase-Lock Loop Clock Driver with 9 Clock Outputs

Product Features

- High performance Phase-Lock Loop Clock Distribution for 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-output delay: Distribute One Clock Input to one bank of five and one bank of four outputs, with separate output enables
- Same pinout as TI CDC2509A/2509B
- Low jitter: Cycle-to-Cycle jitter ± 100 ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Packaged in Plastic 24-pin Thin Shrink Small-Outline Package (L)
- Wide range of Clock Frequencies:

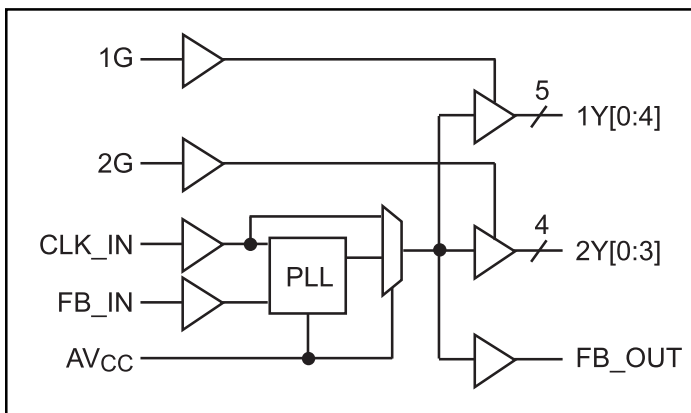
Product Description

The PI6C2509A family features a low-skew, low-jitter, phase-lock loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK_IN input clock to be distributed, providing 5 clocks for the first bank and an additional 4 clocks for the second bank.

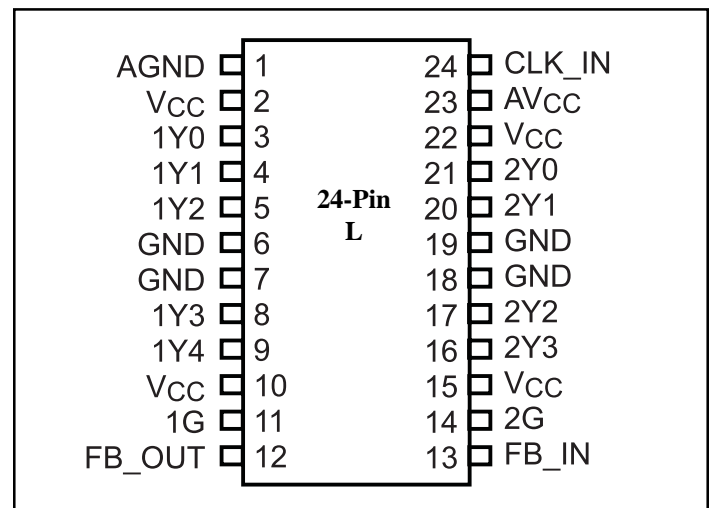
The PI6C2509A part is designed to meet the PC100 SDRAM Registered DIMM specification for heavy load applications. For test purposes, the PLL can be bypassed by strapping AV_{CC} to ground.

The PI6C2509A family has the same pinout as TI CDC2509A/2509B, with enhanced rise/fall times, and allowing a Spread Spectrum clock input.

Logic Block Diagram



Product Pin Configuration



Functional Table

Inputs			Outputs		
1G	2G	CLK_IN	1Y[0:4]	2Y[0:3]	FB_OUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	24	I	Reference Clock input. CLK_IN allows the input clock having spread spectrum of 0.5% modulation.
FB_IN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL.
1G	11	I	Output bank enable. When 1G is LOW, outputs 1Y[0:4] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:4] are enabled.
2G	14	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled.
FB_OUT	12	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Yx, 2Yx.
1Y[0:4]	3,4,5,8,9	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
2Y[3:0]	16,17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AVCC	23	Power	Analog power supply. AVCC can be also used to bypass the PLL for test purpose. When AVCC is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VCC	2,10,15,22	Power	Power supply
GND	6,7,18,19	Ground	Ground

DC Specifications

Absolute maximum ratings over operating free-air temperature range.

Symbol	Parameter	Min.	Max.	Units
V _I	Input voltage range	-0.5	V _{CC} +0.5	V
V _O	Output voltage range			
V _{I_DC}	DC input voltage		+5.0	
I _{O_DC}	DC output current		100	mA
Power	Maximum power dissipation at T _A = 55°C in still air		1.0	W
T _{STG}	Storage temperature	-65	150	°C

Note: Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	V _{CC}	Min.	Typ.	Max.	Units
I _{CC}	V _I = V _{CC} or GND; I _O = 0	3.6V				mA
C _I	V _I = V _{CC} or GND	3.3V		4		pF
C _O	V _O = V _{CC} or GND			6		

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply voltage	3	3.6	V
V _{IH}	High level input voltage	2		
V _{IL}	Low level input voltage		0.8	
V _I	Input voltage	0	V _{CC}	
T _A	Operating free-air temperature	0	70	°C

Electrical characteristics over recommended operating free-air temperature range:

Pull Up/Down Currents of PI6C2509A/PI6C2509A-134, V_{CC} = 3.0V

Symbol	Parameter	Condition	Min.	Max.	Units
I _{OH}	Pull-up current	V _{OUT} = 2.4V		-19	mA
	Pull-up current	V _{OUT} = 2.0V		-32	
I _{OL}	Pull-down current	V _{OUT} = 0.8V	28		
	Pull-down current	V _{OUT} = 0.55V	19		

AC Specifications

Timing requirements over recommended ranges of supply voltage and operating free-air temperature.

Symbol	Parameter	Min.	Max.	Units
Fclock	Clock frequency PI6C2509A	25	125	MHz
Fclock	Clock frequency PI6C2509A-134	25	134	
DCVI	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

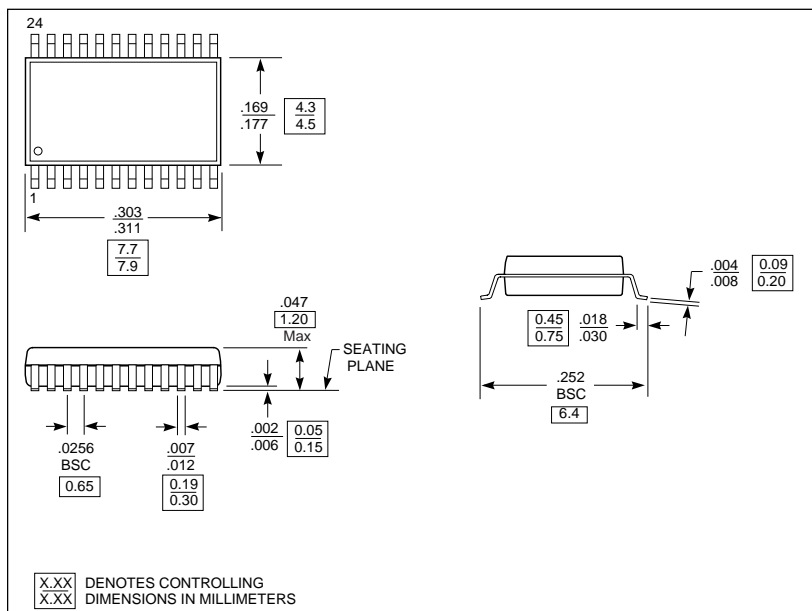
Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L=30\text{pF}$

Parameter	From (Input)	To (Output)	$V_{CC}=3.3\text{V} \pm 0.30\text{V}, 0-70^\circ\text{C}$			Units
			Min.	Typ.	Max.	
tphase error, with and without 0.5% spread spectrum	CLK_IN \uparrow at 100 MHz and 66 MHz	FB_IN \uparrow	-150		+150	ps
Jitter, cycle-to-cycle, with and without 0.5% spread spectrum	Any Output or FB_OUT in CLK n, at 100 MHz and 66 MHz	Output or FB_OUT in CLK n+1	-100		+100	
Skew, at 100 MHz and 66 MHz	Any Y or FB_OUT	Any Y or FB_OUT			200	
Duty cycle			45		55	%
t _R , rise-time, 0.4V to 2.0V				1.0		ns
t _F , fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed, but not production tested.

Package Mechanical Information

Plastic 24-pin Thin Shrink Small-Outline Package (L package).



Ordering Information

Part Number	Operating Freq.Range	Ordering P/N
PI6C2509A	25 MHz-125MHz	PI6C2509AL

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