Precision Clock Synthesizer for Mobile PCs

Features

- Two copies of CPU clock with V_{DD} of 2.5V ±5%
- 100 MHz or 66 MHz operation
- Six copies PCI clock (synchronous with CPU clock) 3.3V
- One copy of Ref. clock @ 14.31818 MHz (3.3V_{TTL})
- 48 MHz USB Clock, 24 MHz Super I/O clock
- I^2C Serial Configuration Interface
- Spread Spectrum Modulation for CPUCLK, and PCICLK
- Low-cost 14.31818 MHz crystal oscillator input
- Power management control
- Isolated core V_{DD}, V_{SS} pins for noise reduction
- 28-pin SSOP and SOIC package (H)

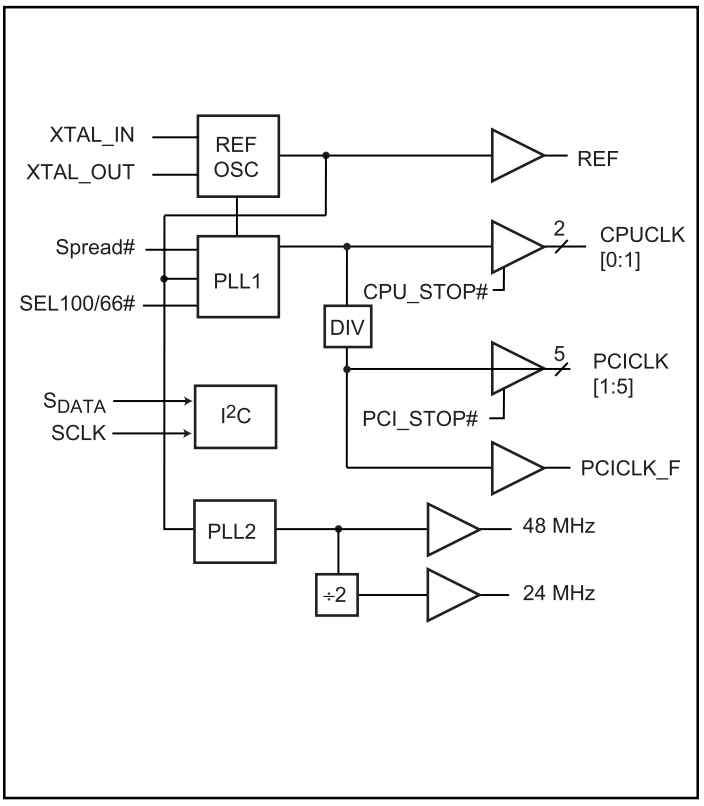
Description

The PI6C105 is a high-speed, low-noise clock generator designed to work with the PI6C18x family of clock buffers to meet all clock needs for Mobile Intel Architecture platforms. CPU and chipset clock frequencies of 66.6 MHz and 100 MHz are supported.

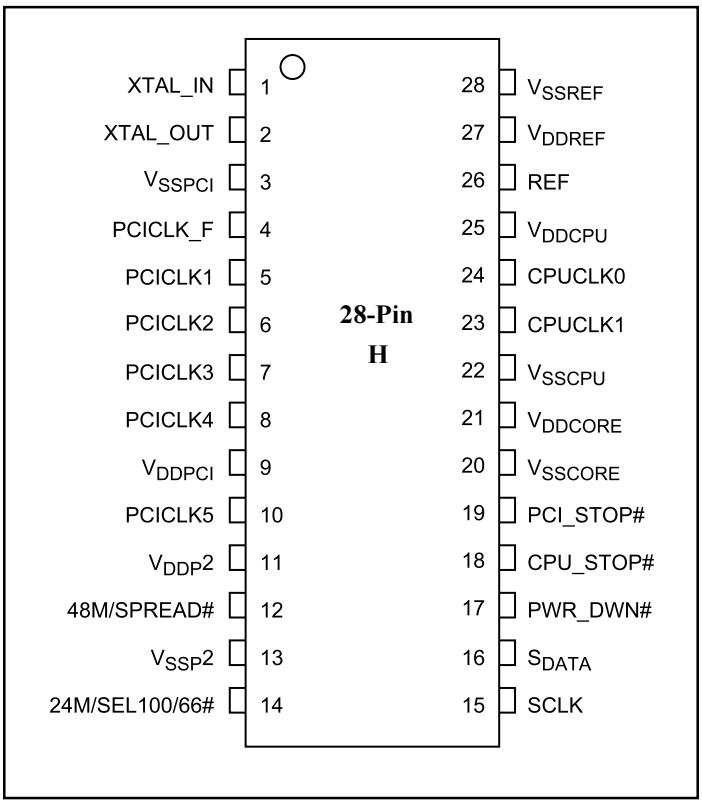
Split supplies of 3.3V and 2.5V are used. The 3.3V power supply powers a portion of the I/O and the core. The 2.5V is used to power the remaining outputs. 2.5V signaling follows JEDEC standard 8-X. Power sequencing of the 3.3V and 2.5V supplies is not required.

An asynchronous PWR_DWN# signal may be used to power down (or up) the system in an orderly manner.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal Name	Qty.	Description
1	XTAL_IN	1	14.318 MHz crystal input
2	XTAL_OUT	1	14.318 MHz crystal input
3	V_{SSPCI}	1	Ground for PCI clock outputs
4	PCICLK_F	1	Free running PCI clock output
5,6,7,8,10	PCICLK[1:5]	5	PCI clock outputs, TTL compatible 3.3V
9	V_{DDPCI}	1	Power for all PCI clock outputs (4,5,6,7,8,10)
11	V_{DDP2}	1	Power Supply for 24 MHz and 48 MHz outputs
12	48 MHz/SPREAD#	1	48 MHz output or SPREAD# input. Internal pull up
	48 MHz		48 MHz output for USB clock
	SPREAD#		Active lowEnable Spread Spectrum mode, default disable. This is an input sampled during power up. Becomes 48 MHz output after power up
13	V_{SSP2}	1	Ground for 24 MHz and 48 MHz
14	24 MHz/SEL100/66#	1	24 MHz output or SEL100/66# input, internal pull up
	24 MHz		24 MHz output for Super I/O Clock
	SEL100/66#		During power up this pin is SEL100/66# input, 24MHz output otherwise. Low = 66MHz, High = 100MHz
15	SCLK	1	Serial Clock for I^2C interface. Internal Pull Up
16	SDATA	1	Serial Data for I^2C interface. Internal Pull Up
17	PWR_DWN#	1	Active Lower Power Down, When active PLLs, crystal, and oscillator is off. CPUCLKs and PCICLK clocks are held low. Internal Pull Up
18	CPU_STOP#	1	Active Low. Stops all CPU clocks to low state. Internal Pull Up
19	PCI_STOP#	1	Active Low. Stops all PCICLK clocks to low state, except for PCICLK_F. Internal Pull Up
20	V_{SSCORE}	1	Ground for chip core
21	V_{DDCORE}	1	Power supply for chip core
22	V_{SSCPU}	1	Ground for CPU clock outputs
23,24	CPUCLK[0:1]	2	CPU and Host clock outputs 2.5V
25	V_{DDCPU}	1	Power supply for CPU clock outputs 2.5V
26	REF	1	Buffered crystal output
27	V_{DDREF}	1	Power Supply for REF outputs
28	V_{SSREF}	1	Ground for REF outputs

Select Functions

SEL100/66#	Function
0	66 MHz active
1	100 MHz active

Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK [0:1]	PCICLK [1:5]	PCICLK_F	Other Clocks	Crystal	VCO's
X	X	0	low	low	low	stopped	off	off
0	0	1	low	low	33 MHz	running	running	running
0	1	1	low	33 MHz	33 MHz	running	running	running
1	0	1	100/66 MHz	low	33 MHz	running	running	running
1	1	1	100/66 MHz	33 MHz	33 MHz	running	running	running

2-Wire I^2C Control

The I^2C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C105 is a slave receiver device. It can not be read back. Sub addressing is not supported. To change one of the control bytes, all preceding bytes must be sent.

Every byte put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device. During normal data transfers, SDATA changes only when SCLK is LOW. Exceptions: A HIGH-to-LOW transition on SDATA while SCLK is HIGH indicates a "start" condition. A LOW-to-HIGH transition on SDATA, while SCLK is HIGH, is a "stop" condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW= write to addressed device). If the device's own address is detected, PI6C105 generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgment of the address byte (D2), two more bytes must be sent:

1. "Command Code" byte, and

2. "Byte Count" byte.

Although the data bits on these two bytes are "don't care," they must be sent and acknowledged.

PI6C105 I^2C Address Assignment

A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	0	1	0

Byte 3: Modes

Bit#	Pup	Pin#	Name	Description				
7	0		RSVD	Reserved				
6	0		SS1	Spread Spectrum Select bit 1				
5	0		SS0	Spread Spectrum Select bit 0				
				SS1	SS0	66M	100M	
				0	0	-0.6%	-0.6%	Default
				0	1	-1.2%	-1.0%	
				1	0	-1.8%	-1.5%	
				1	1	-2.4%	-2.0%	
4	0		RSVD	Reserved				
3	0		RSVD	Reserved				
2	0		RSVD	Reserved				
1	0		MODE1	Mode bit 1				
0	0		MODE0	Mode bit 0				
				M1	M0			
				0	0	Normal		
				0	1	Test Mode		
				1	0	Reserved		
				1	1	Hi-Z		

Byte 4: Clock Controls (1 = Enabled, 0 = Disabled)

Bit #	Pup	Pin #	Name	Description
7	1	12	48MEN	48 MHz Enable, Default is Enable
6		14	24MEN	24 MHz Enable, Default is Enable
5			RSVD	Reserved
4			RSVD	Reserved
3			RSVD	Reserved
2		23	CPU1EN	CPUCLK1 Enable, Default is Enable
1			RSVD	Reserved
0			RSVD	Reserved

Byte 5: PCI Clock Control (1 = Enabled, 0 = Disabled)

Bit #	Pup	Pin #	Name	Description
7	1	4	PCIFEN	PCI_F Enable, Default is Enable
6				Reserved
5		10	PCI5EN	PCI5 Enable, Default is Enable
4				Reserved
3		8	PCI4EN	PCI4 Enable, Default is Enable
2		7	PCI3EN	PCI3 Enable, Default is Enable
1		6	PCI2EN	PCI2 Enable, Default is Enable
0		5	PCI1EN	PCI1 Enable, Default is Enable

Byte 6: REF Clock Control (1 = Enabled, 0 = Disabled)

Bit#	Pup	Pin#	Name	Description		
7	1		RSVD	Reserved		
6						
5						
4						
3		24	CPU0S1	CPU0 Drive Select Bit 1		
2		24	CPU0S0	CPU0 Drive Select Bit 0		
				CPU0S1	CPU0S0	
				0	0	Disable
				0	1	Low Drive
				1	0	High Drive
				1	1	Medium Drive, Default
1		1	26	REFS1REF Drive Select Bit 1		
0		1	26	REFS0REF Drive Select Bit 0		
				REFS1	REFS0	
				0	0	Disable
				0	1	Low Drive
				1	0	High Drive
				1	1	Medium Drive, Default

Note: Outputs are disabled @ low state

SEL100/66# (pin 14)	SS1 Byte3 [6]	SS0 Byte3 [5]	Down Spread	Description
0	0	0	-0.6%	66.6 MHz, -0.6% down spread
0	0	1	-1.2%	66.6 MHz, -1.2% down spread
0	1	0	-1.8%	66.6 MHz, -1.8% down spread
0	1	1	-2.4%	66.6 MHz, -2.4% down spread
1	0	0	-0.6%	100 MHz, -0.6% down spread
1	0	1	-1.0%	100 MHz, -1.0% down spread
1	1	0	-1.5%	100 MHz, -1.5% down spread
1	1	1	-2.0%	100 MHz, -2.0% down spread

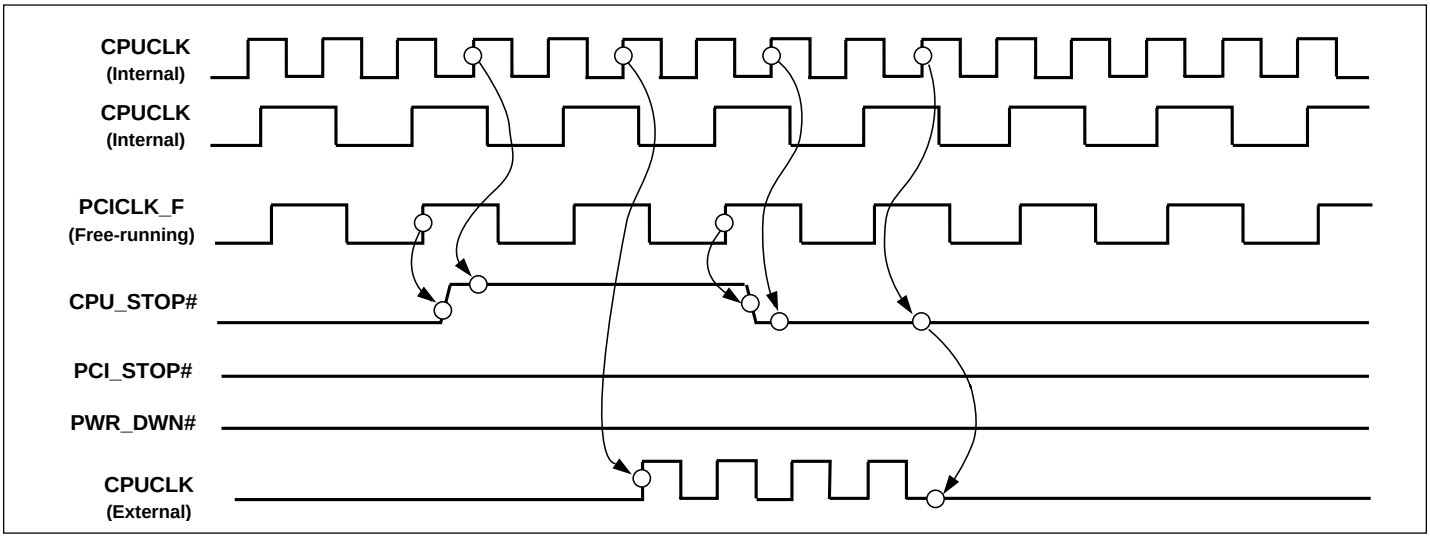
Power Management Timing

Signal	Signal State	Latency
		No. of rising edges of free running PCICLK
CPU_STOP#	0 (disabled)	1
	1 (enabled)	1
PCI_STOP#	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3ms
	0 (power down)	2 max.

Notes:

1. Clock on/off latency is defined as the number of rising edges of free running PCICLKs between when the clock disable goes low/high to when the first valid clock comes out of the device.
2. Power-up latency is from when PWR_DWN# goes inactive (HIGH) to when the first valid clocks are driven from the device.

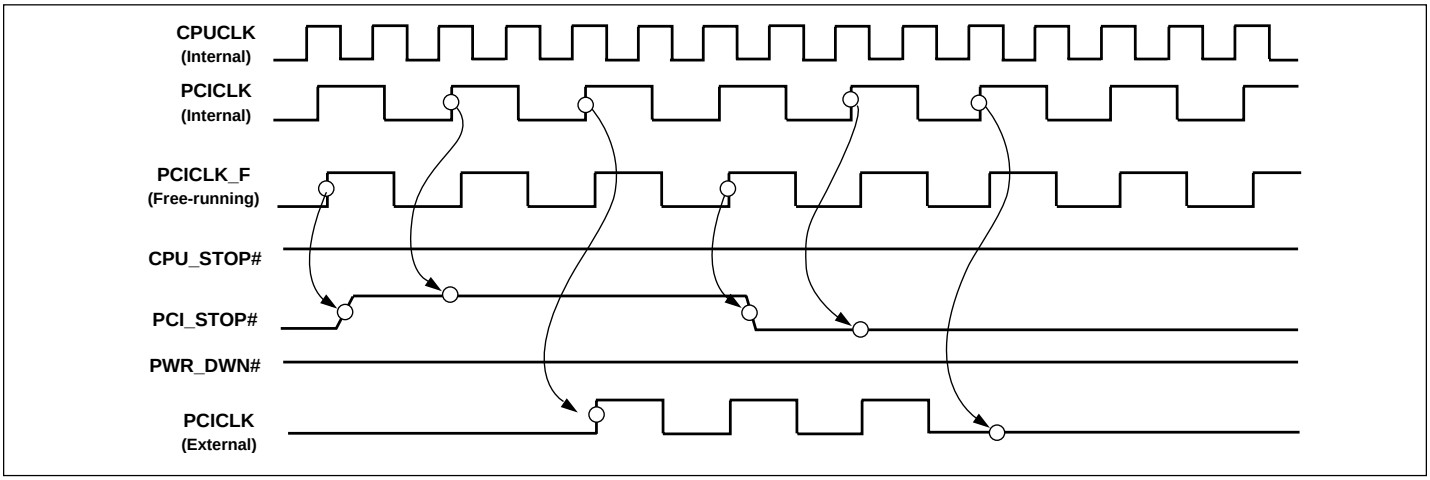
CPU_STOP#, which is an input signal used to turn off the CPU clocks for low power operation, is asserted asynchronously by the external clock control logic with the rising edge of the free running PCI clock and is internally synchronized to the external PCICLK_F output. All other clocks continue to run while the CPU clocks are disabled. The CPU clocks are always stopped in a low state and started guaranteeing that the high pulse width is a full pulse. CPU clock on latency is 2 or 3 CPU clocks while the CPU clock off latency is 2 or 3 CPU clocks.



CPU_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3 CPU_STOP# is an input signal that must be made synchronous to the free running PCI_F.
4. ON/OFF latency shown in the diagram is 2 CPU clocks.
5. All other clocks continue to run undisturbed.
6. PWR_DWN# PCI_STOP# are shown in a high state.
7. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

PCI_STOP# is an input signal used to turn off the PCI clocks for low power operation. PCI clocks are stopped in the low state and started with a guaranteed full high pulse width. There is ONLY one rising edge of external PCICLK after the clock control logic.

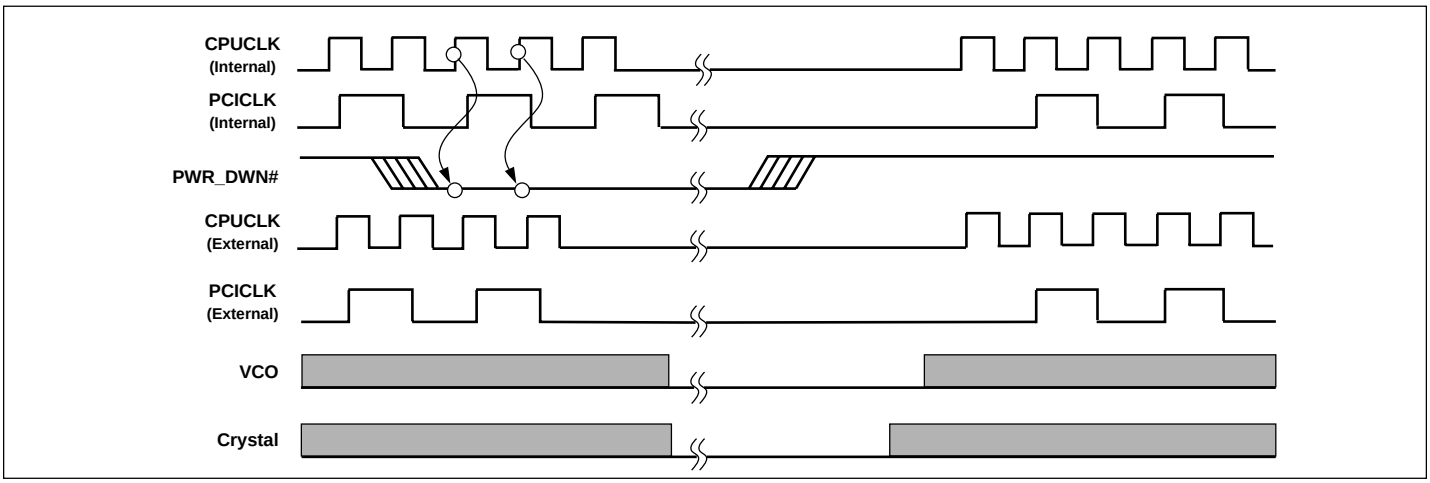


PCI_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCI_F output.
3 Internal means inside the chip.
4. All other clocks continiue to run undisturbed.
5. PWR_DWN# CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

The PWR_DWN#, which is used to place the device in a very low power state, is an asynchronous active low input. Internal clocks are stopped after the device is put in power down mode.

The power on latency is less than 3ms. PCI_STOP# and CPU_STOP# are "don't cares" during the power down operations. The REF clock is stopped in the LOW state as soon as possible.



PWR_DWN# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only.
3. PWR_DWN# is an asynchronous input and metastable conditions could exist. The signal is synchronized inside the part.
4. The Shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown wth respect to 66 MHz. Similar operations as CPU = 100 MHz.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
2.5V Supply Voltage to Ground Potential	–0.5V to +3.6V
DC Input Voltage	–0.5V to +4.6V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C)

PI6C105 Condition	Max. 2.5V Supply Consumption Max. discrete cap loads, V_{DDCPU} = 2.625V All static inputs = V_{DD} or V_{SS}	Max. 3.3V Supply Consumption Max. discrete cap loads, V_{DD} = 3.465V All static inputs = V_{DD} or V_{SS}
Powerdown Mode (PWRDWN# = 0)	100µA	500µA
Active 66 MHz SEL 100/66# = 0	72mA	170mA
Active 100 MHz SEL 100/66# = 1	100mA	170mA

DC Operating Specifications

Symbol	Parameters	Conditions	Min.	Max.	Units
V_{DD} = 3.3V ± 5%					
V_{IH3}	Input high voltage	V_{DD}	2.0	V_{DD} +0.3	V
V_{IL3}	Input low voltage		V_{SS} -0.3	0.8	
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DD}$	-5	+5	
V_{DD2} = 2.5V ± 5%					
V_{OH2}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL2}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{OH3}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL3}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{POH}	PCI Bus output high voltage	I_{OH} = -1mA	2.4		V
V_{POL}	PCI Bus output low voltage	I_{OL} = 1mA		0.55	
C_{IN}	Input pin capacitance			5	pF
C_{XTAL}	Xtal pins capacitance	13.5	18.0	22.5	
C_{OUT}	Output pin capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No airflow	0	70	°C

Buffer Specifications

Buffer Name	V_{DD} Range(V)	Impedance (Ω)	Buffer Type
CPU	2.375 -2.625	13.5 - 45	Type 1
REF, 48/24 MHz	3.135 - 3.465	20 - 60	Type 3
PCI	3.135 - 3.465	12 - 55	Type 5

Type 1: CPU Clock Buffers (2.5V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-27			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-27	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	27			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			30	
t_{RH}	2.5V Type 1 output rise edge rate	2.5V ± 5% @ 0.4V-2.0V	1		4	V/ns
t_{FH}	2.5V Type 1 output fall edge rate	2.5V ± 5% @ 2.0V-0.4V	1		4	

Type 3: REF Buffers (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-29			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-23	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	29			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			27	
t_{RH}	3.3V Type 3 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	0.5		2	V/ns
t_{FH}	3.3V Type 3 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	0.5		2	

Type 5: PCI Clock Buffers (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-33			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-33	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.95V	30			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	
t_{RH}	3.3V Type 5 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	1		4	V/ns
t_{FH}	3.3V Type 5 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	1		4	

AC Timing

Figure 1. Host Clock to PCI CLK Offset	Parameters	66 MHz		100 MHz		Units
		Min.	Max.	Min.	Max.	
t_{HKP} (2.5V)	Host CLK period	15.0	15.5	10.0	10.5	ns
t_{HKH} (2.5V)	Host CLK high time	5.2		3.0		
t_{HKL} (2.5V)	Host CLK low time	5.0		2.8		
t_{HRISE} (2.5V)	Host CLK rise time	0.4	1.6	0.4	1.6	
t_{HFALL} (2.5V)	Host CLK fall time	0.4	1.6	0.4	1.6	
t_{JITTER} (2.5V)	Host CLK Jitter		250		250	ps
Duty Cycle (2.5V)	Measured at 1.25V	45	55	45	55	%
t_{HSKW} (2.5V)	Host Bus CLK Skew		175		175	ps
t_{PZL}, t_{PZH}	Output enable delay	1.0	8.0	1.0	8.0	ns
t_{PLZ}, t_{PHZ}	Output disable delay	1.0	8.0	1.0	8.0	
t_{HSTB}	Host CLK Stabilization from power-up		3		3	ms
t_{PKP}	PCI CLK period	30.0	∝	30.0	∝	ns
t_{PKPS}	PCI CLK period stability		500		500	ps
t_{PKH}	PCI CLK high time	12.0		12.0		ns
t_{PKL}	PCI CLK low time	12.0		12.0		
t_{PSKW}	PCI Bus CLK Skew		500		500	ps
$t_{HPOFFSET}$	Host to PCI Clock Offset	1.5	4.0	1.5	4.0	ns
t_{PSTB}	PCI CLK Stabilization from power-up		3		3	ms

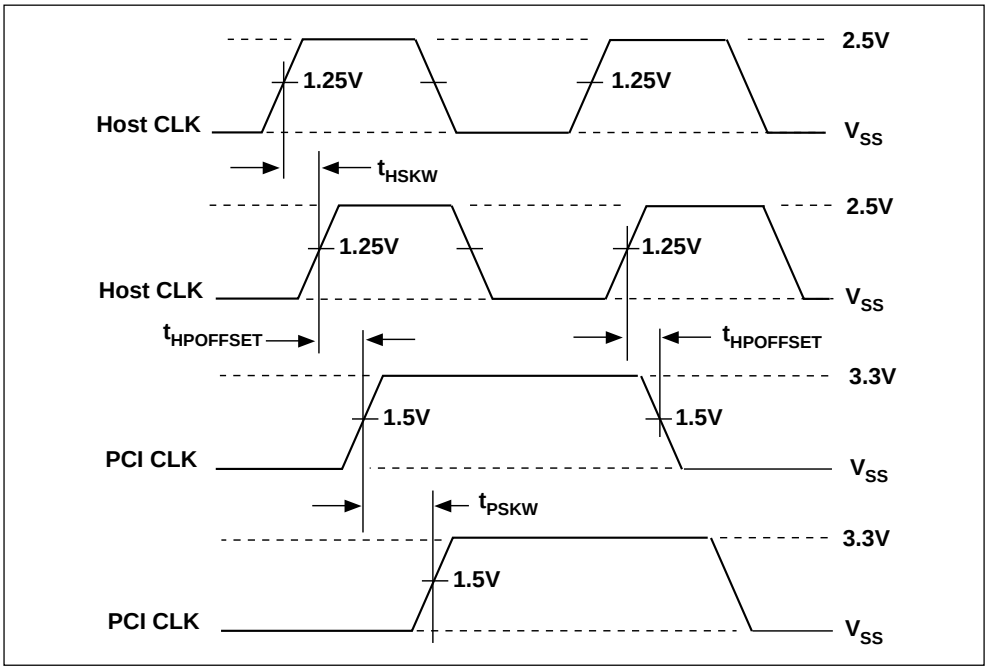


Figure 1. Host Clock and PCI CLK Timing

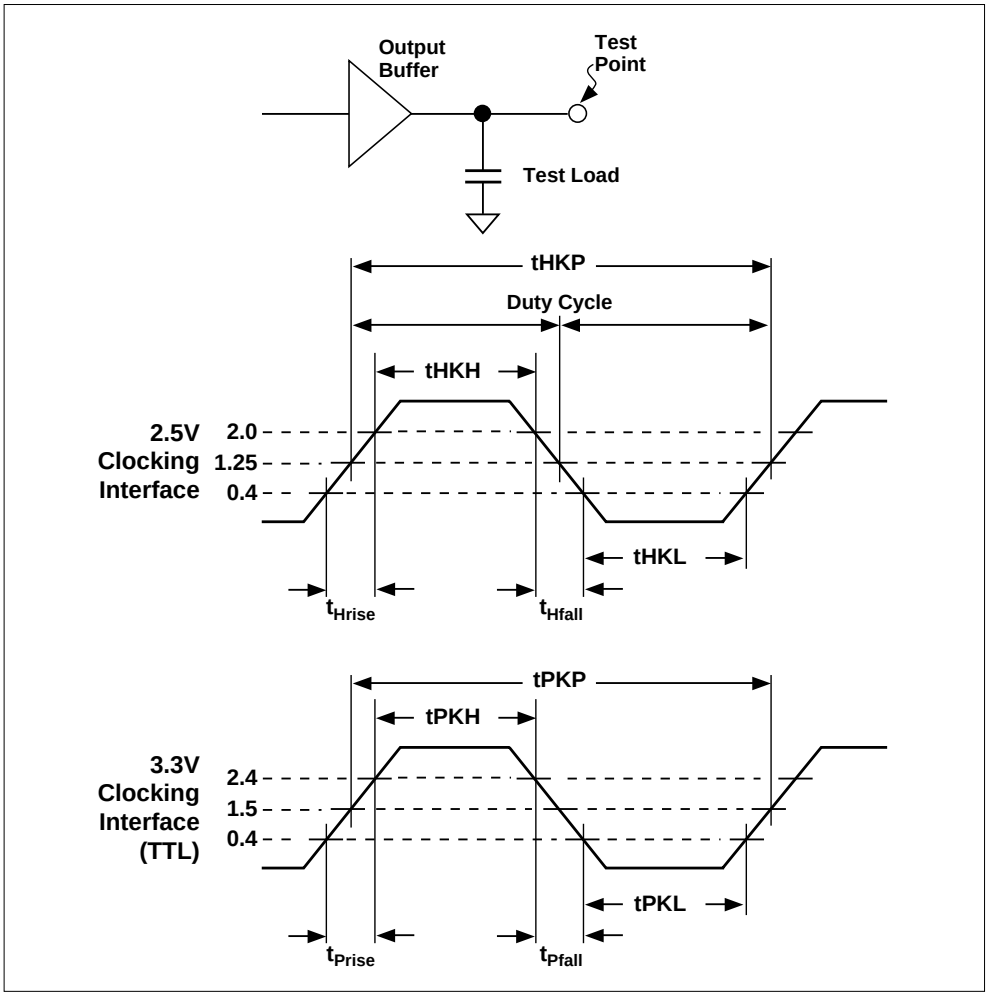


Figure 2. Clock Output Waveforms

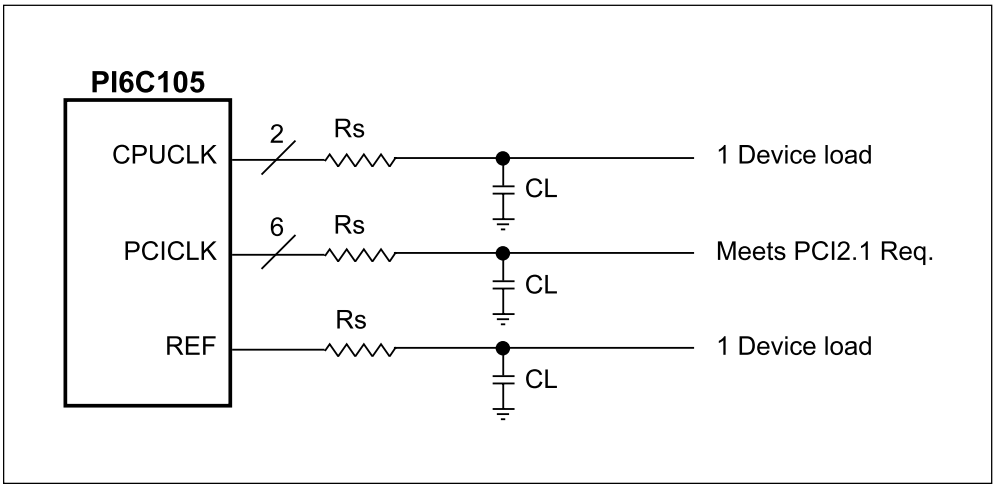
Minimum and Maximum Expected Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads
PCI Clocks (PCLK)	30	30		Meets PCI 2.1 requirements
REF, 48MHz	10	20		1 device load

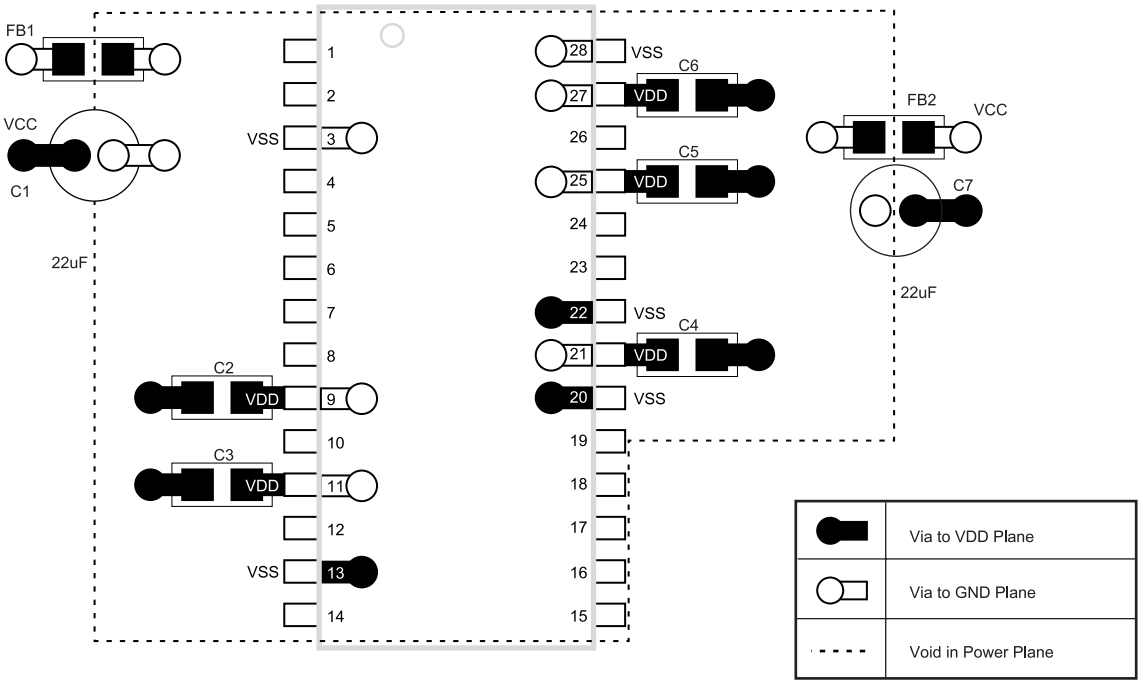
Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. R_S Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.



PCB Layout Suggestion



Note:

This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.

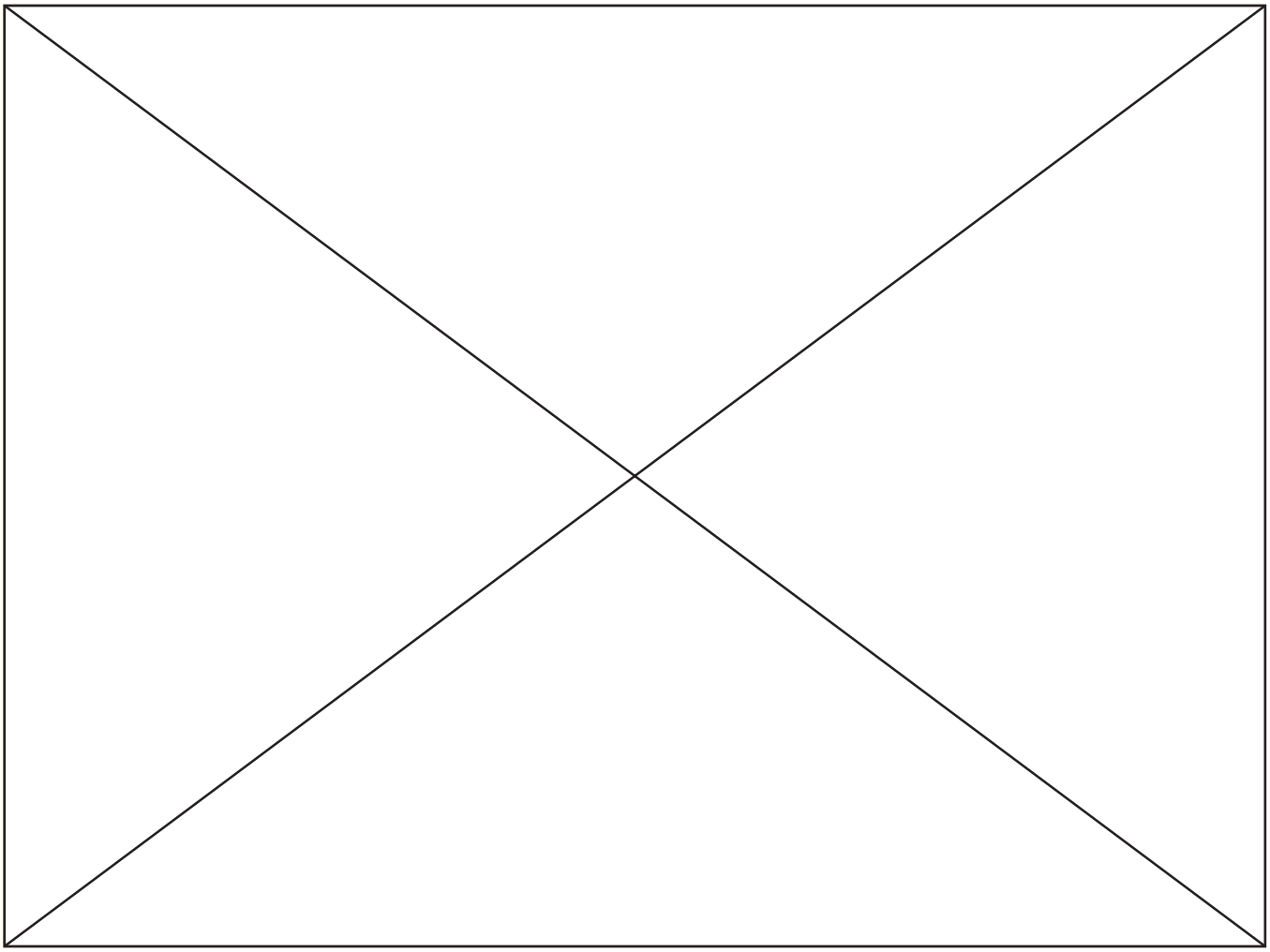
As a general rule, C2-C6 should be placed as close as possible to their respective V_{DD}.

Recommended capacitor values:

C2-C6 ..... 0.1uF, ceramic

C1, C7 ..... 22uF

28-Pin SSOP Package Data



Ordering Information

P/N	Description
PI6C105H	28-pin SSOP Package