

Product Features

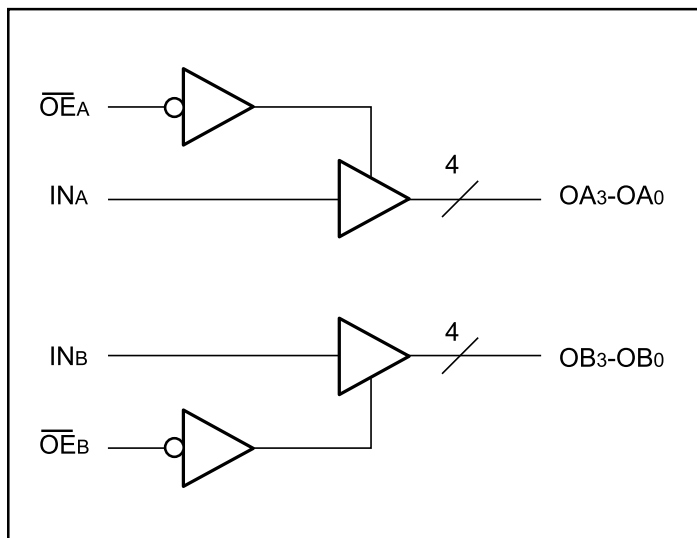
- Low output skew: 0.8ns
- Clock busing with Hi-Z state control
- TTL input and output levels, reducing problematic “ground bounce”
- High output drive, $I_{OL} = 64\text{mA}$
- Extremely low static power (1 mW, typ.)
- Hysteresis on all inputs
- Packages available:
 - 16-pin 300 mil wide plastic DIP (P)
 - 16-pin 300 mil wide plastic SOIC (S)

Product Description

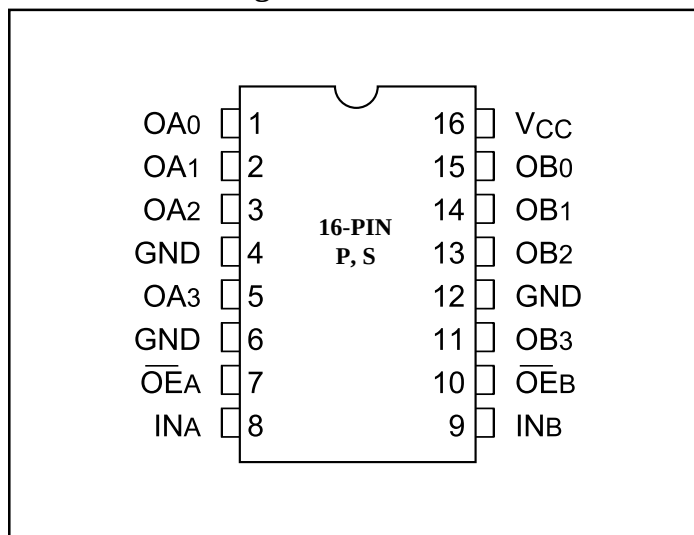
Pericom Semiconductor’s PI49FCT series of logic circuits are produced in the Company’s advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT804T is a non-inverting clock driver designed with two independent groups of buffers. These buffers have Hi-Z state Output Enable inputs (active LOW) with a 1-in, 4-out configuration per group. Each clock driver consists of two banks of drivers, driving four outputs each from a standard TTL compatible CMOS input.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{OE}_A, \overline{OE}_B$	Hi-Z State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_N, OB_N	Clock Outputs
GND	Ground
V_{CC}	Power

Truth Table⁽¹⁾

Inputs		Outputs
$\overline{OE}_A, \overline{OE}_B$	IN_A, IN_B	OA_N, OB_N
L	L	L
L	H	H
H	L	Z
H	H	Z

Note:

1. H = High Voltage Level
L = Low Voltage Level
Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = –24.0mA	2.4	3.3		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			–1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = V _{CC}			1	μA
I _{OZL}	Output Current		V _{OUT} = GND			–1	μA
I _I	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC} (Max.)				20	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = –18 mA			–0.7	–1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		–60	–120	–225	mA
V _H	Input Hysteresis	V _{CC} = 5V			200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		3	30	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Per Output Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _I = 10 MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Four Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND		6.2	11.2 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		6.4	12 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _I = 2.5 MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Eight Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND		3.1	6.3 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		3.5	7.6 ⁽⁵⁾	

Notes:

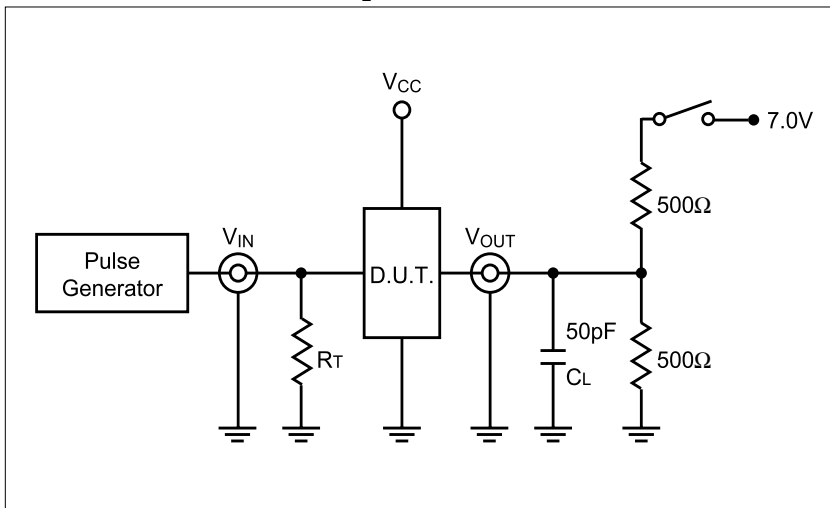
- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

PI49FCT804T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	804T		804AT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH tPHL	Propagation Delay I _{NA} to O _{AN} , I _{NB} to O _{BN}	C _L = 50 pF R _L = 500Ω	1.5	6.5	1.5	5.8	ns
tPZH tPZL	Output Enable Time O _{EA} to O _{AN} , O _{EB} to O _{BN}		1.5	8.0	1.5	8.0	ns
tPHZ tPLZ	Output Disable Time O _{EA} to O _{AN} , O _{EB} to O _{BN}		1.5	7.0	1.5	7.0	ns
tsKEW(o) ⁽³⁾	Skew between two outputs of same package (same transition)		—	0.8	—	0.7	ns
tsKEW(p) ⁽³⁾	Skew between opposite transitions (tPHL-tPLH) of the same output		—	1.0	—	0.8	ns
tsKEW(t) ⁽³⁾	Skew between two outputs of different package at same temperature (same transition)		—	1.6	—	1.4	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).

Tests Circuits For All Outputs⁽¹⁾

Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

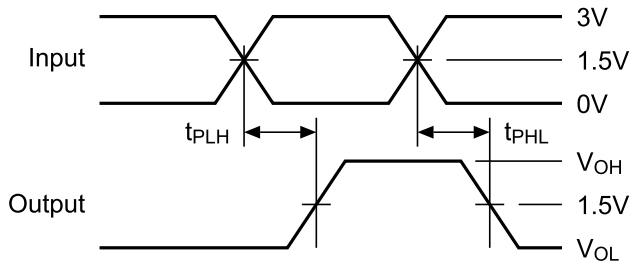
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

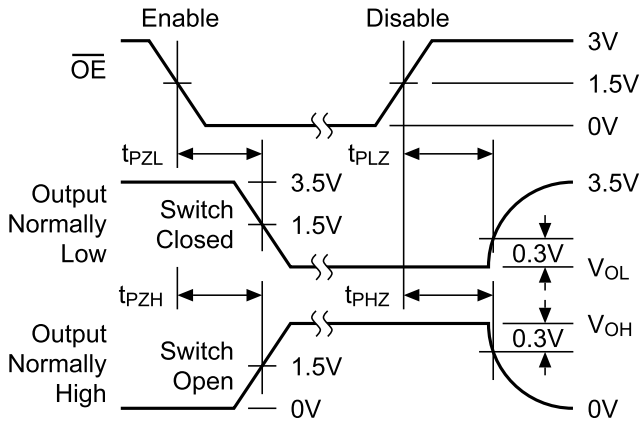
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Switching Waveforms

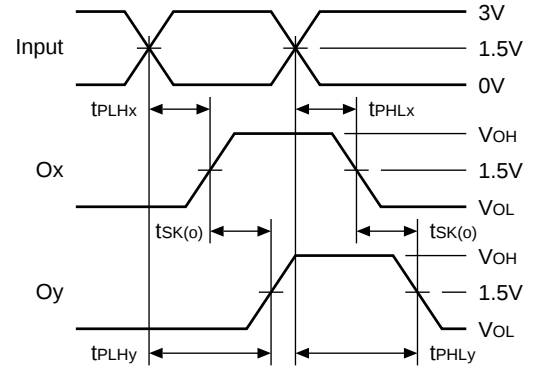
Propagation Delay



Enable and Disable Times

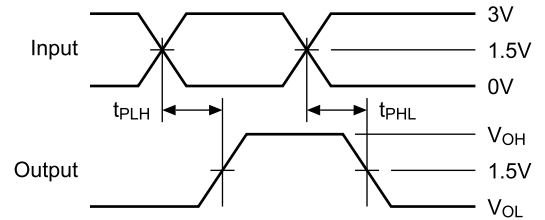


Output Skew – $t_{SK(o)}$



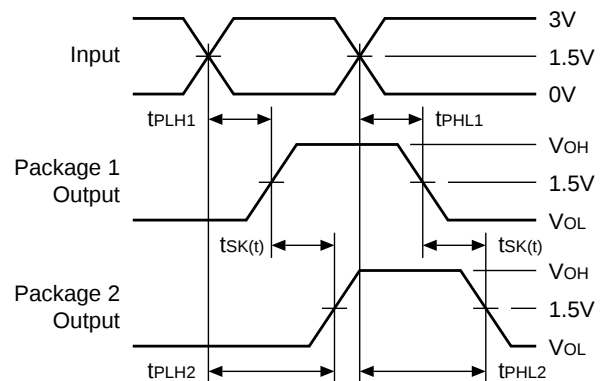
$$t_{SK(o)} = |t_{PLHy} - t_{PLHx}| \text{ OR } |t_{PHLy} - t_{PHLx}|$$

Pulse Skew – $t_{SK(p)}$



$$t_{SK(p)} = |t_{PHL} - t_{PLH}|$$

Package Skew – $t_{SK(t)}$



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ OR } |t_{PHL2} - t_{PHL1}|$$