



PCM1720

## *SoundPlus*™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER MPEG2/AC-3 COMPATIBLE

### FEATURES

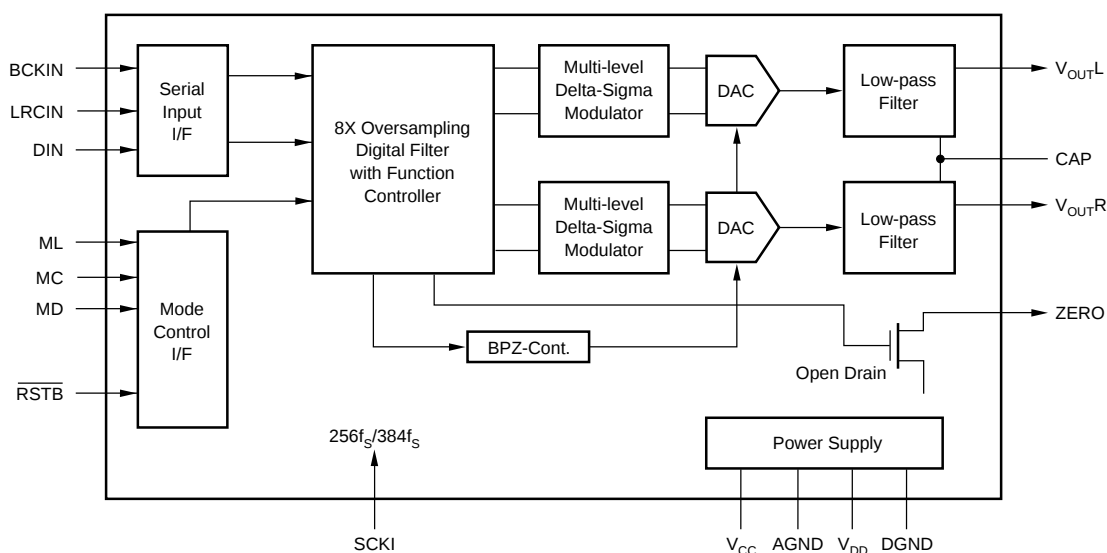
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 96dB
- MULTIPLE SAMPLING FREQUENCIES:  
16kHz to 96kHz  
8X Oversampling at All Sampling Frequencies
- SYSTEM CLOCK:  $256f_s/384f_s$
- NORMAL OR I<sup>2</sup>S DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:  
Soft Mute  
Digital Attenuator (256 Steps)  
Digital De-emphasis
- OUTPUT MODE: Left, Right, Mono, Mute

### DESCRIPTION

The PCM1720 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a  $256f_s$  or  $384f_s$  system clock. The DAC contains a 3rd-order  $\Delta\Sigma$  modulator, a digital interpolation filter, and an analog output amplifier. The PCM1720 can accept 16-, 20-, or 24-bit input data in either normal or I<sup>2</sup>S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PCM1720 can accept standard digital audio sampling frequencies as well as one-half and double sampling frequencies.

The PCM1720 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



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Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

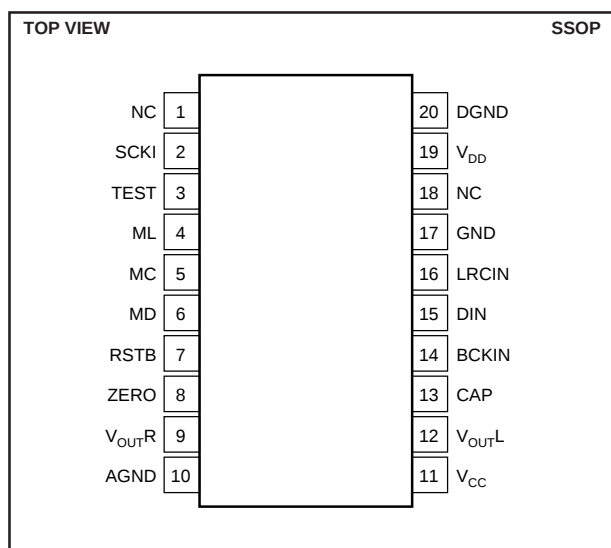
All specifications at +25°C, +V<sub>CC</sub> = +V<sub>DD</sub> = +5V, f<sub>S</sub> = 44.1kHz, and 16-bit input data, SYSCLK = 384f<sub>S</sub>, unless otherwise noted.

| PARAMETER                                                                                                                                                                                  | CONDITIONS                                                                                                                                                                                                                                           | PCM1720                              |                                                                                                                      |                                             | UNITS                                                         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------------------------|---------------------------------------------------------------|
|                                                                                                                                                                                            |                                                                                                                                                                                                                                                      | MIN                                  | TYP                                                                                                                  | MAX                                         |                                                               |
| <b>RESOLUTION</b>                                                                                                                                                                          |                                                                                                                                                                                                                                                      | 16                                   |                                                                                                                      | 24                                          | Bits                                                          |
| <b>DATA FORMAT</b><br>Audio Data Format<br>Data Bit Length<br><br>Sampling Frequency (f <sub>S</sub> )<br><br>Internal System Clock Frequency                                              | <br><br><br>Standard f <sub>S</sub><br>One-half f <sub>S</sub><br>Double f <sub>S</sub>                                                                                                                                                              | <br><br><br>32<br>16<br>64           | Standard/I <sup>2</sup> S<br>16/20/24<br>Selectable<br>44.1<br>22.05<br>88.2<br>256f <sub>S</sub> /384f <sub>S</sub> | <br><br><br>48<br>24<br>96                  | <br><br><br>kHz<br>kHz<br>kHz                                 |
| <b>DIGITAL INPUT/OUTPUT LOGIC LEVEL</b>                                                                                                                                                    |                                                                                                                                                                                                                                                      |                                      | TTL                                                                                                                  |                                             |                                                               |
| <b>DYNAMIC PERFORMANCE<sup>(1)</sup></b><br>THD+N at f <sub>S</sub> (0dB)<br><br>THD+N at -60dB<br><br>Dynamic Range<br><br>Signal-to-Noise Ratio <sup>(2)</sup><br><br>Channel Separation | <br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz<br>f <sub>S</sub> = 96kHz<br>f <sub>S</sub> = 44.1kHz | <br><br><br>90<br><br>92<br><br>90   | <br>-90<br>-88<br>-34<br>-31<br>96<br>93<br>100<br>97<br>97                                                          | <br>-80<br><br><br><br><br><br><br><br><br> | <br>dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB        |
| <b>DC ACCURACY</b><br>Gain Error<br>Gain Mismatch, Channel-to-Channel<br>Bipolar Zero Error                                                                                                | <br><br><br>V <sub>OUT</sub> = V <sub>CC</sub> /2 at BPZ                                                                                                                                                                                             |                                      | <br>±1.0<br>±1.0<br>±30                                                                                              | <br>±5.0<br>±5.0                            | <br>% of FSR<br>% of FSR<br>mV                                |
| <b>ANALOG OUTPUT</b><br>Output Voltage<br>Center Voltage<br>Load Impedance                                                                                                                 | <br>Full Scale (0dB)<br><br>AC Load                                                                                                                                                                                                                  | <br><br><br>5                        | <br>0.62 x V <sub>CC</sub><br>V <sub>CC</sub> /2                                                                     |                                             | <br>Vp-p<br>VDC<br>kΩ                                         |
| <b>DIGITAL FILTER PERFORMANCE</b><br>Passband<br>Stopband<br>Passband Ripple<br>Stopband Attenuation<br>Delay Time<br>De-emphasis Error                                                    |                                                                                                                                                                                                                                                      | <br><br>0.555<br><br>-35<br><br>-0.2 | <br><br><br>11.125/f <sub>S</sub>                                                                                    | <br><br><br>±0.17<br><br>+0.55              | <br>f <sub>S</sub><br>f <sub>S</sub><br>dB<br>dB<br>sec<br>dB |
| <b>INTERNAL ANALOG FILTER</b><br>-3dB Bandwidth<br>Passband Response                                                                                                                       | <br>f = 20kHz                                                                                                                                                                                                                                        |                                      | <br>100<br>-0.16                                                                                                     |                                             | <br>kHz<br>dB                                                 |
| <b>POWER SUPPLY REQUIREMENTS</b><br>Voltage Range<br>Supply Current: I <sub>CC</sub> + I <sub>DD</sub>                                                                                     | <br>V <sub>DD</sub> , V <sub>CC</sub><br>V <sub>CC</sub> = V <sub>DD</sub> = 5V, f <sub>S</sub> = 44.1kHz<br>V <sub>CC</sub> = V <sub>DD</sub> = 5V, f <sub>S</sub> = 96kHz                                                                          | <br>4.5                              | <br>5<br>18<br>25                                                                                                    | <br>5.5<br>25<br>35                         | <br>VDC<br>mA<br>mA                                           |
| <b>TEMPERATURE RANGE</b><br>Operation<br>Storage                                                                                                                                           |                                                                                                                                                                                                                                                      | <br>-25<br>-55                       |                                                                                                                      | <br>+85<br>+100                             | <br>°C<br>°C                                                  |

NOTES: (1) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (2) SNR is tested with Infinite Zero Detection off.

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## PIN CONFIGURATION



## PACKAGE INFORMATION

| PRODUCT | PACKAGE     | PACKAGE DRAWING NUMBER <sup>(1)</sup> |
|---------|-------------|---------------------------------------|
| PCM1720 | 20-Pin SSOP | 334-1                                 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

|                                                 |                                   |
|-------------------------------------------------|-----------------------------------|
| Power Supply Voltage                            | +6.5V                             |
| +V <sub>CC</sub> to +V <sub>DD</sub> Difference | ±0.1V                             |
| Input Logic Voltage                             | −0.3V to (V <sub>DD</sub> + 0.3V) |
| Power Dissipation                               | 300mW                             |
| Operating Temperature Range                     | −25°C to +85°C                    |
| Storage Temperature                             | −55°C to +125°C                   |
| Lead Temperature (soldering, 5s)                | +260°C                            |
| Thermal Resistance, $\theta_{JA}$               | +70°C/W                           |

## PIN ASSIGNMENTS

| PIN | NAME              | TYPE | FUNCTION                                                                                                 |
|-----|-------------------|------|----------------------------------------------------------------------------------------------------------|
| 1   | NC                | —    | No Connection.                                                                                           |
| 2   | SCKI              | IN   | System Clock Input: 256f <sub>S</sub> or 384f <sub>S</sub> .                                             |
| 3   | TEST              | OUT  | Reserved for Factory Use.                                                                                |
| 4*  | ML                | IN   | Latch Enable for Serial Control Data.                                                                    |
| 5*  | MC                | IN   | Clock for Serial Control Data.                                                                           |
| 6*  | MD                | IN   | Data Input for Serial Control.                                                                           |
| 7*  | RSTB              | IN   | Reset Input. When this pin is low, the digital filters and modulators are held in reset.                 |
| 8   | ZERO              | OUT  | Zero Data Flag. This pin is low when the data is continuously zero for more than 65,535 cycles of BCKIN. |
| 9   | V <sub>OUTR</sub> | OUT  | Right Channel Analog Output.                                                                             |
| 10  | AGND              | PWR  | Analog Ground.                                                                                           |
| 11  | V <sub>CC</sub>   | PWR  | Analog Power Supply (+5V).                                                                               |
| 12  | V <sub>OUTL</sub> | OUT  | Left Channel Analog Output.                                                                              |
| 13  | CAP               | —    | Common Pin for Analog Output Amplifiers.                                                                 |
| 14* | BCKIN             | IN   | Bit Clock for Clocking in the Audio Data.                                                                |
| 15* | DIN               | IN   | Serial Audio Data Input.                                                                                 |
| 16* | LRCIN             | IN   | Left/Right Word Clock. Frequency is equal to fs.                                                         |
| 17  | GND               | PWR  | Ground.                                                                                                  |
| 18  | NC                | —    | No Connection.                                                                                           |
| 19  | V <sub>DD</sub>   | PWR  | Digital Power Supply (+5V). Recommended connection is to the analog power supply.                        |
| 20  | DGND              | PWR  | Digital Ground. Recommended connection is to the digital ground plane.                                   |

\* These pins include internal pull-up resistors.



## ELECTROSTATIC DISCHARGE SENSITIVITY

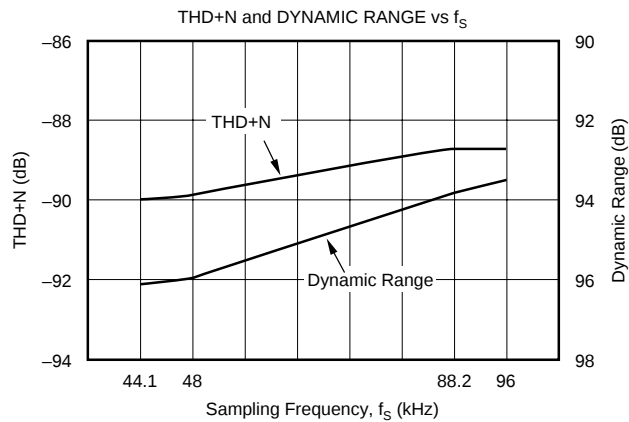
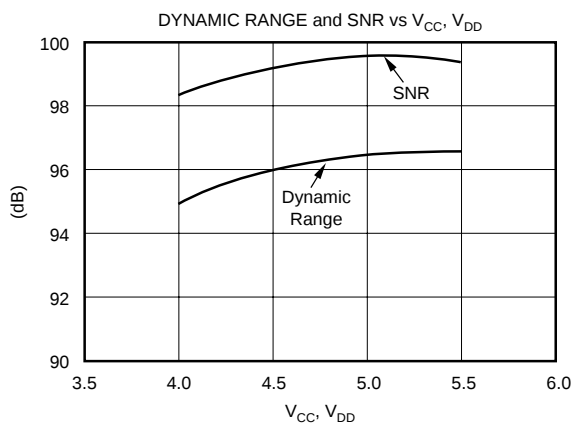
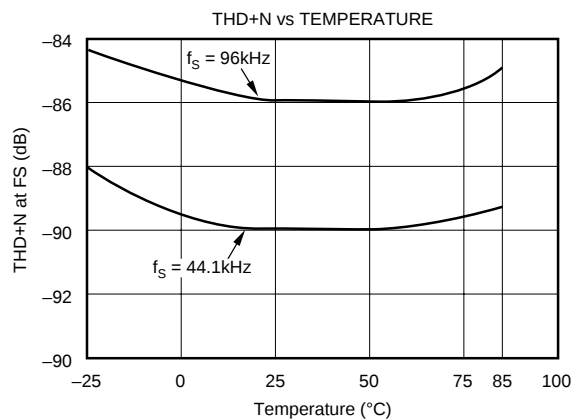
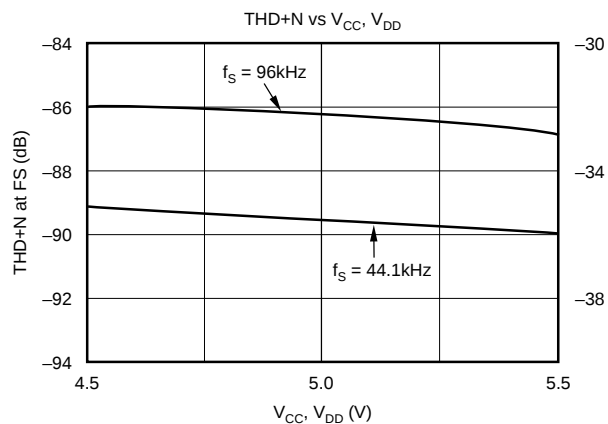
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , 16-bit input data, unless otherwise noted. Measurement bandwidth is 20kHz

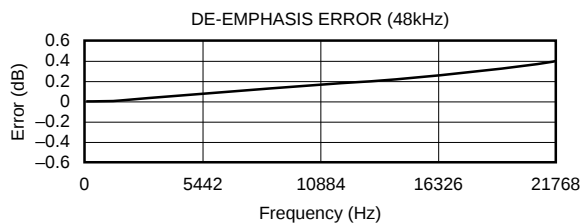
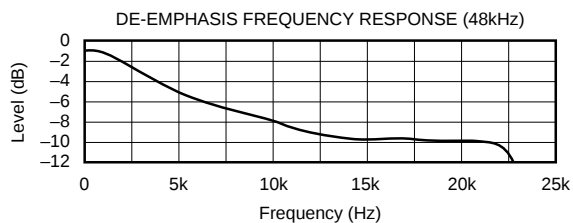
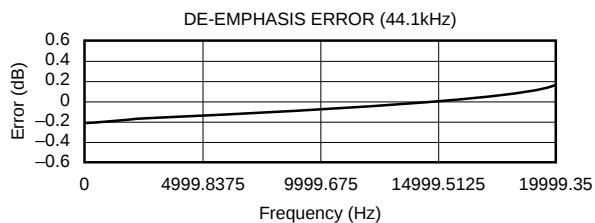
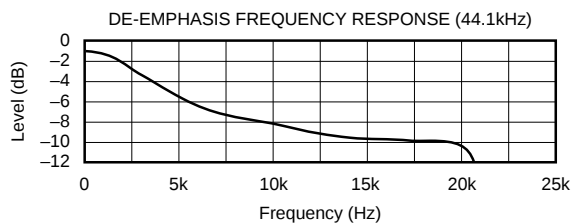
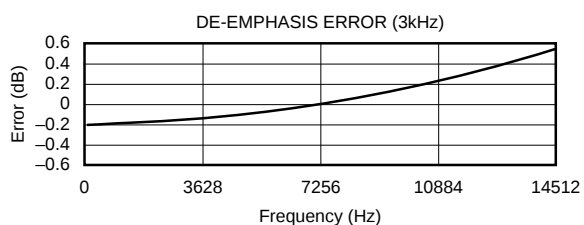
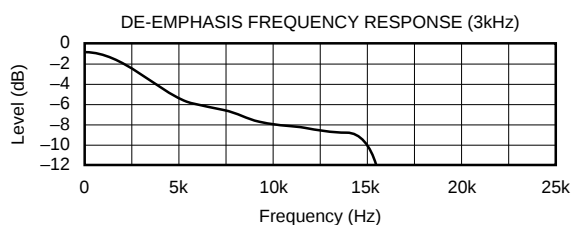
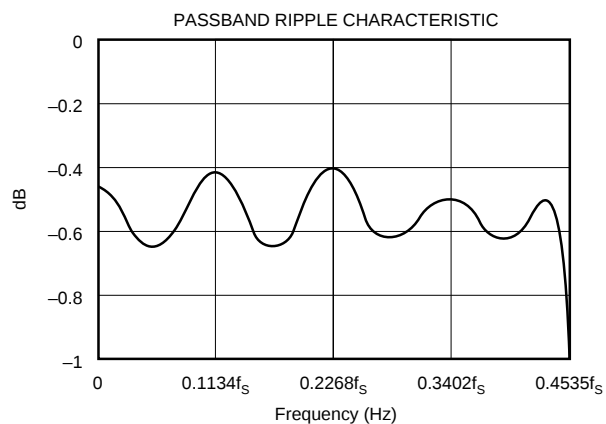
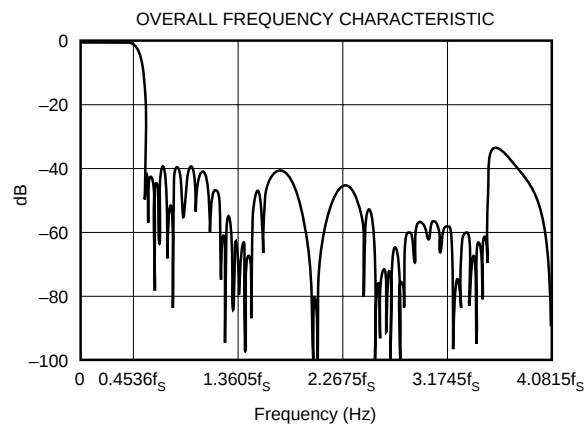
## DYNAMIC PERFORMANCE



# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = +5\text{V}$ ,  $R_L = 44.1\text{kHz}$ ,  $f_{\text{SYS}} = 384f_s$ , and 16-bit input data, unless otherwise noted.

## DIGITAL FILTER



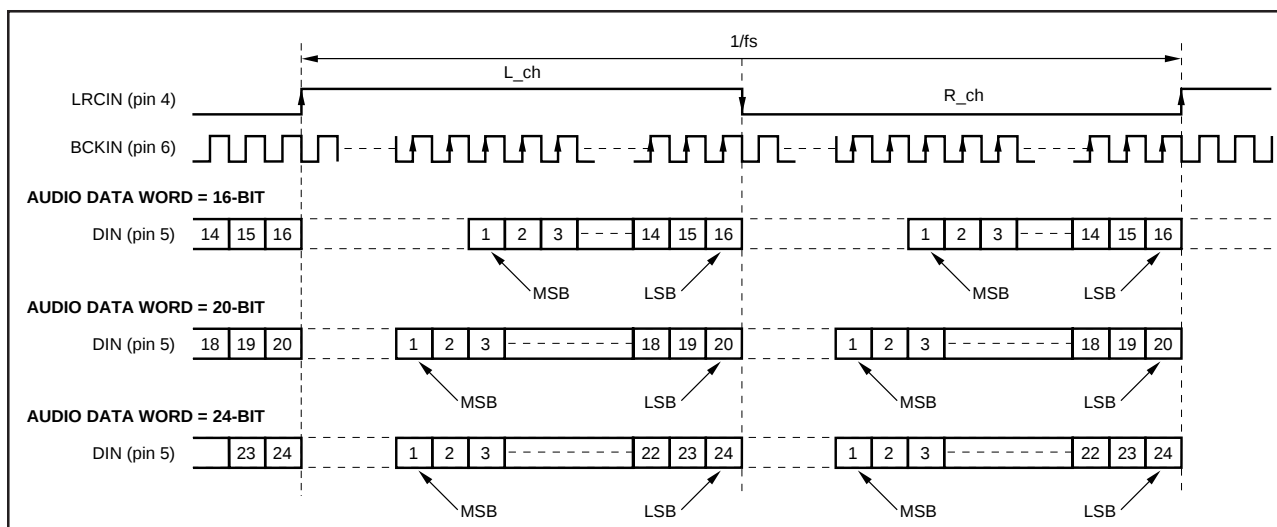


FIGURE 1. "Normal" Data Input Timing.

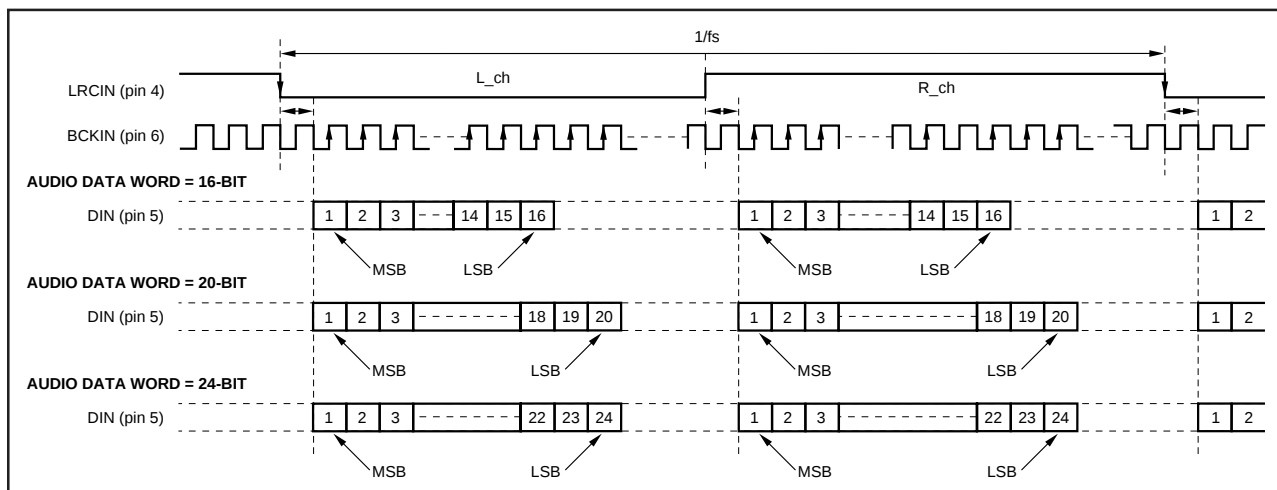


FIGURE 2. "I²S" Data Input Timing.

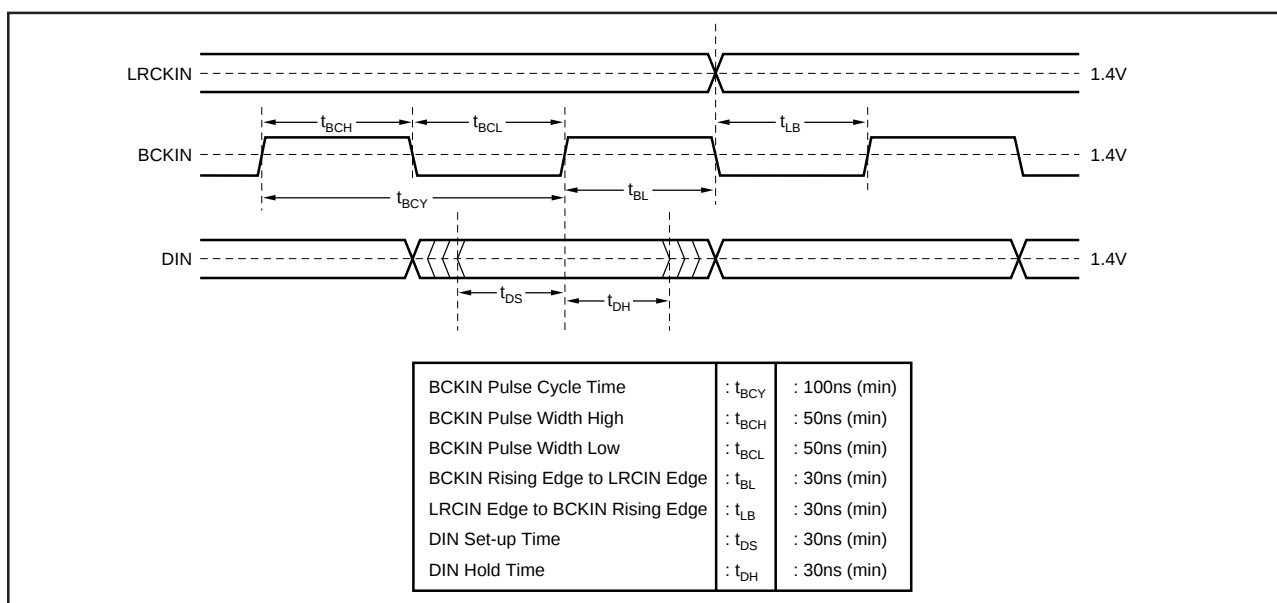


FIGURE 3. Audio Data Input Timing.

## TYPICAL CONNECTION DIAGRAM

Figure 4 illustrates the typical connection diagram for PCM1720 used in a stand-alone application.

## SYSTEM CLOCK

The system clock for PCM1720 must be either  $256f_s$  or  $384f_s$ , where  $f_s$  is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz or 48kHz. The system clock is used to operate the digital filter and the noise shaper. The system clock input (SCKI) is at pin 2.

PCM1720 has a system clock detection circuit which automatically detects the frequency, either  $256f_s$  or  $384f_s$ . The system clock should be synchronized with LRCIN (pin 16), but PCM1720 can compensate for phase differences. If the phase difference between LRCIN and system clock is greater than  $\pm 6$  bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state ( $V_{CC}/2$ ) during the synchronization function. Table I shows the typical system clock frequency inputs for the PCM1720.

| SAMPLING RATE (LRCIN) | SYSTEM CLOCK FREQUENCY (MHz) |          |
|-----------------------|------------------------------|----------|
|                       | $256f_s$                     | $384f_s$ |
| 32kHz                 | 8.192                        | 12.288   |
| 44.1kHz               | 11.2896                      | 16.9340  |
| 48kHz                 | 12.288                       | 18.432   |

TABLE I. System Clock Frequencies vs Sampling Rate.

## SPECIAL FUNCTIONS

PCM1720 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 6) is used for the program data, MC (pin 5) is used to clock in the program data, and ML (pin 4) is used to latch in the program data. Table II lists the selectable special functions.

| FUNCTION                                                                         | DEFAULT MODE                       |
|----------------------------------------------------------------------------------|------------------------------------|
| Input Audio Data Format Selection<br>Normal Format<br>I <sup>2</sup> S Format    | Normal Format                      |
| Input Audio Data Bit Selection<br>16/20/24 Bits                                  | 16 Bits                            |
| Input LRCIN Polarity Selection<br>Lch/Rch = High/Low<br>Lch/Rch = Low/High       | Lch/Rch = High/Low                 |
| De-emphasis Control                                                              | OFF                                |
| Soft Mute Control                                                                | OFF                                |
| Attenuation Control<br>Lch, Rch Individually<br>Lch, Rch Common                  | 0dB<br>Lch, Rch Individually Fixed |
| Infinite Zero Detection Circuit Control                                          | OFF                                |
| Operation Enable (OPE)                                                           | Enabled                            |
| Sample Rate Selection<br>Internal System Clock Selection<br>$256f_s$<br>$384f_s$ | $384f_s$                           |
| Sampling Frequency<br>44.1kHz Group<br>48kHz Group<br>32kHz Group                | 44.1kHz                            |
| Analog Output Mode<br>L, R, Mono, Mute                                           | Stereo                             |

TABLE II. Selectable Functions.

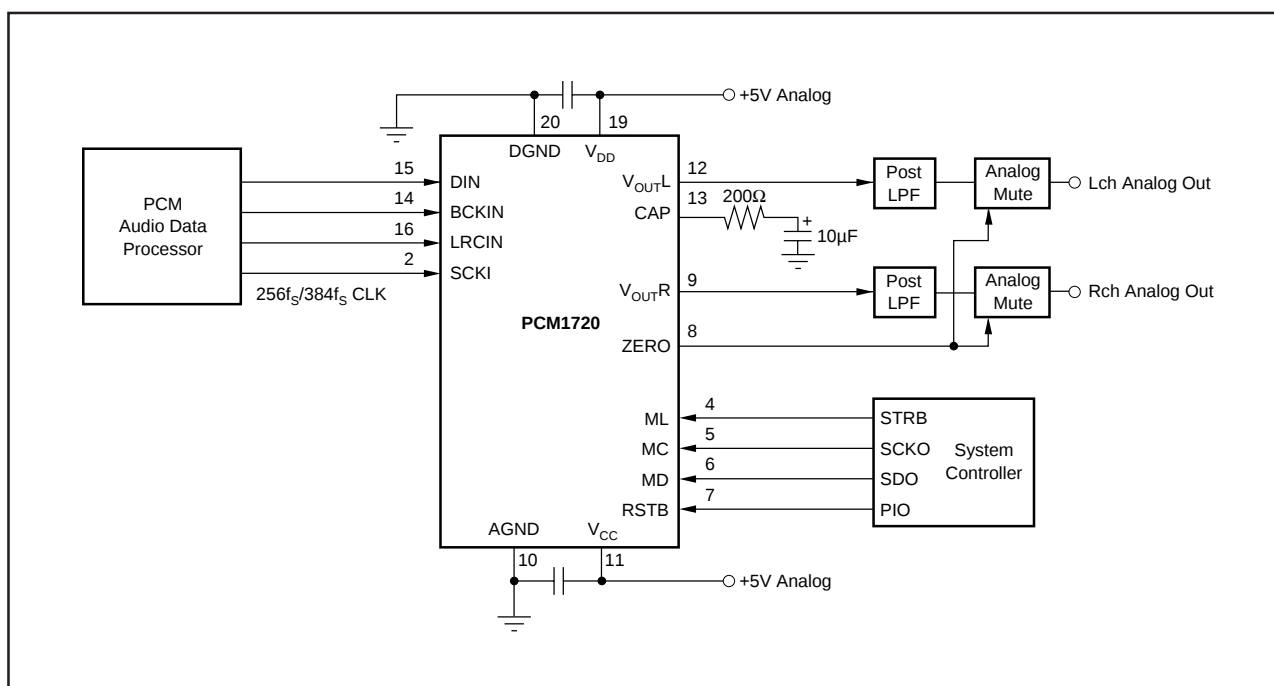


FIGURE 4. Typical Connection Diagram.

## MAPPING OF PROGRAM REGISTERS

|            | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0               |
|------------|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------------------|
| REGISTER 0 | res | res | res | res | res | A1  | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0              |
| REGISTER 1 | res | res | res | res | res | A1  | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0              |
| REGISTER 2 | res | res | res | res | res | A1  | A0 | PL3 | PL2 | PL1 | PL0 | IW1 | IW0 | OPE | DEM | MUT              |
| REGISTER 3 | res | res | res | res | res | A1  | A0 | IZD | SF1 | SF0 | res | res | res | ATC | LRP | I <sup>2</sup> S |

## PROGRAM REGISTER BIT MAPPING

PCM1720's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table III shows the complete mapping of the four registers and Figure 6 illustrates the data input timing.

| REGISTER NAME | BIT NAME                                                                   | DESCRIPTION                                                                                                                                                                                                  |
|---------------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Register 0    | AL (7:0)<br>LDL<br>A (1:0)<br>res                                          | DAC Attenuation Data for Lch<br>Attenuation Data Load Control for Lch<br>Register Address<br>Reserved                                                                                                        |
| Register 1    | AR (7:0)<br>LDL<br>A (1:0)<br>res                                          | DAC Attenuation Data for Rch<br>Attenuation Data Load Control for Rch<br>Register Address<br>Reserved                                                                                                        |
| Register 2    | MUT<br>DEM<br>OPE<br>IW (1:0)<br>PL (3:0)<br>A (1:0)<br>res                | Left and Right DACs Soft Mute Control<br>De-emphasis Control<br>Left and Right DACs Operation Control<br>Input Audio Data Bit Select<br>Output Mode Select<br>Register Address<br>Reserved                   |
| Register 3    | I <sup>2</sup> S<br>LRP<br>ATC<br>SYS<br>SF (1:0)<br>IZD<br>A (1:0)<br>res | Audio Data Format Select<br>Polarity of LRCIN (pin 7) Select<br>Attenuator Control<br>System Clock Select<br>Sampling Rate Select<br>Infinite Zero Detection Circuit Control<br>Register Address<br>Reserved |

TABLE III. Internal Register Mapping.

### REGISTER 0 (A1 = 0, A0 = 0)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1  | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20 \log_{10} (ATT\_DATA/255)] \text{ dB}$$

### ATTENUATION DATA LOAD CONTROL, LCH

Bit 8 (LDL) is used to simultaneously set analog outputs of Lch and Rch. An output level is controlled by AL[0:7] attenuation data when this bit is set to 1. When set to 0, an output level is not controlled and remains at the previous attenuation level. A LDR bit in Register 1 has an equivalent function as the LDL. When one of LDL or LDR is set to 1, the output level of the left and right channel is simultaneously controlled. The attenuation level is given by:

$$ATT = 20 \log (y/256) \text{ (dB)}, \text{ where } y = x, \text{ when } 0 \leq x \leq 254$$

$$y = x + 1, \text{ when } x = 255$$

X is the user-determined step number, an integer value between 0 and 255.

Example:

let x = 255

$$ATT = 20 \log \left( \frac{255+1}{256} \right) = 0 \text{ dB}$$

let x = 254

$$ATT = 20 \log \left( \frac{254}{256} \right) = -0.068 \text{ dB}$$

let x = 1

$$ATT = 20 \log \left( \frac{1}{256} \right) = -48.16 \text{ dB}$$

let x = 0

$$ATT = 20 \log \left( \frac{0}{256} \right) = -\infty$$

### REGISTER 1 (A1 = 0, A0 = 1)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| res | res | res | res | res | A1  | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

## REGISTER 2 (A1 = 1, A0 = 0)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0   |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| res | res | res | res | res | A1  | A0 | PL3 | PL2 | PL1 | PL0 | IW1 | IW0 | OPE | DEM | MUTE |

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a “HIGH” level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no “click” is audible). Bit 1 is used to control de-emphasis. A “LOW” level on bit 1 disables de-emphasis, while a “HIGH” level enables de-emphasis.

Bit 2, (OPE) is used for operational control. Table IV illustrates the features controlled by OPE.

|         | DATA INPUT | DAC OUTPUT                   | SOFTWARE MODE INPUT |
|---------|------------|------------------------------|---------------------|
| OPE = 1 | Zero       | Forced to BPZ <sup>(1)</sup> | Enabled             |
|         | Other      | Forced to BPZ <sup>(1)</sup> | Enabled             |
| OPE = 0 | Zero       | Controlled by IZD            | Enabled             |
|         | Other      | Normal                       | Enabled             |

TABLE IV. Output Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is “LOW”, the DAC will convert all non-zero input data. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be forced to zero only if IZD is “HIGH”. When OPE is “HIGH”, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

|         | DATA INPUT | DAC OUTPUT                   |
|---------|------------|------------------------------|
| IZD = 1 | Zero       | Forced to BPZ <sup>(1)</sup> |
|         | Other      | Normal                       |
| IZD = 0 | Zero       | Zero <sup>(2)</sup>          |
|         | Other      | Normal                       |

TABLE V. Infinite Zero Detection (IZD) Function.

|               | DATA INPUT | DAC OUTPUT                   | SOFTWARE MODE INPUT |
|---------------|------------|------------------------------|---------------------|
| RSTB = “HIGH” | Zero       | Controlled by OPE and IZD    | Enabled             |
|               | Other      | Controlled by OPE and IZD    | Enabled             |
| RSTB = “LOW”  | Zero       | Forced to BPZ <sup>(1)</sup> | Disabled            |
|               | Other      | Forced to BPZ <sup>(1)</sup> | Disabled            |

TABLE VI. Reset (RSTB) Function.

NOTE: (1)  $\Delta\Sigma$  is disconnected from output amplifier. (2)  $\Delta\Sigma$  is connected to output amplifier.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1720 can be set up for input word resolutions of 16, 20, or 24 bits:

| Bit 4 (IW1) | Bit 3 (IW0) | Input Resolution |
|-------------|-------------|------------------|
| 0           | 0           | 16-bit Data Word |
| 0           | 1           | 20-bit Data Word |
| 1           | 0           | 24-bit Data Word |
| 0           | 0           | Reserved         |

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1720 can be programmed for 16 different states, as shown in Table VII.

| PL0 | PL1 | PL2 | PL3 | Lch OUTPUT | Rch OUTPUT | NOTE    |
|-----|-----|-----|-----|------------|------------|---------|
| 0   | 0   | 0   | 0   | MUTE       | MUTE       | MUTE    |
| 0   | 0   | 0   | 1   | MUTE       | R          |         |
| 0   | 0   | 1   | 0   | MUTE       | L          |         |
| 0   | 0   | 1   | 1   | MUTE       | (L + R)/2  |         |
| 0   | 1   | 0   | 0   | R          | MUTE       |         |
| 0   | 1   | 0   | 1   | R          | R          |         |
| 0   | 1   | 1   | 0   | R          | L          | REVERSE |
| 0   | 1   | 1   | 1   | R          | (L + R)/2  |         |
| 1   | 0   | 0   | 0   | L          | MUTE       |         |
| 1   | 0   | 0   | 1   | L          | R          | STEREO  |
| 1   | 0   | 1   | 0   | L          | L          |         |
| 1   | 0   | 1   | 1   | L          | (L + R)/2  |         |
| 1   | 1   | 0   | 0   | (L + R)/2  | MUTE       |         |
| 1   | 1   | 0   | 1   | (L + R)/2  | R          |         |
| 1   | 1   | 1   | 0   | (L + R)/2  | L          |         |
| 1   | 1   | 1   | 1   | (L + R)/2  | (L + R)/2  | MONO    |

TABLE VII. Programmable Output Format.

## REGISTER 3 (A1 = 1, A0 = 1)

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8  | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0               |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------------------|
| res | res | res | res | res | A1  | A0 | IZD | SF1 | SF0 | res | res | res | ATC | LRP | I <sup>2</sup> S |

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency and infinite zero detection.

Bits 0 (I<sup>2</sup>S) and 1 (LRP) are used to control the input data format. A “LOW” on bit 0 sets the format to “Normal” (MSB-first, right-justified Japanese format) and a “HIGH” sets the format to I<sup>2</sup>S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is “LOW”, left channel data is assumed when LRCIN is in a “HIGH” phase and right channel data is assumed when LRCIN is in a “LOW” phase. When bit 1 is “HIGH”, the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is “HIGH”, the attenuation data loaded in program Register 0 is used for both left and right channels. When bit 2 is “LOW”, the attenuation data for each register is applied separately to left and right channels.

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency:

| SF1 | SF0 | Sampling Frequency |                    |
|-----|-----|--------------------|--------------------|
| 0   | 0   | 44.1kHz group      | 22.05/44.1/88.2kHz |
| 0   | 1   | 48kHz group        | 24/48/96kHz        |
| 1   | 0   | 32kHz group        | 16/32/64kHz        |
| 1   | 1   | Reserved           | Not Defined        |

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is “LOW”, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is “HIGH”, the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ( $V_{CC}/2$ ). The zero detection

feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1720 allows the zero detect feature to be disabled so the user can implement external muting circuit.

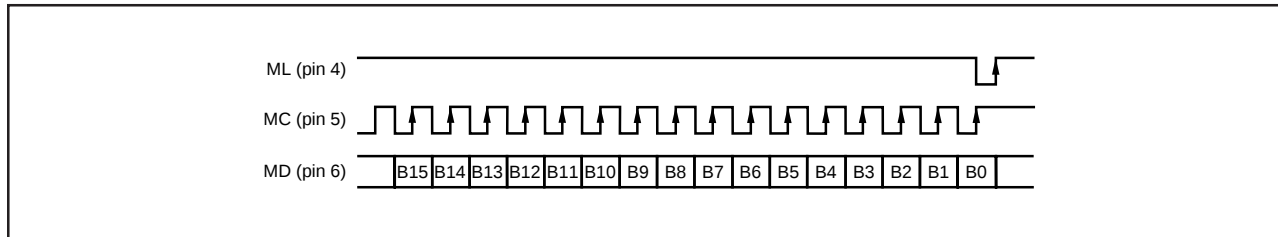


FIGURE 5. Serial Interface Timing.

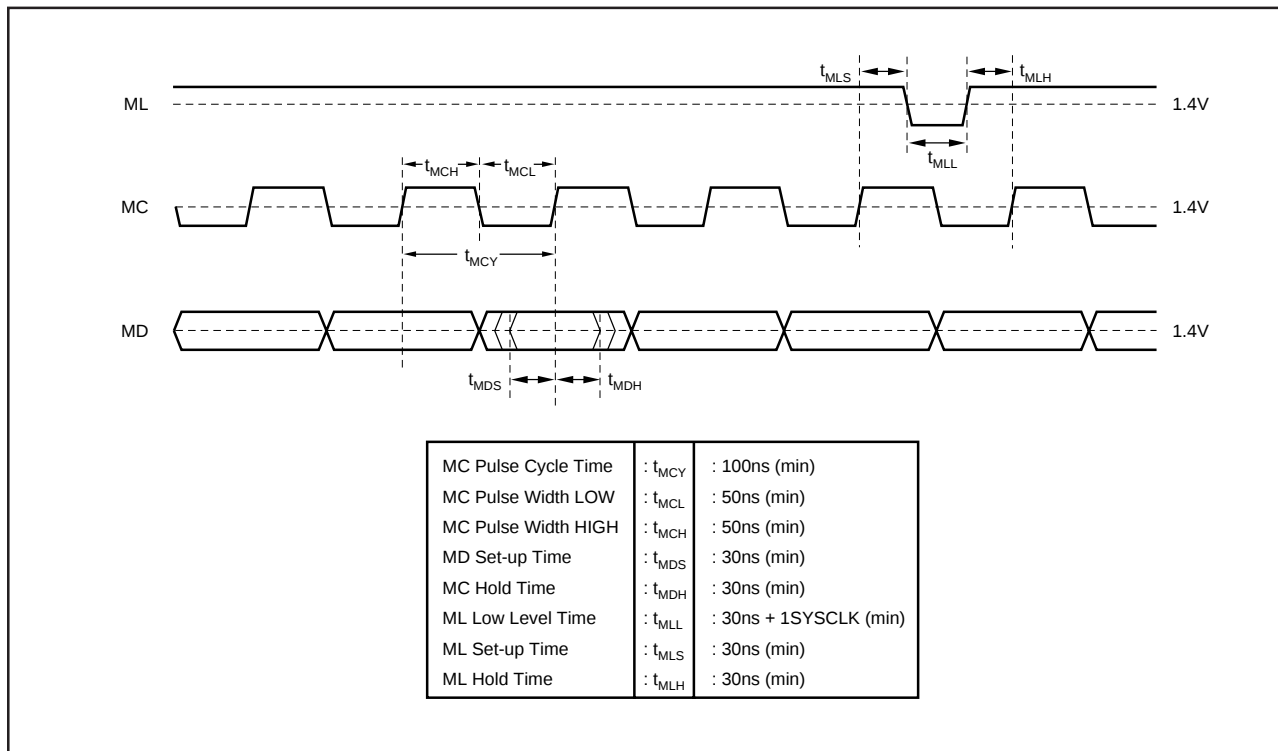


FIGURE 6. Program Register Input Timing.

# APPLICATION CONSIDERATIONS

## DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1720:

$$T_D = 11.125 \times 1/f_S$$

For  $f_S = 44.1\text{kHz}$ ,  $T_D = 11.125/44.1\text{kHz} = 251.4\mu\text{s}$

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

## OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1720 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 7. The higher frequency rolloff of the filter is shown in Figure 8. If the user's application has the PCM1720 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 9. For some applications, a passive RC filter or 2nd-order filter may be adequate.

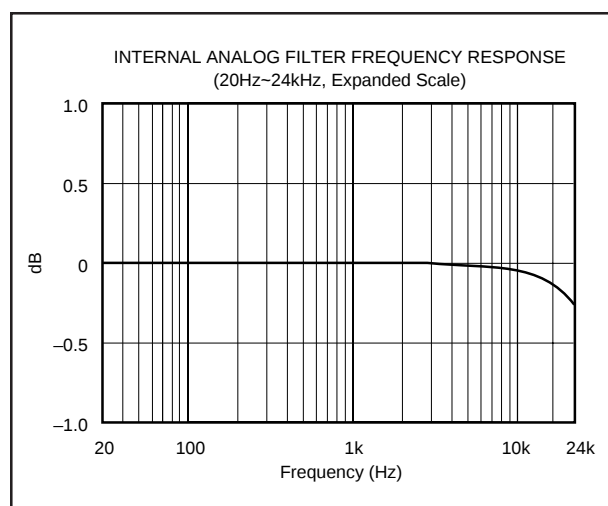


FIGURE 7. Low Pass Filter Frequency Response.

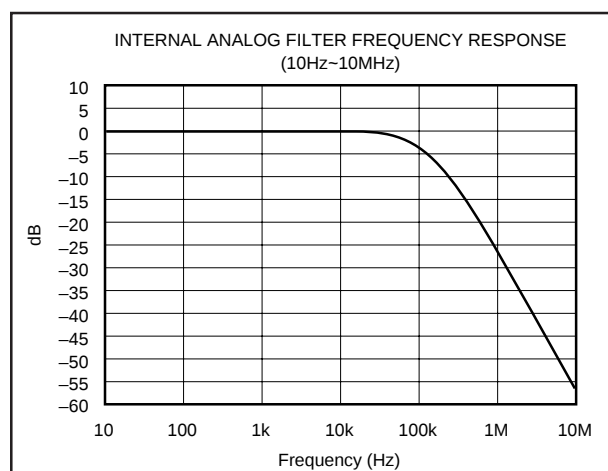


FIGURE 8. Low Pass Filter Wideband Frequency Response.

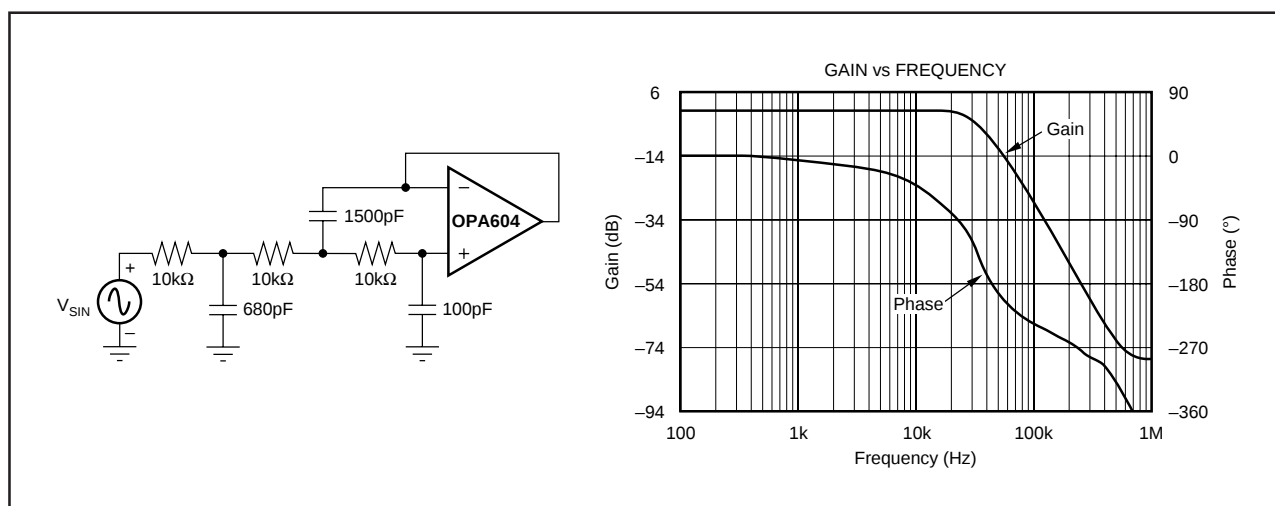


FIGURE 9. 3rd-Order LPF.

## POWER SUPPLY CONNECTIONS

PCM1720 has two power supply connections: digital ( $V_{DD}$ ) and analog ( $V_{CC}$ ). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 10.

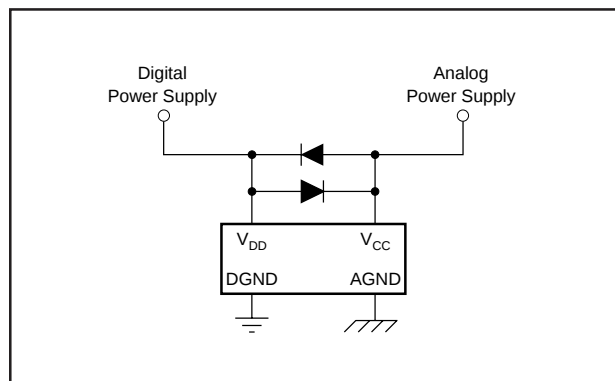


FIGURE 10. Latch-up Prevention Circuit.

## BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 13 for optimal values of bypass capacitors. It is also recommended to include a 0.1 $\mu$ F ceramic capacitor in parallel with the 10 $\mu$ F tantalum capacitor.

## THEORY OF OPERATION

The delta-sigma section of PCM1720 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 11. This 5-level delta-sigma modulator has the advantage of stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is  $48f_s$  for a  $384f_s$  system clock, and  $64f_s$  for a  $256f_s$  system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 12.

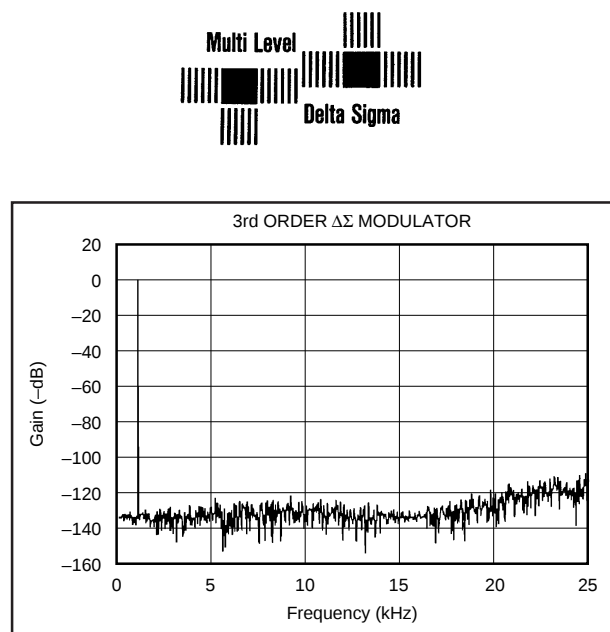


FIGURE 12. Quantization Noise Spectrum.

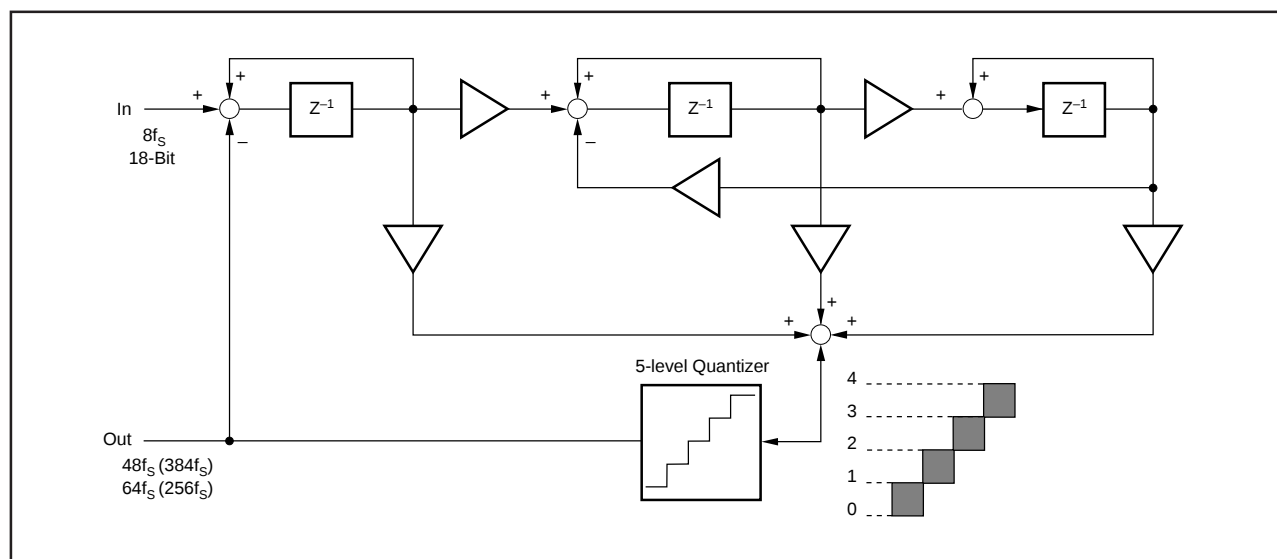


FIGURE 11. 5-Level  $\Delta\Sigma$  Modulator Block Diagram.

## AC-3 APPLICATION

Figure 13 shows the typical circuit diagram for Dolby AC-3, 5.1 channel system.

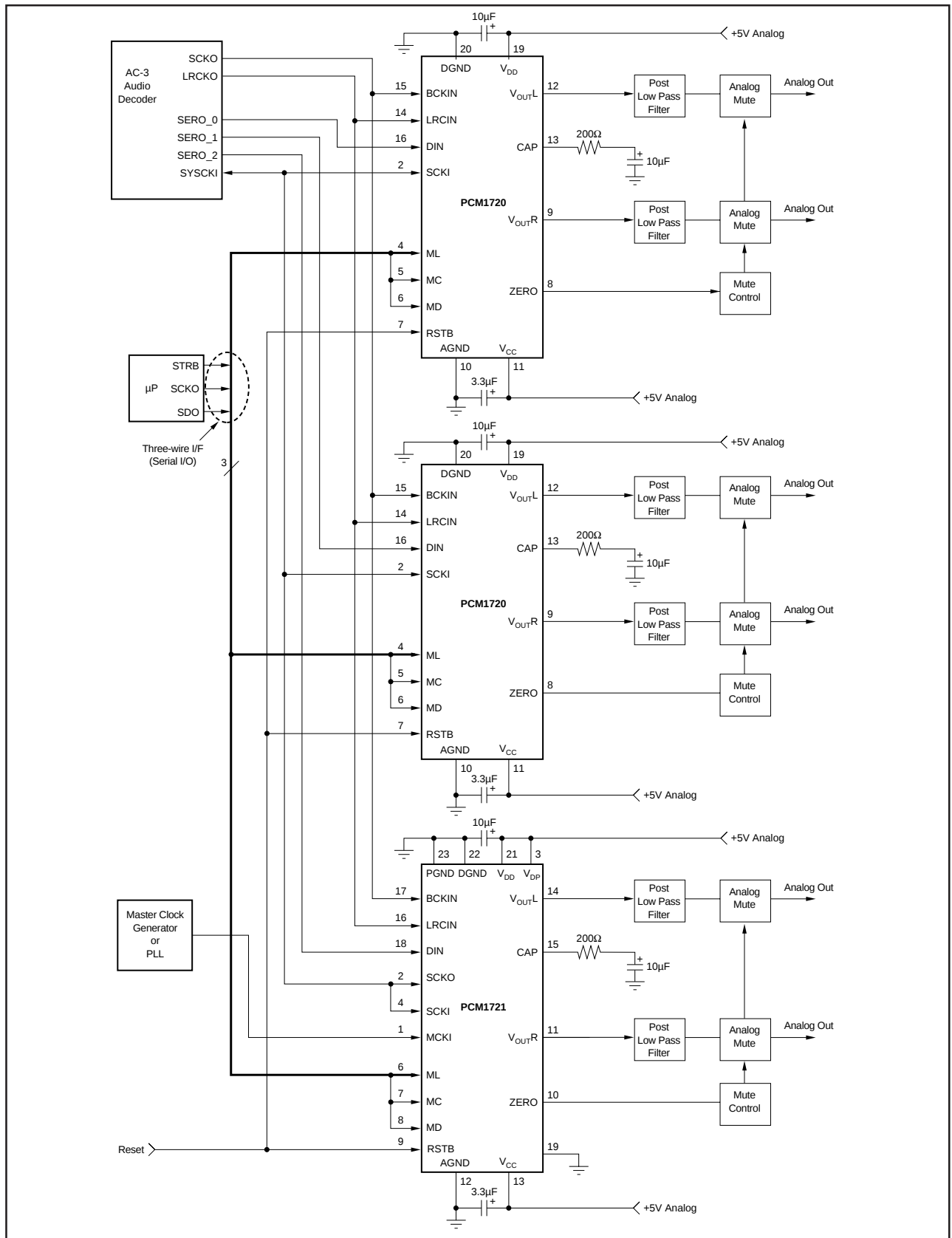


FIGURE 13. Connection Diagram for a 6-Channel AC-3 Application.

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