Fast CMOS 3.3V Octal D Flip-Flop

Product Features

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input can be 3V or 5V
  - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
  Balanced drives (24mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 20-pin 173 mil wide plastic TSSOP (L)
  – 20-pin 150 mil wide plastic QSOP (Q)
  – 20-pin 300 mil wide plastic SOIC (S)

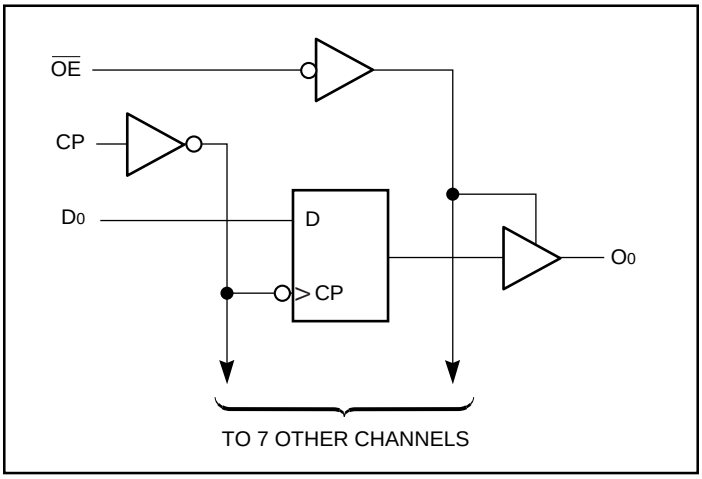
Product Description

Pericom Semiconductor's PI74LPT series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed grades.

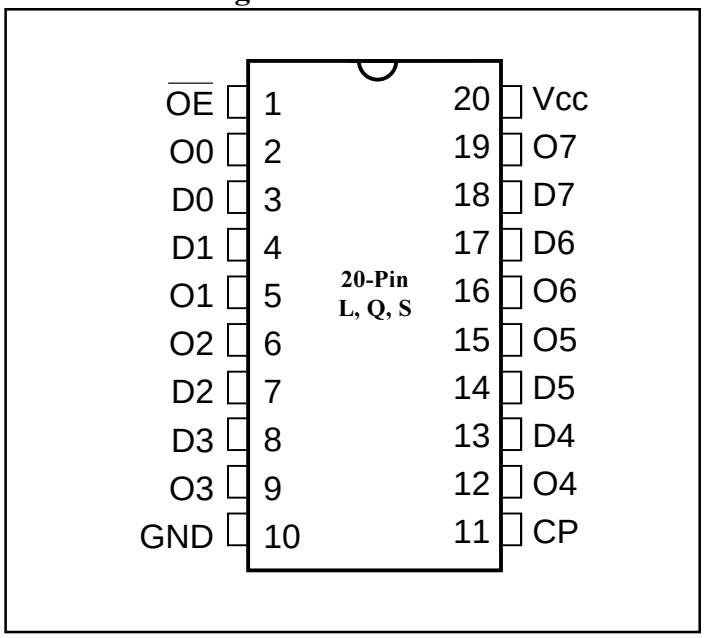
The PI74LPT374 8-bit wide octal resisters designed with eight D-type flip-flops, a buffered common clock, and buffered 3-state outputs. When output enable ($\overline{OE}$) is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The PI74LPT374 can be driven from either 3.3V or 5.0V devices allowing for the device to be used as a translator in a mixed 3.3V/5.0V system.

Logic Block Diagram



Product Pin Configuration



Truth Table[1]

Inputs			Outputs
D_N	CP	$\overline{OE}$	O_N
H	↑	L	H
L	↑	L	L
X	X	H	Z

Note:
1. H = High Voltage Level, X = Don't Care,
   L = Low Voltage Level,
   Z = High Impedance, ↑ LOW-to-HIGH Transition

Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CP	Clock Pulse, LOW-to-HIGH Transition
D7-D0	Data Inputs
O7-O0	3-State Outputs
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) ..... –0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .. –0.5V to +7.0V
DC Input Voltage ..... –0.5V to +7.0V
DC Output Current ..... 120 mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = –40°C$ to $+85°C$, $V_{CC} = 2.7V$ to $3.6V$)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	V
V_{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	$V_{IN} = 5.5V$	—	—	±1	µA
	Input HIGH Current (I/O pins)	V_{CC} = Max.	$V_{IN} = V_{CC}$	—	—	±1	µA
I_{IL}	Input LOW Current (Input pins)	V_{CC} = Max.	V_{IN} = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	V_{CC} = Max.	V_{IN} = GND	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	$V_{OUT} = 5.5V$	—	—	±1	µA
I_{OZL}	(3-State Output pins)	V_{CC} = Max.	V_{OUT} = GND	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., $I_{IN} = –18$ mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	$I_{OH} = –0.1$ mA	V_{CC}-0.2	—	—	V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –3$ mA	2.4	3.0	—	V
		$V_{CC} = 3.0V$,	$I_{OH} = –8$ mA	2.4[5]	3.0	—	V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –24$ mA	2.0	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	$I_{OL} = 0.1$ mA	—	—	0.2	V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16$ mA	—	0.2	0.4	V
			$I_{OL} = 24$ mA	—	0.3	0.5	V
I_{OS}	Short Circuit Current[4]	V_{CC} = Max.[3], V_{OUT} = GND		–60	–85	–240	mA
I_{OFF}	Power Down Disable	$V_{CC} = 0V$, V_{IN} or $V_{OUT} £ 4.5V$		—	—	±100	µA
V_H	Input Hysteresis			—	150	—	mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. $V_{OH} = V_{CC} – 0.6V$ at rated current.

Capacitance ($T_A = 25°C$, f = 1 MHz)

Parameters(1)	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

Note:
1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]		2.0	30	µA
I_{CCD}	Dynamic Power Supply[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open fi = 10 MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND		0.6	2.3	mA
		V_{CC} = Max., Outputs Open fi = 2.5 MHz 50% Duty Cycle $\overline{OE}$ = GND 8 Bits Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND		2.1	4.7[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCV} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range[1]

Parameters	Description	Conditions[2]	LPT374 Com. Min.[3]	LPT374 Com. Max.	LPT374A Com. Min.[3]	LPT374A Com. Max.	LPT374C Com. Min.[3]	LPT374C Com. Max.	Units
F_{MAX}	Maximum Clock Frequency	C_L = 50 pF R_L = 500Ω	150		150		150		MHz
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx		2.0	8.0	2.0	5.5	2.0	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xOx		1.5	8.5	1.5	6.5	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time[4] $x\overline{OE}$ to xOx		1.5	8.5	1.5	5.5	1.5	5.0	ns
t_{SU}	Setup Time HIGH or LOW, xDx to xCLK		2.0		2.0		2.0		ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5		1.5		1.5		ns
t_W	xCLK Pulse Width[4] HIGH		7.0		5.0		5.0		ns
$t_{SK}(o)$	Output Skew[5]			0.5		0.5		0.5	ns

Notes:
1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.