PX4805 - Roshni

Dual OC-48 Framer & ATM/POS Processor

Overview

Roshni PX4805 is a highly integrated, low power Dual OC-48 SONET/SDH physical layer device, which performs Transmission Convergence functionality for ATM and Packet Over SONET (POS). Each independent OC-48 slice provides three modes of operation – a single OC-48 2.4 Gbps stream, a single OC-12 622 Mbps stream, and four 622 Mbps streams multiplexed onto the OC-48 line. Roshni interfaces to the system through a UTOPIA Level 2/3, POS-PHY Level 2/3 interface or Packet Bus Level 3. Two Roshni devices, when interfaced to an external OC-192 framer, can be used to provide an aggregate 9.95 Gbps throughput played out over up to 16 PHY ports. Roshni can also be used as a SONET path terminating multiplexer, terminating into drop-side buses ranging from two STS-48c to eight STS-12c streams. Roshni is implemented in a leading edge 1.5 Volt, 0.14 micron CMOS that yields an industry leading 1.2 Watts per OC-48 stream. Roshni is packaged in a 648-pin TBGA package.

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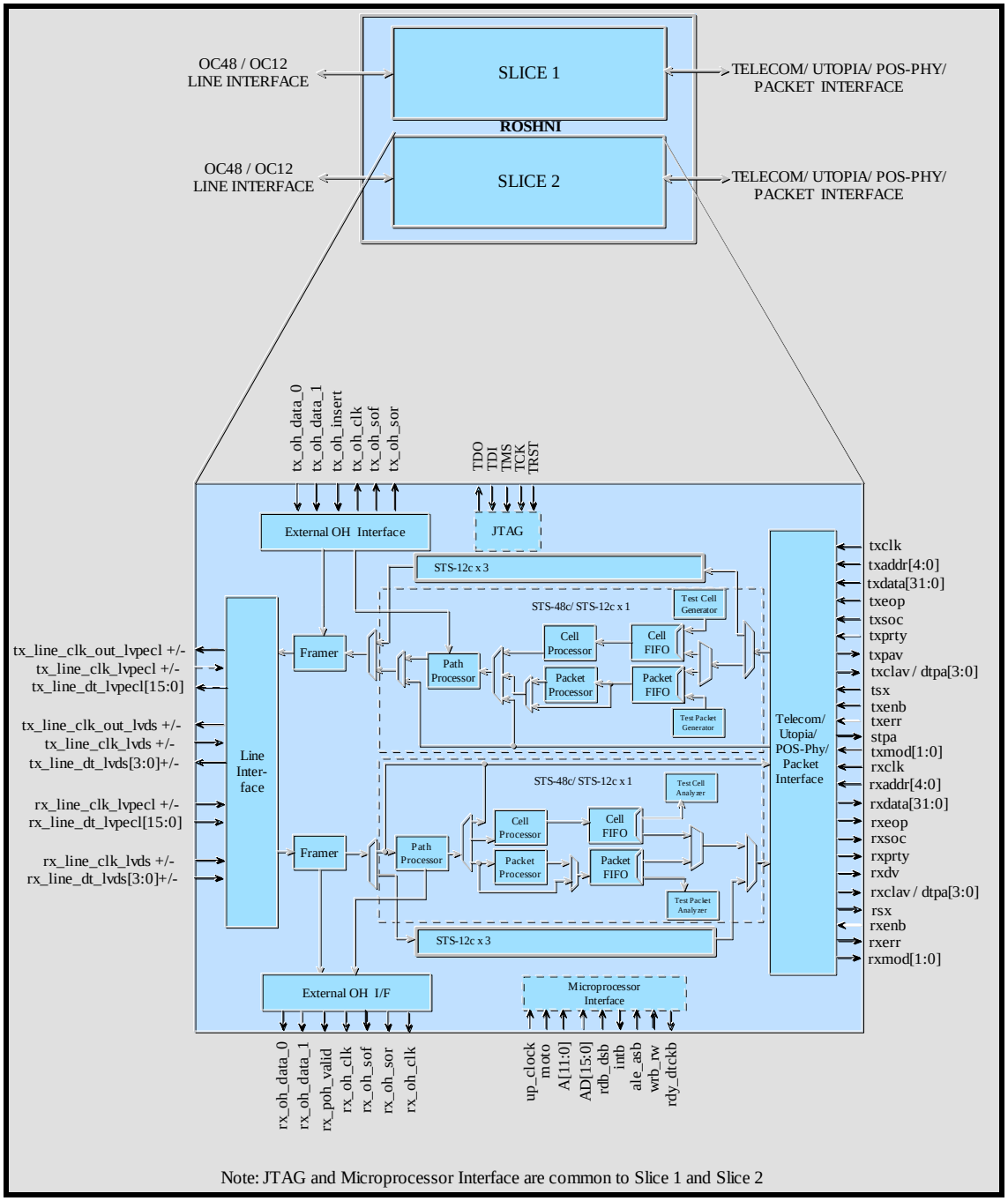

Figure 1: Block Diagram

Block Diagram Description

The *Framer* handles SONET/SDH framing functionality including frame recovery, overhead insertion and extraction, scrambling and de-scrambling and line parity handling. This module handles either STS-48 frames or STS-12 frames.

The *Path Processor* performs pointer extraction and processing, and path overhead processing. This module handles a single STS-48c payload, a single STS-12c payload, or four STS-12c payloads.

The *External OH Interface* provides external access to path, line, and section overheads in both transmit and receive streams.

The *Cell Processor*, in the receive direction, delineates cells, detects and optionally corrects cell header errors, and de-scrambles cell payload. In the transmit direction, it computes and inserts the header error check sequence, handles flow control and scrambles cell payload.

The *Packet Processor* encapsulates data packets into, or extracts packets from, the PPP format specified for SONET links. It analyzes packet headers, and inserts or analyzes the payload FCS. Packet processing can also be bypassed in transparent mode.

The *Packet* and *Cell FIFOs* provide rate-matching buffers between the data on the SONET stream and the user-controlled Utopia and Packet interfaces.

The *Telecom/ Utopia/POS-PHY/Packet interface* provides Utopia Level 3/ Level 2 interface in ATM mode; POS-PHY Level 3/Level 2 interface in POS mode; Packet Bus Level 3 interface in Packet bus mode or Telecom Bus interface in Direct Payload mapping mode. In the Direct payload mapping mode, SONET payload is accepted from or given out through industry standard telecom buses which are multiplexed with the Utopia/Packet interface pins. Each slice supports a single STS-48c telecom bus or up to four STS-12c telecom buses. In this mode, the drop side pins are shared with the Utopia/Packet interface pins and hence this mode is mutually exclusive with the ATM/POS mode.

The *Test Cell/Packet Generator and Analyzer* provide diagnostic and BIST support by inserting test cells or packets into the transmit streams and extracting and analyzing them off the receive streams.

The *Microprocessor Interface* provides a 16-bit microprocessor interface for configuration, control, and status monitoring.

JTAG provides a standard IEEE 1149.1 JTAG test port for boundary scan board test purposes.

Features

SONET/SDH

- Supports 4-bit LVDS Line interface at 622.08 MHz or 16-Bit LVPECL interface at 155.54 MHz in STS-48 mode.
- Supports serial LVDS interface at 622 MHz or 8-bit LVPECL interface at 77.78 MHz in STS-12 mode.
- Performs SONET/ SDH frame generation and recovery.
- Generates/ terminates Section Overhead (SOH), Line Overhead (LOH), and Path Overhead (POH) bytes.
- Detects OOF (Out of Frame), LOF (Loss of Frame), LOS (Loss of Signal), APS byte signal failure, Line/ Path AIS, and Line/ Path RDI conditions on the receive stream.
- Inserts and extracts 16-byte or 64-byte Section Trace (J0) and Path Trace (J1).
- Optional loopback of received frames to the Transmitter providing section-level regenerator Capability.

ATM

- Implements ATM Forum User Network Interface Specifications
- Inserts and extracts ATM cells.
- Scrambles and de-scrambles cell payload, detects and processes header errors.
- Inserts HEC bytes and detects Out of Cell Delineation (OCD) and Loss of Cell Delineation (LCD) on the receive stream
- Extracts OAM cells and user-specified cells
- Performs cell rate adaptation and drops idle cells
- Provides 8-cell deep transmit and receive buffers.

POS

- Implements PPP over SONET/SDH specification according to RFC 2315 and 1662 of the IETF.
- Inserts and extracts POS packets.
- Inserts and detects flag sequences
- Optionally processes address, control, and protocol fields.
- Supports CRC-16 and CRC-32
- Optional transparent mode –no packet processing is performed.
- Provides 4096-byte deep transmit and receive buffers.

Others

- Provides two Local loopbacks – Near end and Far end, and two Remote Loopback – Near end and Far end for diagnostic purposes

Applications

- Packet over SONET Routers and Switches
- ATM switches
- SONET/SDH Terminal Multiplexers and Regenerators

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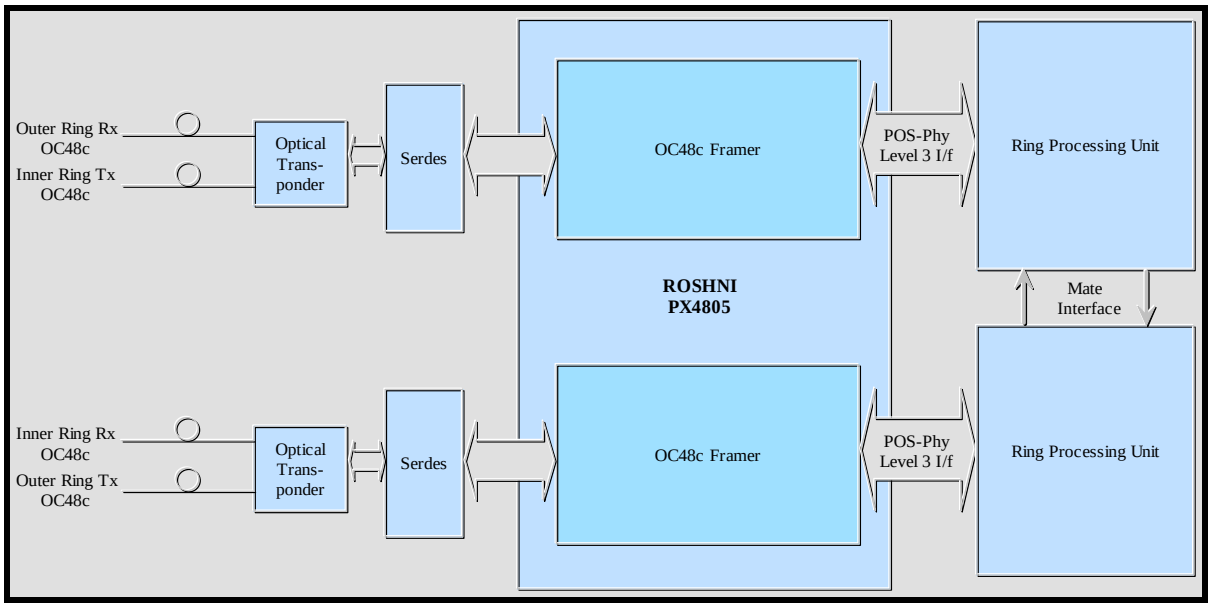
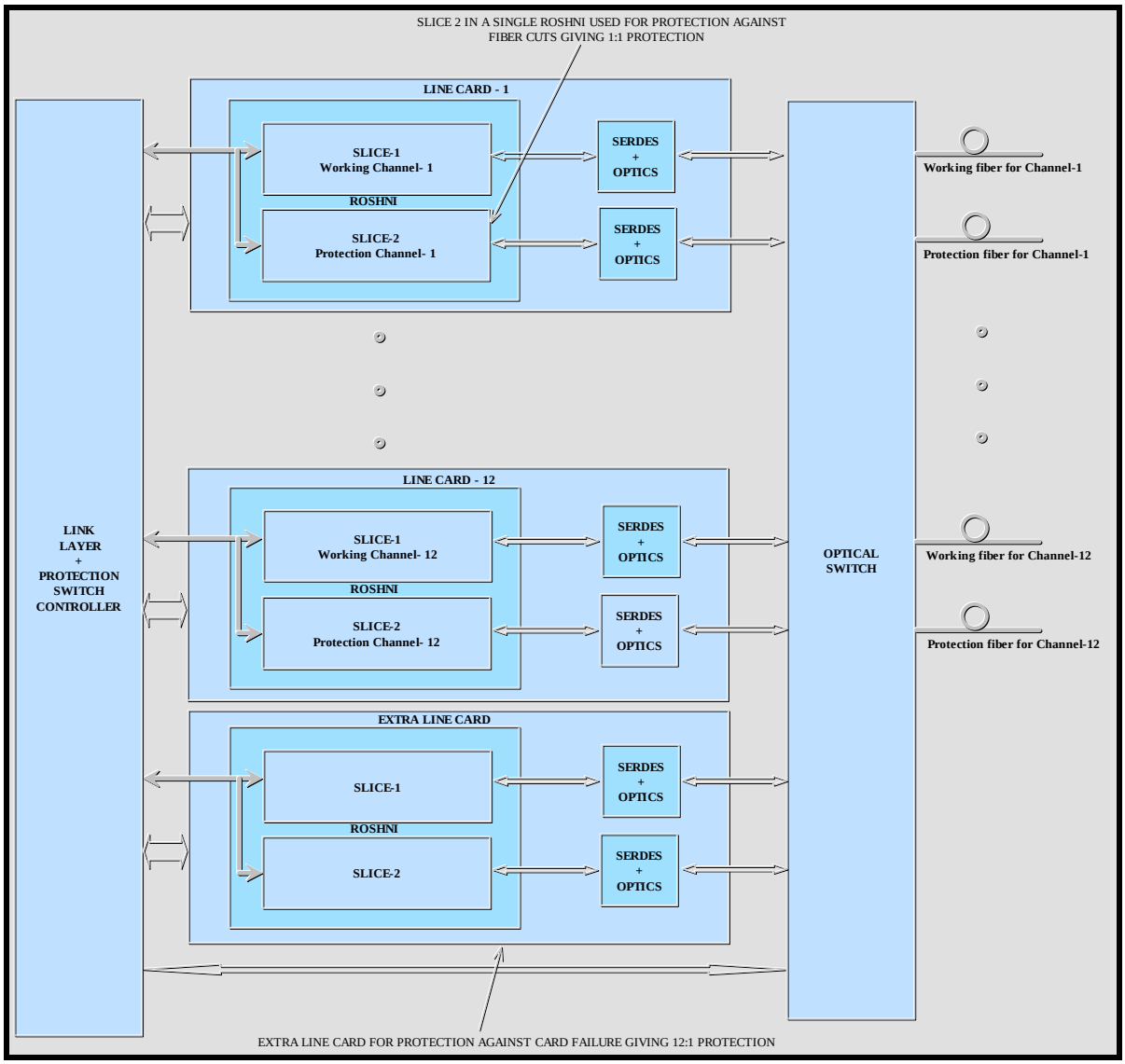
Application Examples

Resilient Packet Ring Network



Fiber Cut and Card Failure Protection Scheme



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