IWE8

Interworking Element for 8 E1/T1 Lines

PXB4219 / PXB4220 / PXB4221 Version 3.x

QuadFALC

Quad E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications

PEB 22554 Version 1.3/2.x

WAN Solutions

Never stop thinking.

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Table of Contents **Page**

1 Overview . . . 1
1.1 IWE8 overview . . . 2
1.2 QuadFALC overview . . . 3

2 Hardware Interface between IWE8 and QuadFALC . . . 4

3 Functional Description . . . 5
3.1 Framing and line interface modes . . . 6
3.1.1 T1 mode . . . 6
3.1.2 E1 mode . . . 6
3.2 Framer Interface Modes . . . 8
3.2.1 FALC Mode (FAM) . . . 8
3.2.2 Generic Interface Mode (GIM) . . . 9
3.3 Interworking Modes . . . 11
3.3.1 AAL Mode . . . 11
3.3.1.1 Unstructured CES Mode . . . 11
3.3.1.2 Structured CES Mode . . . 11
3.3.2 ATM G.804 Mode . . . 12
3.4 IWE8 Framer Transmit Clock Sources . . . 13
3.4.1 FRCLK . . . 13
3.4.2 External Clock . . . 13
3.4.3 Reference Clock / 16 . . . 13
3.4.4 Reference Clock / ICRC in free running mode . . . 13
3.4.5 Clock Recovery: SRTS . . . 13
3.4.6 Clock Recovery ACM . . . 14

4 Register Settings . . . 15
4.1 Initialisation of the IWE8 . . . 16
4.1.1 Basic IWE8 configuration . . . 16
4.1.2 T1 specific settings . . . 16
4.1.3 E1 specific settings . . . 16
4.1.4 FALC mode specific settings . . . 16
4.1.5 GIM mode specific settings . . . 16
4.1.6 Clocking Modes . . . 16
4.1.6.1 FRCLK . . . 16
4.1.6.2 External Clock . . . 17
4.1.6.3 Reference Clock / 16 . . . 17
4.1.6.4 Reference Clock / ICRC in free running mode . . . 17
4.1.6.5 Clock Recovery: SRTS . . . 18
4.1.6.6 Clock Recovery ACM . . . 18
4.2 Initialisation of the QuadFALC . . . 19
4.2.1 Basic QuadFALC configuration . . . 20
4.2.2 Basic T1 configuration . . . 22
4.2.3 T1 FALC modes . . . 23

4.2.3.1 T1 FAM Multiframe based structured CES 24
4.2.3.2 T1 FAM Unstructured CES 25
4.2.3.3 T1 FAM ATM G.804 service 26
4.2.4 T1 GIM modes 27
4.2.4.1 T1 GIM Multiframe based structured CES 28
4.2.4.2 T1 GIM Unstructured CES 29
4.2.4.3 T1 GIM ATM G.804 service 30
4.2.5 Basic E1 configuration 30
4.2.6 E1 FALC modes 32
4.2.6.1 E1 FAM Multiframe based structured CES 33
4.2.6.2 E1 FAM Unstructured CES 34
4.2.6.3 E1 FAM ATM G.804 service 35
4.2.7 E1 GIM modes 36
4.2.7.1 E1 GIM Multiframe based structured CES 37
4.2.7.2 E1 GIM Unstructured CES 38
4.2.7.3 E1 GIM ATM G.804 service 39

List of Figures **Page**

Figure 1 Basic connection between one IWE8 and one QuadFALC channel . . . 4
Figure 2 IWE8 framer interface in FALC mode . . . 9
Figure 3 IWE8 framer interface in T1 GIM mode . . . 10
Figure 4 IWE8 framer interface in E1 GIM mode . . . 10
Figure 5 T1 FALC structured CES . . . 24
Figure 6 T1 FALC unstructured CES . . . 25
Figure 7 T1 FALC ATM . . . 26
Figure 8 T1 GIM structured CES . . . 28
Figure 9 T1 GIM unstructured CES . . . 29
Figure 10 T1 GIM ATM . . . 30
Figure 11 E1 FALC structured CES . . . 33
Figure 12 E1 FALC unstructured CES . . . 34
Figure 13 E1 FALC ATM . . . 35
Figure 14 E1 GIM structured CES . . . 37
Figure 15 E1 GIM unstructured CES . . . 38
Figure 16 E1 GIM ATM . . . 39

List of Tables **Page**

Table 1 Basic QuadFALC configuration 20
Table 2 Basic T1 configuration of the QuadFALC 22
Table 3 T1 FALC mode specific QuadFALC configuration 23
Table 4 T1 FALC structured CES specific QuadFALC configuration 24
Table 5 T1 FALC unstructured CES specific QuadFALC configuration 25
Table 6 T1 FALC ATM specific QuadFALC configuration 26
Table 7 T1 GIM mode specific QuadFALC configuration 27
Table 8 T1 GIM structured specific QuadFALC configuration 28
Table 9 T1 GIM unstructured CES specific QuadFALC configuration 29
Table 10 T1 GIM ATM specific QuadFALC configuration 30
Table 11 Basic E1 configuration of the QuadFALC 31
Table 12 E1 FALC mode specific QuadFALC configuration 32
Table 13 E1 FALC structured CES specific QuadFALC configuration 33
Table 14 E1 FALC unstructured CES specific QuadFALC configuration 34
Table 15 E1 FALC ATM specific QuadFALC configuration 35
Table 16 E1 GIM mode specific QuadFALC configuration 36
Table 17 E1 GIM structured CES specific QuadFALC configuration 37
Table 18 E1 GIM unstructured CES specific QuadFALC configuration 38
Table 19 E1 GIM ATM specific QuadFALC configuration 39

1 Overview

This Application Note describes how to connect the Infineon Interworking Element for 8 E1/T1 Lines, IWE8 (PXB4219 / PXB4220 / PXB4221) to the Infineon Quad E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications, QuadFALC (PEB 22554).

As these devices are very flexible, there are several different operational modes for the interworking between the two ICs. This document also aims to help a designer decide which mode is best suited for the desired application and support how to set the registers correctly for the chosen mode.

Chapter 2 shows the hardware connection between IWE8 and QuadFALC which doesn't differ very much for the different modes of interworking. To keep your hardware design flexible, it is recommended to connect all in Figure 1 mentioned pins of the devices. Chapter three gives an overview over the dedicated operational modes and explains the differences and gives recommendations. In chapter four, register settings are described.

1.1 IWE8 overview

The Interworking Element for 8 E1/T1 Lines PXB4219 / PXB4220 / PXB4221 (IWE8) is a member of Infineon's ATM chip set. Together with framing and line interface components (e.g. Infineon's QuadFALC PEB 22554) the IWE8 serves as a gateway between Asynchronous Transfer Mode (ATM) networks and timeslot based PDH networks.

The IWE8 can operate in two functional modes, either in ATM mode to perform cell mapping into PDH frames according to ITU-T specification G.804 or in AAL mode. A port that is configured in AAL mode offers ATM Forum compliant circuit emulation services as defined in ITU-T specification I.361.1. For Unstructured T1/E1 Circuit Emulation Service (CES) the ATM adaptation layer type 1 (AAL1) with Unstructured Data Transfer (UDT) as defined in ITU-T I363.1 is used. The use of partial filled cells is possible. For clock recovery the IWE8 supports Synchronous Residual Time Stamp (SRTS) method and Adaptive Clock Method (ACM). The Structured Circuit Emulation Service is intended to carry N of the 24 (T1) or 32 (E1) timeslots across the ATM network.

Each of the 8 E1 or T1 input and output ports can be configured independently to operate in one of this two basic modes.

1.2 QuadFALC overview

The QuadFALC framer and line interface component is designed to fulfill all required interfacing between four analog E1/T1/J1 lines and the digital PCM system highway, H.100/H.110 or H-MVIP bus for world market telecommunication systems.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards. An integrated signaling controller including Signaling System #7 support reduces software overhead.

Crystal-less jitter attenuation with only one master clock source reduces the amount of required external components.

Equipped with a flexible microprocessor interface, it connects to any control processor environment. A standard boundary scan interface is provided to support board level testing. Flat pack device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

Other members of the FALC® family are the FALC®54 for short haul applications, the FALC®-LH for long haul and short haul applications as well as the FALC®56 supporting three HDLC channels on one single chip.

2 Hardware Interface between IWE8 and QuadFALC

The electrical connections to be made between these two devices are more or less fixed for the different operational modes.

The wiring for one single IWE-FALC connection is suggested as shown in **Figure 1**. Using this connection all different framer (T1/E1), system interface (FALC/GIM) and port modes (structured/unstructured/ATM) supported by both devices can be configured using software and is described in **Chapter 4** of this document.

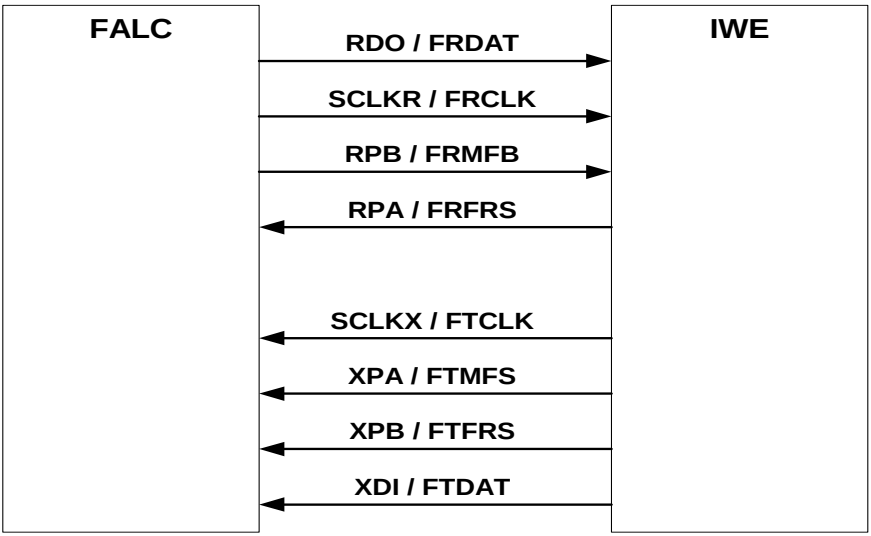

Figure 1 Basic connection between one IWE8 and one QuadFALC channel

3 Functional Description

When connecting the Infineon devices IWE8 and QuadFALC to each other, two different framer interface modes can be selected, the FALC Mode (FAM) and the Generic Interface Mode (GIM). Generally, the FALC mode can only be used between the Infineon Interworking Element IWE8 and the Infineon framer (FALC) family. When using the IWE8 alongside other framer devices, GIM has to be selected.

Although GIM can be used interfacing IWE8 and QuadFALC, FAM is recommended. While in GIM the clock frequency is equal to the data rate, the clock frequency in FALC mode is four times higher than the data rate which makes the system more stable. Additionally, in FALC mode the same clock frequency is used for E1 and T1. This may be an advantage in systems that can operate either in E1 or in T1 mode (SW configurable).

The IWE8 interface modes SYM8 and SYM2 are of minor importance and will not be covered by this document.

When designing a system, some thoughts have to be spend on the clocking concept. In the receive path the QuadFALC recovers the clock from the line and provides it as the receive clock to the IWE8.

In the transmit path, between several possible clock sources can be chosen. The clock can be generated by the IWE8, the receive clock of the dedicated port or an external clock can be used. In order not to get slips, the transmit clock has to be chosen carefully. Please refer to chapter 3.4 for detailed information about the different clocking modes of the IWE8.

3.1 Framing and line interface modes

Both IWE8 and QuadFALC are able to operate in both primary multiplex modes T1 and E1.

The IWE8 is configured via the external pin “E1/$\overline{T1}$” in either of these modes while the QuadFALC can be programmed via software. The device can not be hotswitched while operation.

3.1.1 T1 mode

PCM line bit rate	:	1.544 Mbit/s
Single frame length	:	193 bit, No. 1…193
Framing frequency	:	8 kHz
Organization	:	24 time slots, No. 1…24 with 8 bits each, No. 1…8 and one preceding F-bit

Summary of T1 Framing Modes:

F4	:	4-frame multiframe
F12	:	12-frame multiframe (D4)
ESF	:	Extended Superframe (F24)
F72	:	72-frame multiframe (SLC96)

The IWE8 only supports the 12-frame multiframe (D4) and the Extended Superframe (F24) framing mode (see **Chapter 4.1**).

The operating mode of the QuadFALC is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme (see **Chapter 4.2**).

The QuadFALC implements all of the standard and/or common framing structures PCM24 (T1/J1, 1.544 Mbit/s) carriers. The internal HDLC controller supports all signaling procedures including signaling frame synchronization/synthesis in all framing formats.

3.1.2 E1 mode

PCM line bit rate	:	2.048 Mbit/s
Single frame length	:	256 bit, No. 1…256
Framing frequency	:	8 kHz
HDLC controller	:	nx64 kbit/s, n = 1...32 or n×4 kbit/s, n = 1...5
Organization	:	32 time slots, No. 0…31 with 8 bits each, No. 1…8

Summary of E1 Framing Modes

- Doubleframe format according to ITU-T G. 704
- Multiframe format according to ITU-T G. 704
- CRC4 processing according to ITU-T G. 706
- Multiframe format with CRC4 to non CRC4 interworking according to ITU-T G. 706
- Multiframe format with modified CRC4 to non CRC4 interworking
- Multiframe format with CRC4 performance monitoring

In the IWE8 only Doubleframe format or Multiframe format can be chosen (see **Chapter 4.1**).

The operating mode of the QuadFALC is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme (see **Chapter 4.2**).

The QuadFALC implements all of the standard framing structures for E1 or PCM 30 (CEPT, 2.048 Mbit/s) carriers. The internal HDLC or CAS controller supports all signaling procedures including signaling frame synchronization/synthesis and signaling alarm detection in all framing formats. The time slot assignment from the PCM line to the system highway and vice versa is performed without any changes of numbering (TS0 ↔ TS0, …, TS31 ↔ TS31).

3.2 Framer Interface Modes

The IWE8 can be operated in four different interface modes, FAM, GIM, SYM2 and SYM8. SYM2 and SYM8 have only historical meaning, therefore only FAM and GIM are described in this Application Note. The interface mode is selected with the “om” bits in the “opmo” register of the IWE8.

The QuadFALC offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked by pin SCLKR, while the interface to the transmit system highway is independently clocked by pin SCLKX. The frequency of these working clocks and the data rate of 2.048/4.096/8.192/16.384/ 1.544/3.088/6.192/12.352 Mbit/s for the receive and transmit system interface is programmable by FALC-SIC1.SSC1/0, FALC-SIC2.SSC2 and FALC-SIC1.SSD1, FALC-FMR1.SSD0.

3.2.1 FALC Mode (FAM)

The receive system clock and transmit system clock are both 8.192 MHz, and may be independent from each other. The datarate is 2.048 Mbit/s. This means that each bit lasts for 4 clock cycles.

Data on the system internal highway is structured in frames of 256 bits every 125 µs. It is transmitted in 32 slots numbered from 0 to 31 with slot 0 transmitted first. The data bits of a slot are numbered from 1 to 8. The first transmitted bit ‘bit 1’ is the most significant bit. **Figure 2** shows the bit ordering.

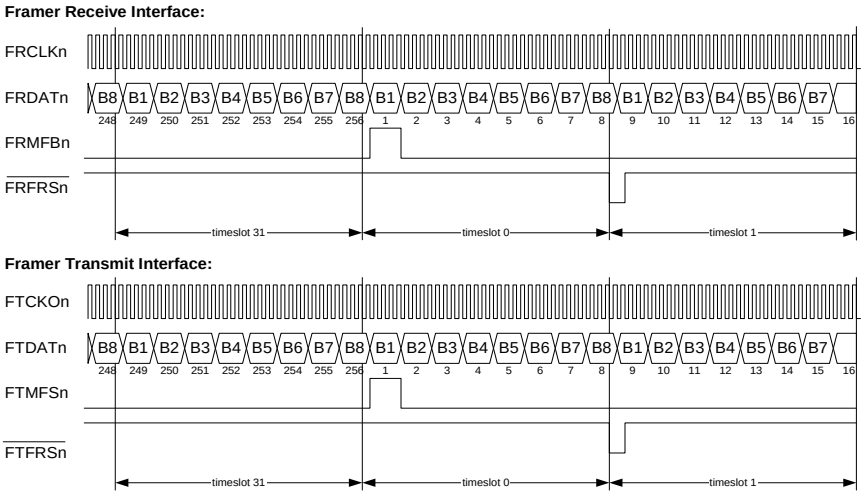

Figure 2 IWE8 framer interface in FALC mode

In T1 mode (IWE8-Pin E1/$\overline{T1}$ = 0) there is one F-channel carrying the F-bit (Frame Alignement Signal/Data Link (FS/DL)) and 24 data channels numbered from 0 to 23. These channels are mapped into the 32 frame slots, wich means that some frame slots are unused (see IWE8 V3.x Data Sheet chapter 4.11).

In E1 mode (IWE8-Pin E1/$\overline{T1}$ = 1) there are 32 channels numbered from 0 to 31. The channels are directly mapped into the corresponding 32 frame slots.

3.2.2 Generic Interface Mode (GIM)

The Generic Interface Mode (GIM) makes the framer interface more universal, so that other framer/line interface units or T1/E1 transceivers can be connected directly to the IWE8. Depending on the IWE8-E1/$\overline{T1}$ pin, the interface can be adapted to line bit rates of 1.544 MHz (T1 rate) or 2.048 MHz (E1 rate). The mode is enabled by setting IWE8 bit om = 01_B in “opmo” (FALC mode is default). Make sure that no clocks are applied to the transmitter when switching to GIM. **Figure 3** and **Figure 4** show the alignement of the bits and frame syncs to each other.

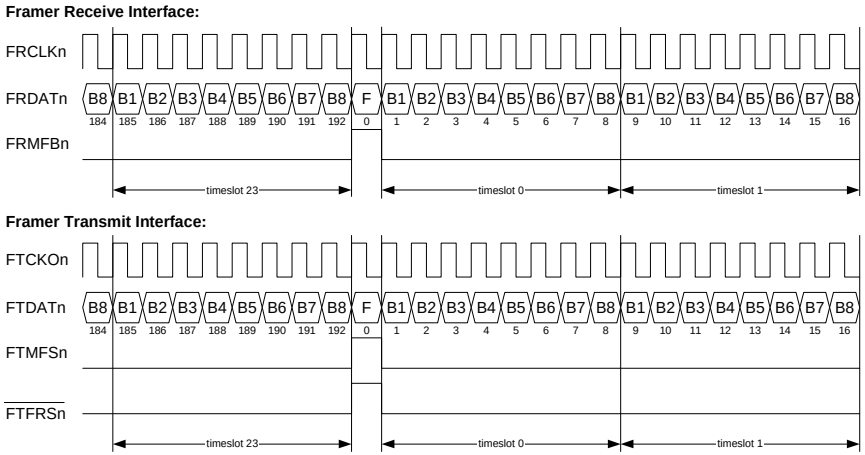

Figure 3 IWE8 framer interface in T1 GIM mode

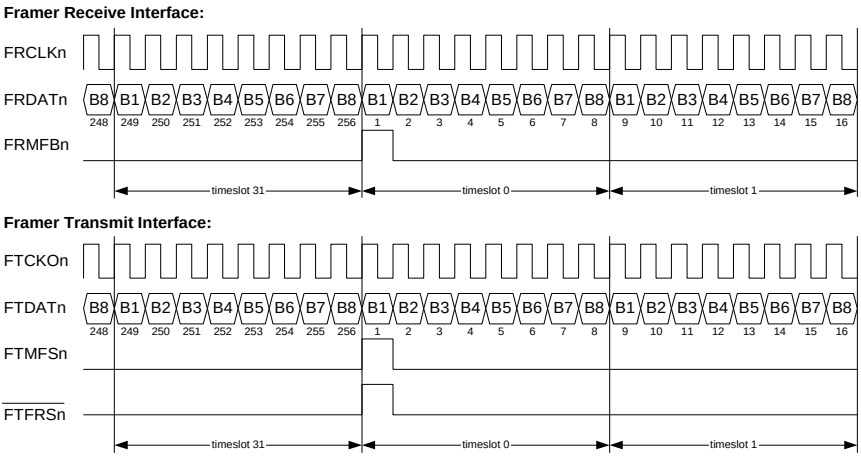

Figure 4 IWE8 framer interface in E1 GIM mode

3.3 Interworking Modes

3.3.1 AAL Mode

A port that is configured to AAL mode offers ATM Forum compliant circuit emulation services via AAL1 as defined in ITU-T I.361.1. A port N can be configured to AAL mode via “p_atm” in register “pcfN” of the IWE8.

Some features of the AAL mode are controlled by the internal registers “acfg”, “caal”, “bp32”, “bp10” and “cfil”. The features controlled by these registers are common to all AAL ports.

Some features of the AAL mode can be controlled per port, by programming the port configuration registers “pcfN”.

Some features of the AAL mode can be controlled per channel, by programming the channel specific “AAL Reference Slot” in the internal configuration RAM’s (RAM1 for receive ports, RAM2, RAM3 and RAM4 for transmit ports).

3.3.1.1 Unstructured CES Mode

A 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1) bitstream is packed into ATM cells without any framing. No alignment between octets in E1 or T1 frames and octets in the ATM cells is done.

For this Unstructured T1/E1 Circuit Emulation Service (CES) the ATM adaptation layer type 1(AAL1) with Unstructured Data Transfer (UDT) as defined in ITU-T I.363.1 is used. The use of partially filled cells is possible.

For clock recovery the IWE8 supports the Synchronous Residual Time Stamp (SRTS) method and Adaptive Clock Method (ACM).

- SRTS is possible on channels with completely filled cells
- ACM can be used on both, channels with partially and completely filled cells

A port is programmed to unstructured CES via “p_ces” in the Port Configuration Register “pcfN”.

Per port a Segmentation Buffer with a maximum size of 16 cells and a Reassembly Buffer with a maximum size of 256 cells is implemented in external RAM.

3.3.1.2 Structured CES Mode

A port is programmed for the Structured T1/E1 Nx64 kbit/s Basic Service (Structured CES) via the port configuration register “pcfN” (“p_ces” = 0).

The structured circuit emulation service is intended to carry N of the 24 (T1) or 32 (E1) timeslots across the ATM network.

An emulated Nx64 kbit/s circuit will be referred to as a channel throughout this document. It is possible that several channels share the same physical interface port.

In structured CES mode neither SRTS nor ACM clock recovery is possible.

3.3.2 ATM G.804 Mode

ATM mode ports operate as an ATM User Network Interface (UNI) at 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1).

The device supports mapping of ATM cells in T1/E1 frames according to ITU-T G.804, “ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)” and ATM Forum, “ATM on Fractional E1/T1”.

It implements all Transmission Convergence (TC) sublayer functions of the Physical Layer (PHY) defined in ITU-T I.432, “B-ISDN User-network Interface - Physical layer Specification”

3.4 IWE8 Framer Transmit Clock Sources

The following clock sources can be chosen to be the framer transmit clock. Chapter 8.1 of the IWE8 V3.x Data Sheet also gives a good overview over the IWE8 clocking concept.

3.4.1 FRCLK

IWE8 uses the framer receive clock of the corresponding port as transmit clock. Pin FTCKO is output.

3.4.2 External Clock

FTCKO is an input and an external clock has to be applied.

This external clock could either be derived from an external clock recovery circuit or could just come out of a given fixed clock. In E1 GIM a 2.048 MHz, in T1 GIM a 1.544 MHz and in FALC mode a 8.192 MHz clock has to be provided.

3.4.3 Reference Clock / 16

The clock applied to RFCLK is divided by 16 and used as framer transmit clock. Pin FTCKO is output.

This mode is only for GIM mode. The clocks that have to be applied to RFCLK have to be different for E1 and T1 operation. For E1 GIM RFCLK has to get a 32.768 MHz clock and for T1 GIM RFCLK needs an external 24.704 MHz clock.

3.4.4 Reference Clock / ICRC in free running mode

The clock applied to RFCLK is modified by the internal clock recovery circuit of the IWE8 to generate an appropriate framer transmit clock. Pin FTCKO is output.

This is a very special mode of the IWE8. The built in clock recovery circuit is used to generate the appropriate framer transmit clock out of a 32.768 MHz clock which has to be applied to RFCLK for FALC mode and E1 GIM. In T1 GIM a 24.704 MHz clock needs to be applied to RFCLK. SRTS as well as ACM are disabled. Depending on the selected framer mode the correct framer transmit clock will be generated. For E1 GIM FTCKO will be 2.048 MHz, for T1 GIM FTCKO will be 1.544 MHz and for the FALC mode FTCKO will be 8.192 MHz (GIM and FALC mode).

In systems where a very accurate 32.768 MHz clock is available and shall be used as a reference for all transmit clocks, this mode shall be used in FALC mode.

3.4.5 Clock Recovery: SRTS

IWE8 generates a recovered clock. Pin FTCKO is output.

When doing unstructured Circuit Emulation Service (unstructured CES), the transmit clock can be recovered using additional information out of the ATM cell stream. SRTS is one method to take care of this issue. When using SRTS, a 51.84 MHz clock has to be applied to IWE8 pin CLK52 and a 32.768 MHz clock to IWE8 pin RFCLK.

Please note that a patent fee has to be paid to Telcordia (former Bellcore) when using SRTS. Please refer to IWE8 data sheet for contact.

For customers who do not want to use the built-in SRTS mechanism, Infineon provides a special version of the IWE8. The name of this device is PXB4221 and covers the same functionality (pin and register compatible) like the PXB4220. SRTS is physically and permanently disabled, so that no patent fees have to be paid.

3.4.6 Clock Recovery ACM

IWE8 generates a recovered clock. Pin FTCKO is output.

When doing unstructured Circuit Emulation Service (unstructured CES), the transmit clock can be recovered using additional information out of the ATM cell stream. ACM is one method to take care of this issue. When using ACM, a 32.768 MHz clock has to be applied to IWE8 pin RFCLK.

4 Register Settings

In the following section you will find the necessary connections between one IWE8 and one FALC for different modes. Unused or unsupported connections or signals are marked grey. All connection recommendations are derived from **Figure 1** which can be used for all supported modes. The only difference are the register settings of the single interfaces which are described in this chapter in detail.

4.1 Initialisation of the IWE8

If the IWE8 operates in E1 mode, the pin E1/$\overline{T1}$ has to be tied to high TTL signal. For T1 operation pin E1/$\overline{T1}$ has to be tied to ground.

4.1.1 Basic IWE8 configuration

When configuring the IWE8, the decision has to be made whether the framer interface of the IWE8 runs in FALC mode or in GIM. FALC mode is the default selection after reset, for GIM the “om” bit in the “opmo” register has to be changed. **Make sure that no clocks are applied to the transmitter when switching to GIM**.

Concerning the configuration of the dedicated RAM slots of the IWE8 in the different modes, please refer to IWE8 V3.x Data Sheet chapter 4.11

4.1.2 T1 specific settings

IWE8 register pcfN bit p_tx_mfs: 0 for T1 Superframe mode

IWE8 register pcfN bit p_tx_mfs: 1 for T1 Extended Superframe mode

4.1.3 E1 specific settings

IWE8 register pcfN bit p_tx_mfs: 0 for E1 Doubleframe mode

IWE8 register pcfN bit p_tx_mfs: 1 for E1 CRC Multiframe mode

4.1.4 FALC mode specific settings

IWE8 register opmo bits om: 00

4.1.5 GIM mode specific settings

IWE8 register opmo bits om: 01

IWE8 register opmo bit frri: 1

IWE8 register opmo bit ftri: 0

IWE8 register opmo bit rfpp: 1

IWE8 register opmo bit rtpp: 1

4.1.6 Clocking Modes

4.1.6.1 FRCLK

IWE8 uses the framer receive clock of the corresponding port as transmit clock. Pin FTCKO is output.

IWE8 register opmo bit rts_eval: 1

IWE8 register ftcs bits ftckN: 01

4.1.6.2 External Clock

FTCKO is an input and an external clock has to be applied. In E1 GIM 2.048 MHz, in T1 GIM 1.544 MHz and in FALC mode 8.192 MHz have to be provided.

IWE8 register opmo bit rts_eval: 0

IWE8 register ftcs bits ftckN: 00

4.1.6.3 Reference Clock / 16

The clock applied to RFCLK is divided by 16 and used as framer transmit clock. Pin FTCKO is output.

This mode is only for GIM mode. The clocks that have to be applied to RFCLK have to be different for E1 and T1 operation. For E1 GIM RFCLK has to get a 32.768 MHz clock and for T1 GIM RFCLK needs an external 24.704 MHz clock.

IWE8 register opmo bit rts_eval: 1

IWE8 register ftcs bits ftckN: 10

4.1.6.4 Reference Clock / ICRC in free running mode

The clock applied to RFCLK is modified by the internal clock recovery circuit of the IWE8 to generate an appropriate framer transmit clock. Pin FTCKO is output.

Depending on the selected framer mode the correct framer transmit clock will be generated. For FALC mode and E1 GIM a 32.768 MHz clock has to be applied to RFCLK, for T1 GIM a 24.704 MHz is necessary.

IWE8 register ftcs bits ftckN:00

IWE8 register opmo bit rts_eval: 1

IWE8 register icrcconf bit gim: 0 for FALC mode and 1 for GIM mode

IWE8 register icrcconf bit ds1: 0 for E1 and 1 for T1 operation

IWE8 register icrcconf bit pdcri: 0

IWE8 register condN bit pwd: 0

IWE8 register condN bit srt: 0

IWE8 register condN bit acm: 0

4.1.6.5 Clock Recovery: SRTS

IWE8 generates a recovered clock. Pin FTCKO is output.

When using SRTS, a 51.84 MHz clock has to be applied to IWE8 pin CLK52 and a 32.768 MHz clock to IWE8 pin RFCLK.

IWE8 register ftcs bits ftckN:00

IWE8 register opmo bit rts_eval: 1

IWE8 register icrcconf bit gim: 0 for FALC mode and 1 for GIM mode

IWE8 register icrcconf bit ds1: 0 for E1 and 1 for T1 operation

IWE8 register icrcconf bit pdcri: 0

IWE8 register condN bit pwd: 0

IWE8 register condN bit srt: 1

4.1.6.6 Clock Recovery ACM

IWE8 generates a recovered clock. Pin FTCKO is output.

When using ACM, a 32.768 MHz clock has to be applied to IWE8 pin RFCLK.

IWE8 register ftcs bits ftckN:00

IWE8 register opmo bit rts_eval: 1

IWE8 register icrcconf bit gim: 0 for FALC mode and 1 for GIM mode

IWE8 register icrcconf bit ds1: 0 for E1 and 1 for T1 operation

IWE8 register icrcconf bit pdcri: 0

IWE8 register condN bit pwd: 0

IWE8 register condN bit acm: 1

4.2 Initialisation of the QuadFALC

The QuadFALC needs a free running master clock for proper operation between 1.02 MHz and 20.00 MHz. The provided frequency must be programmed via GCM1..6 (QuadFALC V1.x) or GCM1..8 (QuadFALC V2.x) registers. In many applications a derived STM1/OC-3 clock is available on board so that this clock can be used directly for the QuadFALC master clock (MCLK). If MCLK is 19.44 MHz the following QuadFALC register setting has to be done:

QuadFALC V1.x

– GCM1 = 0x54
– GCM2 = 0x51
– GCM3 = 0x31
– GCM4 = 0x8F
– GCM5 = 0x0B
– GCM6 = 0x14

QuadFALC V2.x

– GCM1 = 0xD6
– GCM2 = 0x1F
– GCM3 = 0x99
– GCM4 = 0x02
– GCM5 = 0x0B
– GCM6 = 0x2A
– GCM7 = 0xB8
– GCM8 = 0xAB

If a different master clock frequency is used Infineon Technologies provides a software tool called 'Master Clock Frequency Calculator' where the correct register setting for the GCM registers is automatically calculated.

The QuadFALC provides four multifunction ports for transmit and four multifunction ports for receive direction per channel where different input / output functions (e.g. frame sync. or maker) can be performed.

All multifunction ports for transmit and receive direction are bidirectional. After RESET these ports are configured as inputs ($\overline{\text{SYPX}}$, $\overline{\text{SYPR}}$). With the selection of the pin function in registers PC1...4 the input / output functions for transmit and receive direction are achieved.

The receive input multifunction port $\overline{\text{SYPR}}$ can only be selected once, it should not be selected twice or more. Because of the offset programing the $\overline{\text{SYPR}}$ and RFM pin function can not be selected in parallel.

Each of the four different transmit input functions (SYPX, XMFS, TCLK, XSIG) may only be selected once. **No input function should be selected twice or more. SYPX and XMFS should not be selected in parallel**.

However for the connection of the QuadFALC to the IWE8 five programmable pins of each QuadFALC channel are used. For proper operation following relationship has to be fulfilled (see **Figure 1**):

– QuadFALC pin RPA has the function SYPR (Synchronous Pulse Receive; input).
– QuadFALC pin RPB has the function RMFB (Receive Multiframe Begin; output).
– QuadFALC pin RPC has the function FREEZ (Freeze Signaling; output).
– QuadFALC pin XPA has the function XMFS (Transmit Multiframe Synchronization; input) in case the IWE8 provides the Multiframe Sync Pulse.
– QuadFALC pin XPB has the function SYPX (Synchronous Pulse Transmit; input) in case the IWE8 provides the Frame Sync. Pulse only (and not the Multiframe sync. Pulse).

Because using SYPX and XMFS multifunction port configuration of the QuadFALC in parallel is not allowed the non-used pin function should be configured to TCLK function and CMR1.DXSS is reset. With these configuration XPA (reserved for XMFS) and XPB (reserved for SYPX) can be connected to the IWE8 but depending on the IWE8 configuration only Frame Sync. or Multiframe sync. input can be used.

All unused multifunction ports for transmit and receive direction have to be configured to a defined output function because the RESET value is not recommended. Recommended for unused multifunction QuadFALC pins is pin function RSIGM (RPC2..0 = 011) for receive direction and XSIGM (XPC2..0 = 101) for transmit direction.

Note: All these recommendations result in the following detailed configuration recommendation for several modes.
Not mentioned registers have to be set to (or left in) their reset condition for proper operation.

4.2.1 Basic QuadFALC configuration

The basic configuration of the QuadFALC consists of setting the modes of some hardware pins and selection of the external supplied MCLK clock frequency.

For calculation of the right GCM-Register values please use the 'flexible master clock calculator' supplied by Infineon Technologies.

Table 1 Basic QuadFALC configuration

Registers	Values
GPC1	0x60[1)]
IPC	0x01[2)]

GCR	0x40
GCM1..6 or 1..8[3)]	according to flexible master clocking calculator program.

1) Dependend on the desired PIN function of SEC/FSC and RCLK1

2) Dependend on the disired PIN functions of SYNC and INT

3) QuadFALC v2.x has two additional global clocking registers

4.2.2 Basic T1 configuration

The basic T1 configuration consists of defining unused multifunction port signals, clock routing, line interface mode, puls shape, interrupt usage and alarm handling.

The framer is programmed for extended super framing. The line interface generates standard T1 pulses with B8ZS line coding.

Table 2 Basic T1 configuration of the QuadFALC

Registers	Values
PC3	0x56
PC4	0x35
CMR1	n * 0x40 (n = 0..3; Channel)
LIM0	0x01 (Master); 0x00 (Slave)
LIM1	0x30
LIM2	0x01
RC1	0x24
XPM0	0xD7
XPM1	0x22
XPM2	0x01
FMR0	0xF0
FMR1	0x18
FMR4	0x0E
IMR0	0xFD[1)]
IMR2	0x03[1)]
IMR3	0x3F[1)]
IMR4	0xFF[1)]
ESM	0x04[1)]
PCD	0x0A
PCR	0x15
CCB1..3	0xFF[2)]

1) Dependent or the interrupts to react on. This is a recommendation only

2) CAS data will not be inserted by the FALC

4.2.3 T1 FALC modes

The following register settings define the used system interface clock- and datarate configuration.

The used system interface clockrate is 8.192 MHz.

The used system interface datarate is 2.048 Mbit/s.

Table 3 T1 FALC mode specific QuadFALC configuration

Registers	Values
SIC1	0x82
SIC2	0x00
SIC3	0x00
CMR2	0x04

4.2.3.1 T1 FAM Multiframe based structured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'structured CES':

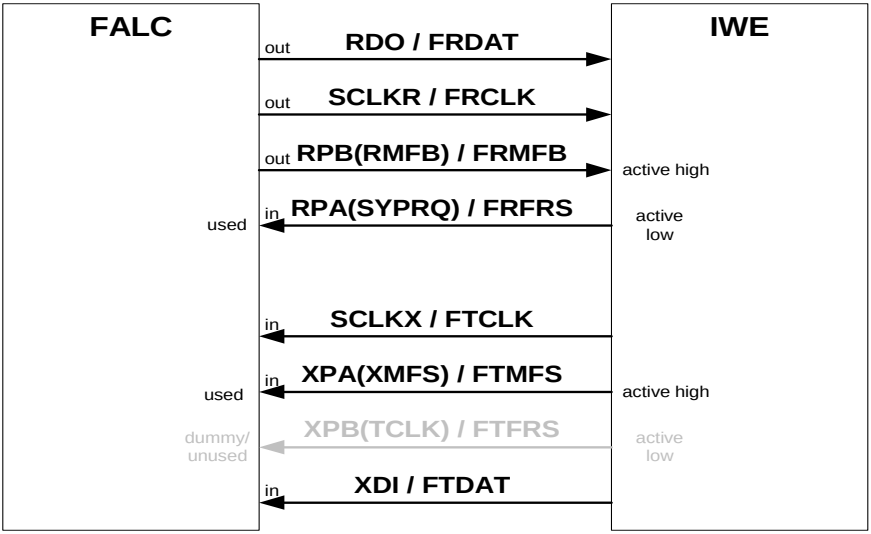

Figure 5 T1 FALC structured CES

Table 4 T1 FALC structured CES specific QuadFALC configuration

Registers	Values
PC1	0x01
PC2	0x23
PC5	0x0B
FMR2	0x60
FMR4	0x0E
LOOP	0x00
XC0	0x40
XC1	0x04

4.2.3.2 T1 FAM Unstructured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'unstructured CES':

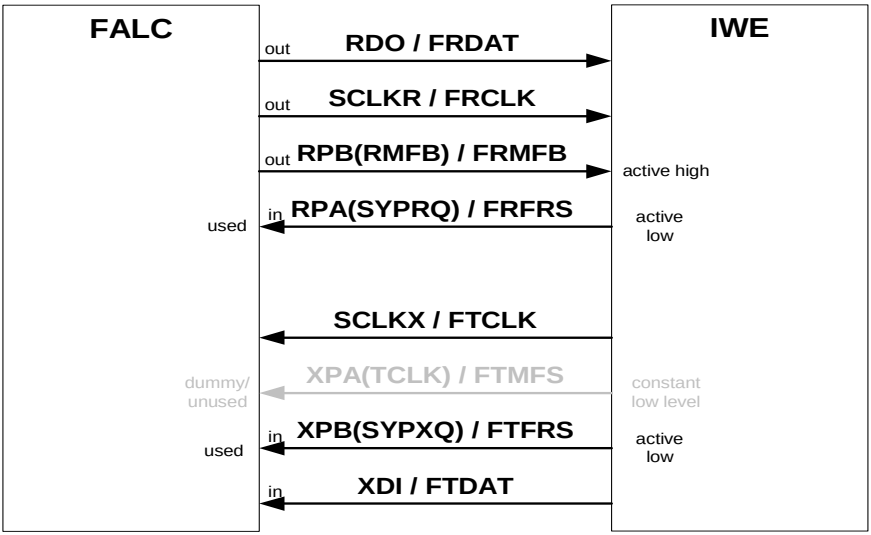

Figure 6 T1 FALC unstructured CES

Table 5 T1 FALC unstructured CES specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
FMR2	0x70
FMR4	0x4E
LOOP	0x40
XC0	0x00
XC1	0x23

4.2.3.3 T1 FAM ATM G.804 service

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'ATM':

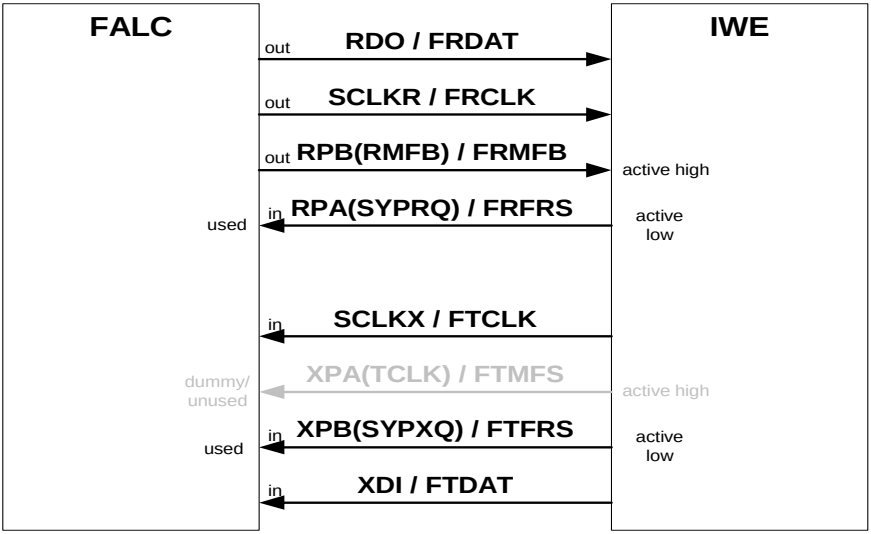

Figure 7 T1 FALC ATM

Table 6 T1 FALC ATM specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
FMR2	0x60
FMR4	0x0E
LOOP	0x00
XC0	0x40
XC1	0x23

4.2.4 T1 GIM modes

The following register settings define the used system interface clock- and datarate configuration.

The used system interface clockrate is 1.544 MHz.

The used system interface datarate is 1.544 Mbit/s.

Table 7 T1 GIM mode specific QuadFALC configuration

Registers	Values
SIC1	0x02
SIC2	0x10
SIC3	0x08
CMR2	0x0C
XC1	0x0B

4.2.4.1 T1 GIM Multiframe based structured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'structured CES':

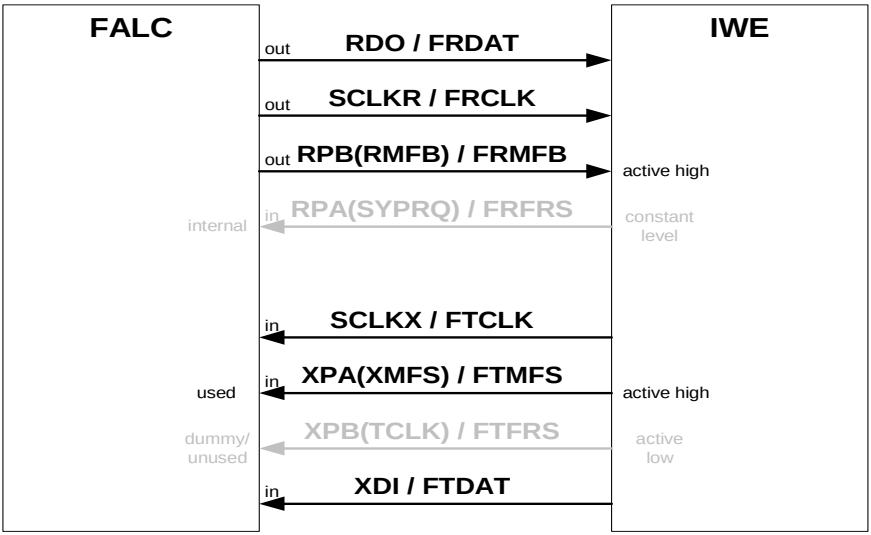

Figure 8 T1 GIM structured CES

Table 8 T1 GIM structured specific QuadFALC configuration

Registers	Values
PC1	0x01
PC2	0x23
PC5	0x0B
FMR2	0x60
FMR4	0x0E
LOOP	0x00
XC0	0x40

4.2.4.2 T1 GIM Unstructured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'unstructured CES':

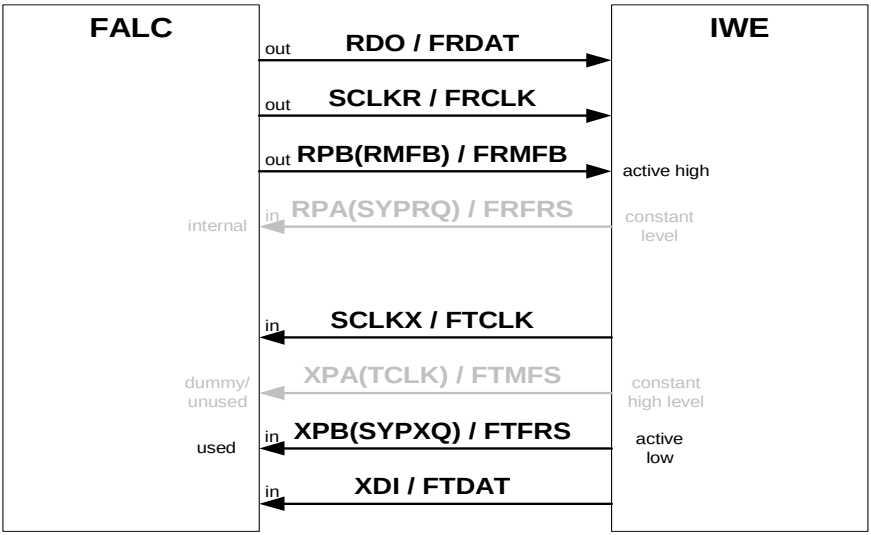

Figure 9 T1 GIM unstructured CES

Table 9 T1 GIM unstructured CES specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
FMR2	0x70
FMR4	0x4E
LOOP	0x40
XC0	0x00

4.2.4.3 T1 GIM ATM G.804 service

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'ATM':

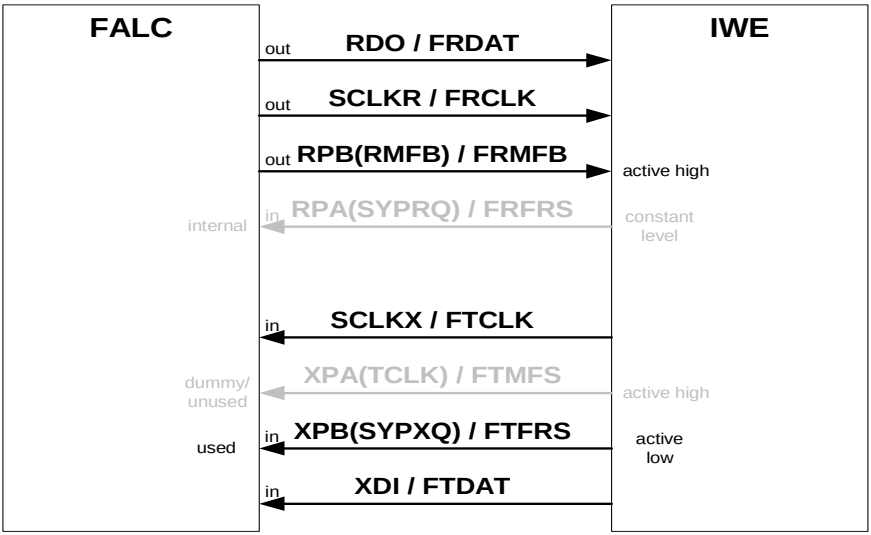

Figure 10 T1 GIM ATM

Table 10 T1 GIM ATM specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
FMR2	0x60
FMR4	0x0E
LOOP	0x00
XC0	0x40

4.2.5 Basic E1 configuration

The basic E1 configuration consists of defining unused multifunction port signals, clock routing, line interface mode, puls shape, interrupt usage and alarm handling.

The framer is programmed for CRC4 multiframing. The line interface generates standard E1 pulses with HDB3 line coding.

Table 11 Basic E1 configuration of the QuadFALC

Registers	Values
PC3	0x56
PC4	0x35
CMR1	n * 0x40 (n = 0..3; Channel)
CMR2	0x0F
LIM0	0x01 (Master); 0x00 (Slave)
LIM1	0x30
RC1	0x24
XPM0	0x9C
XPM1	0x03
XPM2	0x00
FMR0	0xF0
FMR1	0x4C
XSW	0x9F
IMR2	0x03[1)]
IMR3	0x3F[1)]
IMR4	0xFF[1)]
ESM	0x04[1)]
PCD	0x0A
PCR	0x15

1) Dependent or the interrupts to react on. This is a recommendation only

4.2.6 E1 FALC modes

The following register settings define the used system interface clock- and datarate configuration.

The used system interface clockrate is 8.192 MHz.

The used system interface datarate is 2.048 Mbit/s.

Table 12 E1 FALC mode specific QuadFALC configuration

Registers	Values
SIC1	0x82
SIC3	0x00
CMR2	0x04

4.2.6.1 E1 FAM Multiframe based structured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'structured CES':

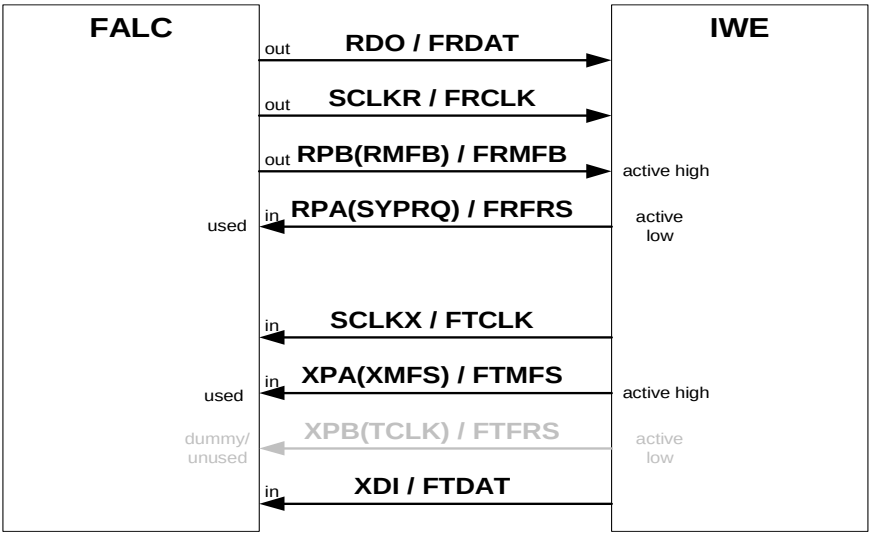

Figure 11 E1 FALC structured CES

Table 13 E1 FALC structured CES specific QuadFALC configuration

Registers	Values
PC1	0x01
PC2	0x23
PC5	0x0B
XC1	0x04
FMR2	0x83
XSP	0x1C

4.2.6.2 E1 FAM Unstructured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'unstructured CES':

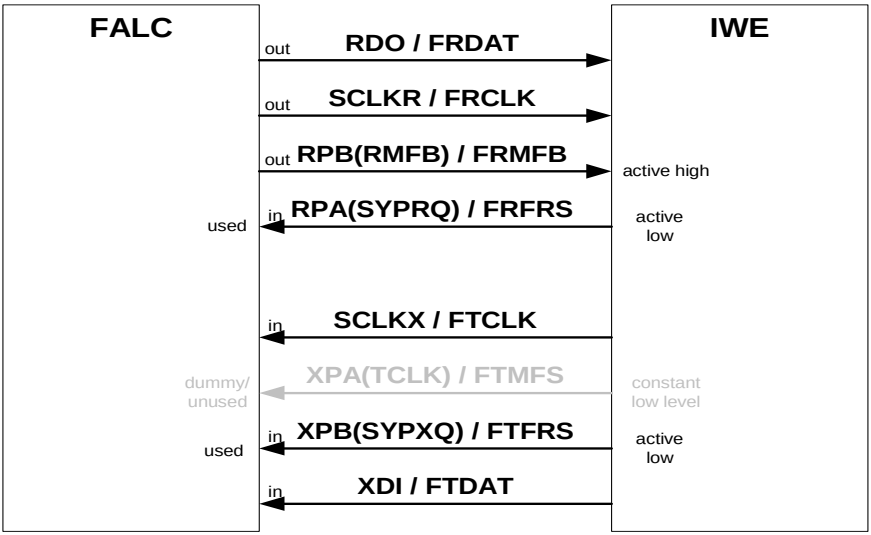

Figure 12 E1 FALC unstructured CES

Table 14 E1 FALC unstructured CES specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
XC1	0x23
FMR2	0xB3
XSP	0x3C

4.2.6.3 E1 FAM ATM G.804 service

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'ATM':

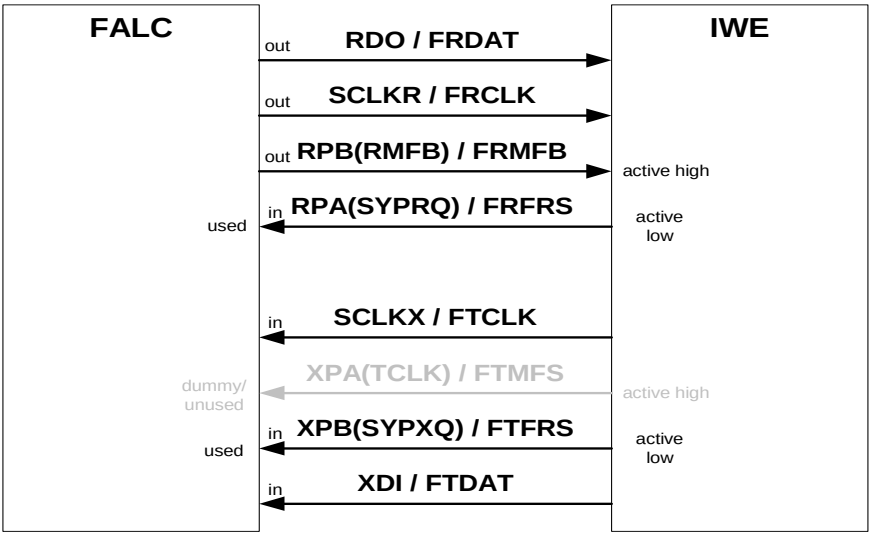

Figure 13 E1 FALC ATM

Table 15 E1 FALC ATM specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
XC1	0x23
FMR2	0x83
XSP	0x1C

4.2.7 E1 GIM modes

The following register settings define the used system interface clock- and datarate configuration.

The used system interface clockrate is 2.048 MHz.

The used system interface datarate is 2.048 Mbit/s.

Table 16 E1 GIM mode specific QuadFALC configuration

Registers	Values
SIC1	0x02
SIC3	0x08
CMR2	0x0C
XC1	0x04

4.2.7.1 E1 GIM Multiframe based structured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'structured CES':

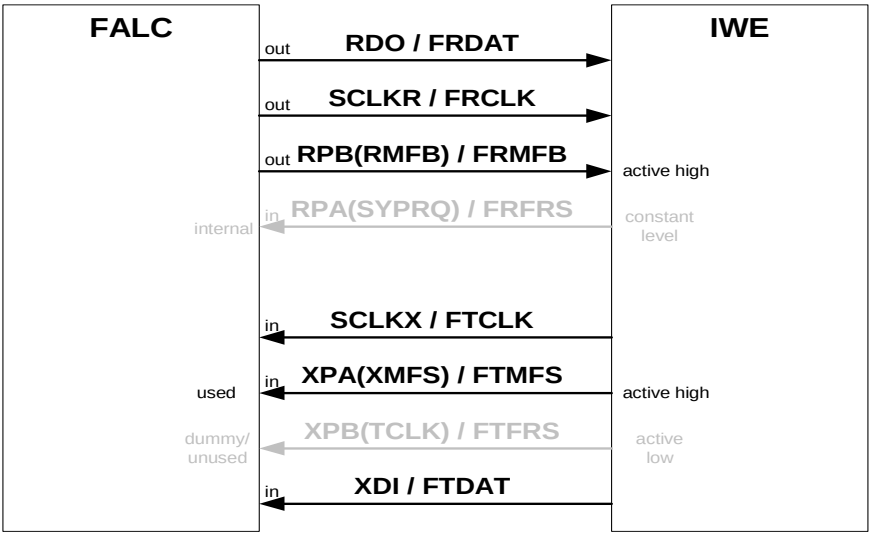

Figure 14 E1 GIM structured CES

Table 17 E1 GIM structured CES specific QuadFALC configuration

Registers	Values
PC1	0x01
PC2	0x23
PC5	0x0B
FMR2	0x83
XSP	0x1C

4.2.7.2 E1 GIM Unstructured CES

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'unstructured CES':

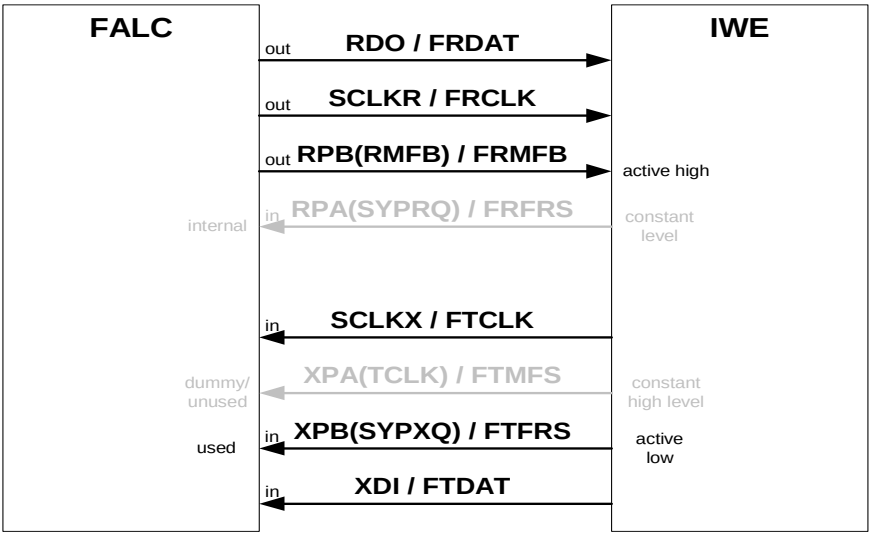

Figure 15 E1 GIM unstructured CES

Table 18 E1 GIM unstructured CES specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
FMR2	0xB3
XSP	0x3C

4.2.7.3 E1 GIM ATM G.804 service

The multifunction ports and bit offsetts on the system interface of the QuadFALC are configured according to the selected interworking mode 'ATM':

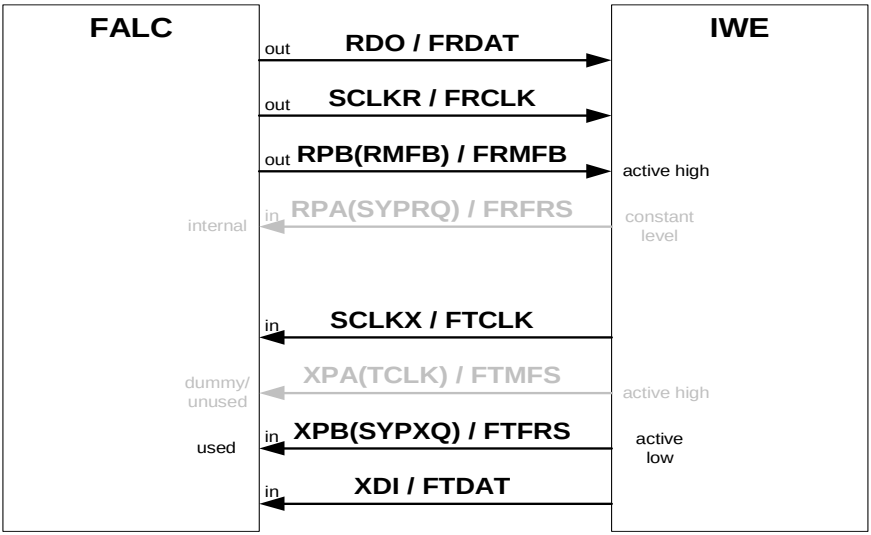

Figure 16 E1 GIM ATM

Table 19 E1 GIM ATM specific QuadFALC configuration

Registers	Values
PC1	0x03
PC2	0x20
PC5	0x03
FMR2	0x83
XSP	0x1C

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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