PowerPC™

IBM

High Speed and Performance

PowerPC 604e RISC Microprocessor 250, 300, 333 and 350MHz

Highlights

Dispatch Unit
- Dispatch up to 4 instructions per cycle
- 8-instruction dispatch buffer

Completion Unit
- Completes up to 4 instructions plus 1 store and 1 branch per cycle

Integer Unit
- 2 Simple Fixed Point units
- 1 Complex Fixed Point unit

Load/Store Unit
- Hardware supported misaligned little endian accesses
- Hardware controlled load-multiple and store-multiple registers and byte strings
- Data alignment to byte addresses
- Out of order loads and stores

Integrated Floating Point Unit
- IEEE-754 standard single-and double-precision floating point arithmetic

Cache
- Separate instruction and data caches, each 32K bytes, 4-way set associative
- 32-byte cache line
- Physically indexed, physical tags
- Hardware invalidate all cache lines
- Write-in and write-through data cache
- Data cache line-fill buffer forwarding
- Software cache disable

Branch Prediction and Processing
- 512-entry branch history table
- 64-entry branch target address cache, fully associative
- Branch prediction for unresolved branches

Memory Management Structure
- 32-bit real memory support for up to 4 GB
- 64-entry 2-way instruction and data TLB
- Hardware controlled TLB mishandling

Multiprocessor Support
- Bus snooping
- 4-state MESI data cache coherency control
- Dual port data cache tags
- Software controlled Instruction cache coherency, programmable coherent instruction fetch mode

Bus Interface
- 32-bit real address
- 64-bit data
- Processor Clock: Bus Clock ratios of 1:1, 3:2, 2:1, 5:2, 3:1, 7:2, 4:1, 9:2, 5:1, 11:2, 6:1, 13:2, 7:1

Performance Monitor
- Four programmable event counting registers
- Programmable trigger or interrupt signal

Testability
- IEEE 1149.1 (JTAG) compatible chip interface
- Level Sensitive Scan Design (LSSD)

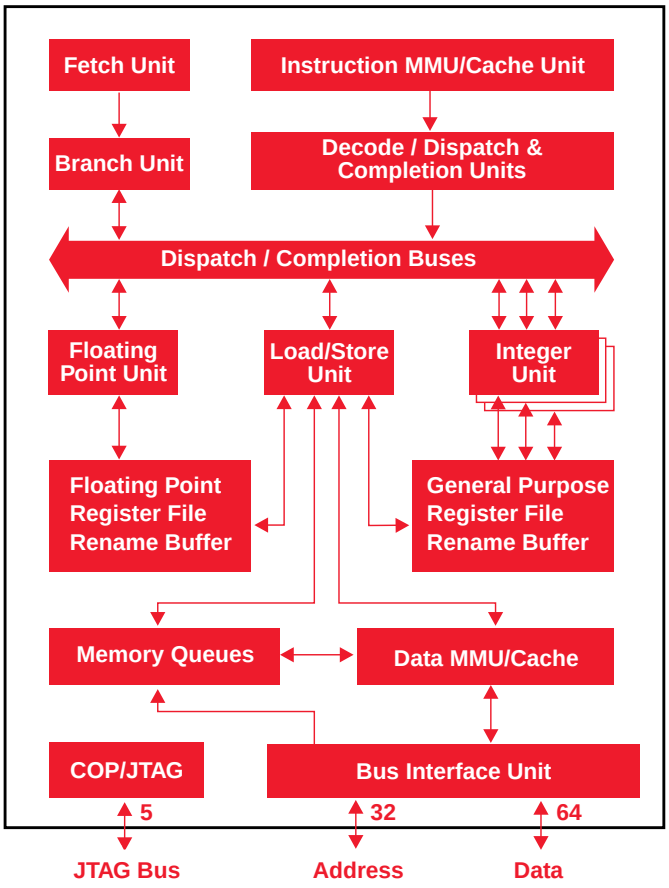
Product Description

The PowerPC 604e* microprocessor is a 32-bit implementation of the PowerPC* family of Reduced Instruction Set Computer (RISC) microprocessors. It is a functionally equivalent, enhanced microarchitecture derivative of the PowerPC 604e microprocessor using split voltages of 1.9 VDC for core logic and 3.3 VDC for I/O. The PowerPC 604e microprocessor is targeted at the workstation, PC server and power user desktop segments. The suite of operating environments available to systems designed in accordance with the PowerPC microprocessor Common Hardware Reference Platform Specification includes: Mac OS**, AIX*.

Enhancements to the PowerPC 604e microprocessor over previous releases include:

- Advanced .25 micron CMOS technology
- Higher clock frequencies with increased bus divider ratios
- Extended debug mode

Specifications	***PID 9q-604e and PID 10 q-604e***
Technology	.25µm / .15µmLeff - CMOS technology, six levels of metal
Die Size	47 mm^2
Number of Transistors	~5.1 million
Performance (estimated)	11.1 SPECint95, 7.8 SPECfp95 @ 250/71, 1M L2 cache 12.9 SPECint95, 8.5 SPECfp95 @ 300/75, 1M L2 cache 13.9 SPECint95, 8.6 SPECfp95 @ 333/74, 1M L2 cache 14.6 SPECint95, 9.0 SPECfp95 @ 350/77, 1M L2 cache
Signal I/Os	171
Power Supply†	1.9 V ± 100mV Core 3.3 V ± 5% I/O
Power Dissipation (est, typ)	7.5 W @ 333MHz
Temperature Range†	0°C to 85°C
Packaging	BGA



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