PowerPC 401GF 32-Bit RISC Embedded Controller

Data Sheet

Features

- PowerPC™ RISC CPU core and instruction set architecture
- Pipelined CPU core runs at up to 4X the external bus clock rate
- Separate instruction cache and write-back/ write-through data cache, both two-way set-associative
- Multiplexed external bus
- Configurable interfaces to memory and peripherals:
  – Device-paced wait states
  – 8-,16-, or 32-bit bus widths
  – Programmable hold states
- Flexible interface to external bus masters
- Integrated power management and clock generator
- Big-Endian or Little-Endian device attachment
- Hardware support for unaligned accesses
- Thirty-two 32-bit general purpose registers

Applications

- Set-top boxes
- Consumer electronics and video games
- Telecommunications and networking
- Office automation (printers, copiers, fax)
- Personal digital assistants (PDA)

Specifications

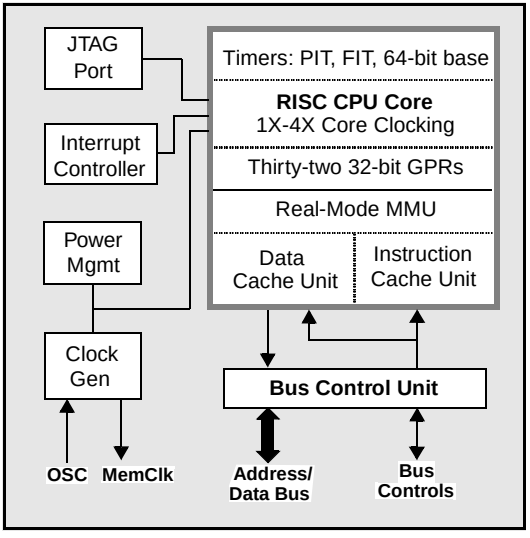
- CPU core frequency to 50 MHz, I/Os to 25 MHz
- Interfaces to both 3V and 5V technologies
- Low-power 3.3V operation with doze/nap/ sleep modes
- Low-cost 80-lead TQFP package
- 0.5 µm triple-level-metal CMOS

Overview

The 401GF RISC controller consists of a pipelined CPU core, data cache unit (DCU), instruction cache unit (ICU), memory management unit (MMU), bus control unit (BCU), asynchronous interrupt controller, and JTAG debug port.

The internal 2KB instruction cache and 1KB data cache reduce overhead for data transfers to or from external memory. Each cache unit consists of a data array and a tag array, and the MMU is provided for cache management and addressing.

The CPU core consists of general purpose registers (GPR), special purpose registers (SPR), ALU, barrel shifter, and the control logic required to manage data flow and instruction execution within the CPU core.



The CPU core handles instruction decoding and execution. The instruction cache unit passes instructions to the queue in the CPU core or, in the event of a cache miss, requests a fetch from external memory through the bus control unit.

General Purpose Registers

Data transfers to and from the CPU core are handled through the bank of 32 GPRs, each 32 bits wide. Load and store instructions move data operands between the GPRs and the data cache unit, except in the cases of noncacheable data or cache misses. In such cases the DCU passes the address for the data read or write to the BCU. When noncacheable operands are being transferred, data can pass directly between the CPU core and the BCU, which interfaces to the external memory being accessed.

Special Purpose Registers

Special purpose registers are used to control debug facilities, timers, interrupts, memory cacheability, and other architected processor resources. SPRs are accessed using move to/from special purpose register (mtspr/mfspr) instructions, which move operands between GPRs and SPRs.

Supervisory programs can write the appropriate SPRs to configure the operating and interface modes of the CPU core. The condition register (CR) and machine state register (MSR) are written by internal control logic with program execution status and machine state, respectively. Fixed-point arithmetic exception status is available from the exception register (XER).

Device Control Registers

Device control registers (DCR) are used to manage I/O interfaces. DCRs are accessed using move to/from device control register (mtdcr/mfdcr) instructions, which move operands between GPRs and DCRs.

Instruction Set

Table 1 summarizes the 401GF instruction set by categories of operations. When the requisite data and instructions are available in cache, the CPU core executes most instructions in a single cycle, with the exception of multiply, divide, and storage instructions.

Bus Control Unit

The BCU controls address output and data transfers on the multiplexed external bus, B0:31. To enhance data transfer bandwidth, the BCU supports both four-beat burst access and continuous burst access, up to 16 transfers.

Table 1. 401GF Instructions by Category

Category	Base Instructions
Data Movement	load, store
Arithmetic / Logical	add, subtract, negate, multiply, divide, and, or, xor, nand, nor, xnor, sign extension, count leading zeros
Comparison	compare, compare logical, compare immediate
Branch	branch, branch conditional
Condition	condition register logical
Rotate/Shift	rotate, rotate and mask, shift left, shift right
Cache Control	invalidate, touch, zero, flush, store
Interrupt Control	write to external interrupt enable bit, move to/from machine state register, return from interrupt, return from critical interrupt
Processor Management	system call, synchronize, move to/from device control registers, move to/from special purpose registers

All 401GF external bus operations are synchronous to the MemClk output, simplifying control logic for external memory attached to the bus. The external bus interface can be programmed to operate at 1x, 1/2x, 1/3x or 1/4x the internal clock speed. Bus width is programmable to support attachment to 8-, 16-, and 32-bit memory and peripherals. Further details of peripheral attachment are given in "Connecting to the 401GF Bus," on page 12.

Memory Addressing Regions

The 401GF can address an effective range of four gigabytes, mapped to eight 512MB regions. Region attributes such as hold time, bus width, burst mode, and cache line mode (sequential/ target word first) are controlled by the eight bus region control registers (BRCR). Wait states are device-paced so the bus interface can be used with I/O devices of varying speeds.

Cacheability with respect to the instruction and data caches is programmed via the instruction and data cache control registers, respectively.

Instruction Cache Unit

The instruction cache unit (ICU) is a two-way set-associative 2KB cache memory unit. The ICU is organized as 64 sets of 2 lines, each line containing 16 bytes.

The cache can send one cached instruction per cycle to the CPU core. The instruction queue can buffer two prefetched instructions, in addition to the instruction being decoded and the instruction currently being executed.

A separate bypass path is available to handle cache-inhibited instructions and to improve performance during line fill operations.

Data Cache Unit

The data cache unit is provided to minimize the access time of frequently used data items in external memory. The 1KB cache is organized as a two-way set associative cache. There are 32 sets of 2 lines, each line containing 16 bytes of data. The cache features byte-writeability to improve the performance of byte and halfword store operations.

Cache operations are performed using write-back or write-through strategy, as programmed in the data cache write-through register. A write-back cache only updates locations in external memory that corresponds to changed locations in the cache. Data is flushed from the cache to external memory whenever changed data needs to be removed from the cache to make room for other data. Write-through cache operation is supported as a programmable cache management option.

The data cache may be disabled for a memory region via control bits in the data cache control register. A separate bypass path is available to handle cache-inhibited data operations and to improve performance during line fill operations. Cache flushing and filling are triggered by load, store, and cache control instructions executed by the processor.

Exception Handling

The 401GF contains a unique dual-level interrupt structure, which is specific to the IBM PowerPC 400Series family. This interrupt structure allows for a typical latency of 3 cycles to critical system interrupts as well as robust debug capability, even for first level interrupt handlers.

Exceptions are generated by interrupts from external peripherals, instructions, the internal timer facility, debug events or error conditions. Two external interrupt signals are provided on the 401GF: one critical and one general-purpose.

The 401GF processes exceptions as either, critical or non-critical. Four exceptions are defined as critical: machine check exceptions, debug exceptions, exceptions caused by an active level on the critical interrupt pin, and the first time-out from the watchdog timer.All other exceptions are non-critical.

Each class of exception has its own pair of save/ restore registers to hold the status and instruction address of the routine which was running at the time of the exception. This state is automatically restored upon execution of a return-from-interrupt (rfi) or return-from-critical-interrupt (rfci) instruction.

Timers

The 401GF contains four timer functions: a time base, a programmable interval timer (PIT), a fixed interval timer (FIT), and a watchdog timer. The time base is a 64-bit counter incremented by an internal signal equal to the CPU core clock rate. No interrupts are generated when the time base rolls over.

The programmable interval timer is a 32-bit register that is decremented at the same rate as the time base is incremented. The user preloads the PIT register with a value to create the desired delay. When the register is decremented to zero, the timer stops decrementing, a bit is set in the timer status register (TSR), and a PIT interrupt is generated. Optionally, the PIT can be programmed to reload automatically the last value written to the PIT register, after which the PIT begins decrementing again.The timer control register (TCR) contains the interrupt enable for the PIT interrupt.

The fixed interval timer generates periodic interrupts based on selected bits in the time base. Users may select one of four intervals for the timer period by setting the correct bits in the TCR. When the selected bit in the time base changes from 0 to 1, a bit is set in the TSR and a FIT interrupt is generated. The FIT interrupt enable is contained in the TCR.

The watchdog timer generates a periodic interrupt based on selected bits in the time base. Users may select one of four time periods for the interval and the type of reset generated if the watchdog timer expires twice without an intervening clear from software.

Clock Generation and Power Management

The 401GF clock unit integrates clock generation and power management. The clock unit uses a crystal or oscillator input as a reference, generating both the internal clock signal used by the CPU core and the MemClk output from the 401GF. Duty cycle correction is performed on the crystal or oscillator reference input, as needed.

The CPU core can operate with a clock rate up to four times that of the external bus, up to a maximum frequency of 50 MHz and a maximum bus frequency of 25 MHz.

The clock unit also provides sleep mode management, reducing standby power consumption when programmed to invoke the three sleep modes (doze, nap, and sleep) available on the 401GF.

JTAG Port

The JTAG port has been enhanced to allow it to be used as a debug port. Through the JTAG test access port, debug software on a workstation can single-step the processor and interrogate internal processor state to facilitate software debugging. The standard JTAG boundary-scan register allows testing of circuitry external to the chip, primarily the board interconnect. Alternatively, the JTAG bypass register can be selected when no other test data register needs to be accessed during a board-level test operation.

P/N Code

Table 2. PPC401GF Part Number

MHz (CPU Core)	Part Number
50	PPC401GF-MC50C2

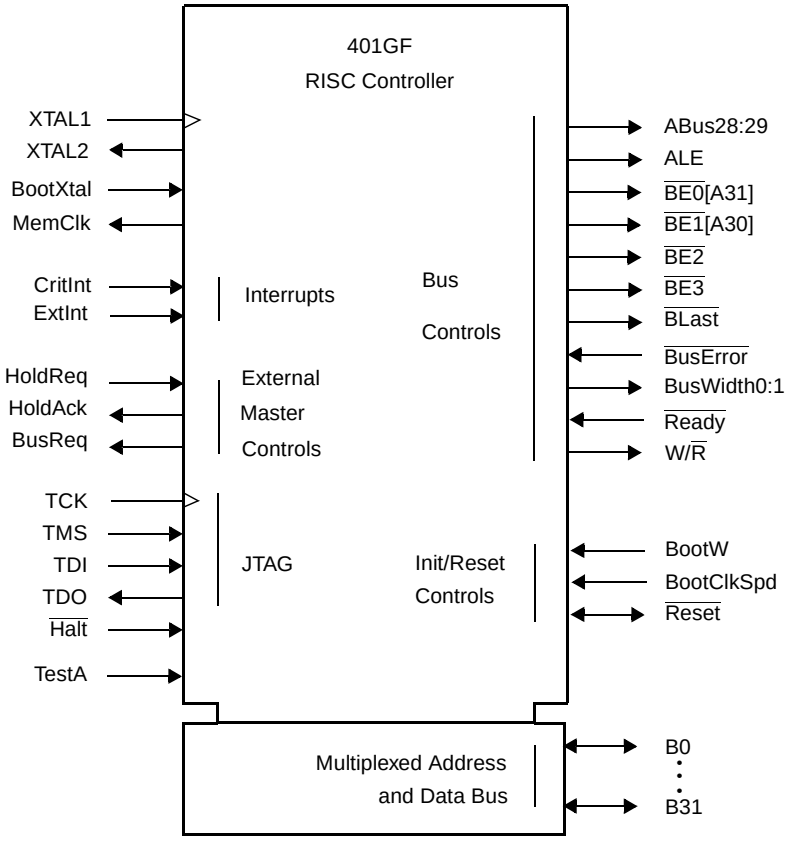
Notes:

1. The dash number indicates the speed version (maximum internal clock rate).
2. The characters in the dash number indicate package type (M), revision level (C), maximum internal CPU core clock rate (MHz), commercial version (C), ratio of CPU core speed to external bus clock rate (2:1).

For availability of 401GF versions operating at faster CPU core frequencies, please contact your IBM Microelectronics sales representative.

Logic Symbol

Signals in brackets are multiplexed.



Pin Functional Descriptions

Active-low signals are shown with overbars: $\overline{BE0}$. Multiplexed signals are alphabetized under the first (unmultiplexed) signal names on the same pins: $\overline{BE0}$[A31]. The 401GF logic symbol above shows all signals arranged by functional groups.

Table 3. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
-	Pin must be connected as described.
S(...)	Synchronous. Inputs must meet setup and hold times relative to MemClk for proper operation. S(E) Edge sensitive S(L) Level sensitive
T(...)	Synchronous to TCK. T(E) Edge sensitive input T(L) Level sensitive input
A(...)	Asynchronous. Inputs may be asynchronous relative to the MemClk A(E) Edge sensitive input A(L) Level sensitive input
R(...)	While the processor's $\overline{Reset}$ pin is asserted, the pin: R(1) is driven high R(0) is driven low R(Q) is a valid output R(X) is driven to unknown state R(Z) is placed in high impedance
H(...)	While the processor is in the hold state, the pin: H(1) is driven high H(0) is driven low H(Q) Maintains previous state or continues to be a valid output H(Z) Floats

Table 4. 401GF Signal Descriptions

Signal Name	Pin	I/O Type	Function
ABus28	77	O R(Z) H(Z)	Address bits A28:29. ABus28:29 output a partial unmultiplexed word address during the Address state. The partial word address is incremented, with each assertion of Ready, during burst transfers.
ABus29	78		
ALE	76	O R(0) H(Z)	Address Latch Enable. The 401GF asserts this signal high at the beginning of the cycle when an address is output on the multiplexed bus. The signal goes inactive before the beginning of the Data state. For an early implementation of the 401GF (Part No. PPC401GF-MA50C2), the polarity of the ALE signal was reversed and this signal was active low (ALE). For all other PPC401GF chips, ALE is active high.
B0	39	I/O S(L) R(Z) H(Z)	Multiplexed bus bit 0. This bus, B0:31, carries 32-bit physical addresses and 8-, 16-, and 32-bit data to and from memory. During the Wait/Data state, read or write data is present on one or more contiguous bytes. During write operations, unused pins continue to drive address; during read operations, unused pins are hi-Z. The determinate values are also driven on the bus during the Idle state.
B1	38	I/O	Multiplexed bus bit 1
B2	37	I/O	Multiplexed bus bit 2
B3	36	I/O	Multiplexed bus bit 3
B4	35	I/O S(L) R(Z) H(Z)	Multiplexed bus bit 4. Depending on burst mode configuration, transfer size information is output on B6:7 (BRCR*n*[MB] = 0) for a four-beat burst, or on B4:7 (BRCR*n*[MB] = 1) for continuous burst (up to 16 transfers).
B5	34	I/O	Multiplexed bus bit 5. See description of B4 above.
B6	33	I/O	Multiplexed bus bit 6. See description of B4 above.
B7	29	I/O	Multiplexed bus bit 7. See description of B4 above.
B8	49	I/O	Multiplexed bus bit 8
B9	48	I/O	Multiplexed bus bit 9
B10	47	I/O	Multiplexed bus bit 10
B11	46	I/O	Multiplexed bus bit 11
B12	45	I/O	Multiplexed bus bit 12
B13	42	I/O	Multiplexed bus bit 13
B14	41	I/O	Multiplexed bus bit 14
B15	40	I/O	Multiplexed bus bit 15
B16	61	I/O	Multiplexed bus bit 16

Table 4. 401GF Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
B17	60	I/O	Multiplexed bus bit 17
B18	59	I/O	Multiplexed bus bit 18
B19	56	I/O	Multiplexed bus bit 19
B20	55	I/O	Multiplexed bus bit 20
B21	54	I/O	Multiplexed bus bit 21
B22	53	I/O	Multiplexed bus bit 22
B23	52	I/O	Multiplexed bus bit 23
B24	72	I/O	Multiplexed bus bit 24
B25	68	I/O	Multiplexed bus bit 25
B26	67	I/O	Multiplexed bus bit 26
B27	66	I/O	Multiplexed bus bit 27
B28	65	I/O	Multiplexed bus bit 28
B29	64	I/O	Multiplexed bus bit 29
B30	63	I/O	Multiplexed bus bit 30
B31	62	I/O	Multiplexed bus bit 31
$\overline{BE0}$[A31]	24	O R(1) H(Z)	Byte Enable 0[Address 31]. $\overline{BE0:3}$ select which (of up to four) bytes on the bus participate in the current bus access. Byte enable encoding depends on the bus width of the memory region accessed. $\overline{BE0}$ $\overline{BE1}$ $\overline{BE2}$ $\overline{BE3}$ 32-Bit Bus Accesses: Enables B0:7 / Enables B8:15 / Enables B16:23 / Enables B24:31 16-Bit Bus Accesses: Enables B0:7 / Becomes addr A30 / Unused (high) / Enables B8:15 8-Bit Bus Accesses: Becomes addr A31 / Becomes addr A30 / Unused (high) / Unused (high) The 401GF asserts byte enables during the Address state. For unaligned burst transfers, these signals switch with each assertion of $\overline{Ready}$.
$\overline{BE1}$[A30]	25	O	Byte Enable 1[Address 30]
$\overline{BE2}$	27	O	Byte Enable 2
$\overline{BE3}$	28	O	Byte Enable 3

Table 4. 401GF Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
BLast	21	O R(1) H(Z)	Burst Last. Indicates the last transfer of a memory access, whether burst or nonburst. BLast stays active as long as the Ready signal is not asserted to introduce wait states on the external bus. BLast goes inactive when the last transfer of an external bus transaction is done.
BootClkSpd	19	I S(L)	The Boot Clock Speed pin determines the internal clock speed and the bus clock speed. BootClkSpd — Internal Clock — MemClk 0 — 1X of input clock — 1X of internal clock 1 — 1/4X of input clock — 1/4X of internal clock
BootXtal	7	I S(L)	Boot Crystal. This pin is for internal use only and should always be fixed high.
BootW	9	I S(L)	Boot-up ROM Width Select. BootW is sampled before and after the Reset pin is active to determine the width of the boot-up ROM. If this pin is tied to logic 0 when sampled on reset, an 8-bit boot width is assumed. If BootW is tied to logic 1, a 32-bit boot width is assumed. For 16-bit boot widths, this pin should be tied to the Reset pin.
BusError	13	I S(L)	Bus Error Input. A logic 0 input to the BusError pin by an external device signals to the 401GF that an error occurred on the bus transaction. BusError is only sampled when Ready is asserted.
BusReq	22	O R(Q) H(Q)	Bus Request. While HoldAck is active, BusReq is active when the 401GF has a bus operation pending and needs to regain control of the bus. BusReq is also active during bus operations.
BusWidth0	79	O R(Z) H(Z)	BusWidth0:1 indicates the width of a bus transaction on the 401GF external multiplexed bus: 00 = 8 bit, 01 = 16 bit, 10 = 32 bit, 11 = reserved.
BusWidth1	80		
CritInt	15	I A(L)	Critical Interrupt. CritInt is a critical interrupt input to the 401GF and users may program the polarity to be active high or active low. The IOCR contains the bit necessary to program the polarity.
ExtInt	14	I A(L)	External interrupt. ExtInt is an interrupt input to the 401GF and users may program the polarity to be active high or active low. The IOCR contains the bit necessary to program the polarity.

Table 4. 401GF Signal Descriptions (Continued)

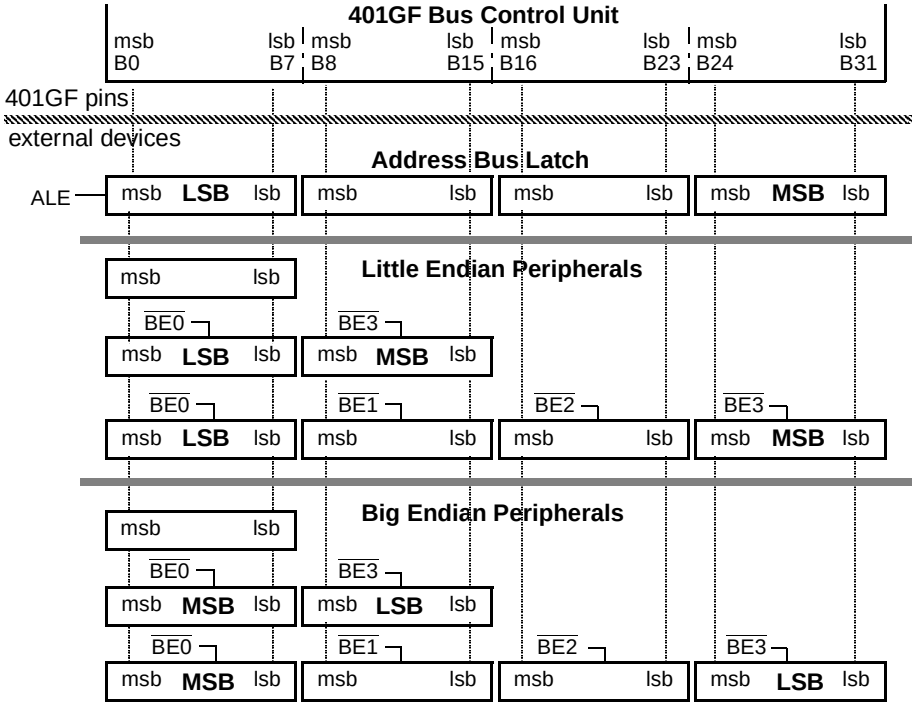
Signal Name	Pin	I/O Type	Function
GND	10	—	Ground. All ground pins must be used.
	30	—	Ground. All ground pins must be used.
	32	—	Ground. All ground pins must be used.
	43	—	Ground. All ground pins must be used.
	50	—	Ground. All ground pins must be used.
	58	—	Ground. All ground pins must be used.
	69	—	Ground. All ground pins must be used.
	71	—	Ground. All ground pins must be used.
	75	—	Ground. All ground pins must be used.
$\overline{\text{Halt}}$	16	I, A(L)	Halt from external debugger, active low.
HoldAck	2	O R(Q) H(1)	Hold Acknowledge. HoldAck outputs a logic 1 when the 401GF relinquishes its external bus to an external bus master. The external bus master uses the HoldReq pin to request use of the 401GF bus.
HoldReq	11	I S(L)	Hold Request. External bus masters can request the 401GF bus by placing a logic1 on this pin. When the 401GF HoldAck pin is logic 1, the 401GF has relinquished its external bus to the external master. The external bus master relinquishes the bus to the 401GF by deasserting HoldReq. The 401GF then deasserts HoldAck during the following cycle.
MemClk	5	O R(Q) H(Q)	Memory Clock. Clock output from the internal 401GF clock generator. MemClk is a clock output at the bus frequency. The bus can be configured to run at 1x, 1/2x, 1/3x or 1/4x the internal clock frequency. See “MemClk Termination” on page 16.
$\overline{\text{Ready}}$	12	I S(L)	Ready. $\overline{\text{Ready}}$ inserts externally generated (device-paced) wait states into bus transactions. $\overline{\text{Ready}}$ indicates to the 401GF that data on the external bus can be sampled or removed.
$\overline{\text{Reset}}$	73	I/O R(L)	Reset. As an input, the $\overline{\text{Reset}}$ pin is driven low for 1 ms to perform a system reset. The $\overline{\text{Reset}}$ signal, used as an output, can be driven by software or an external debug tool. When a system reset occurs, the $\overline{\text{Reset}}$ pin outputs logic 0 for up to 2048 internal clock cycles.
TCK	18	I	JTAG Test Clock Input. TCK is the clock source for the 401GF test access port (TAP). The maximum clock rate into the TCK pin is one half of the processor MemClk clock rate.
TDI	8	I T(L)	Test Data In. The TDI is used to input serial data into the TAP. When the TAP enables the use of the TDI pin, the TDI pin is sampled on the rising edge of TCK and this data is input to the selected TAP shift register.

Table 4. 401GF Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
TDO	1	O, R(Z), H(Q), T(L)	Test Data Output. TDO is used to transmit data from the 401GF TAP. Data from the selected TAP shift register is shifted out on TDO.
TestA	20	I	Reserved for manufacturing test. Tied low for normal operation.
TMS	17	I T(L)	Test Mode Select. The TMS pin is sampled by the TAP on the rising edge of TCK. The TAP state machine uses the TMS pin to determine the mode in which the TAP operates.
V_{DD}	6	—	Power. All power pins must be connected to 3.3V supply.
	26	—	Power. All power pins must be connected to 3.3V supply.
	31	—	Power. All power pins must be connected to 3.3V supply.
	44	—	Power. All power pins must be connected to 3.3V supply.
	51	—	Power. All power pins must be connected to 3.3V supply.
	57	—	Power. All power pins must be connected to 3.3V supply.
V_{DD}	70	—	Power. All power pins must be connected to 3.3V supply.
	74	—	Power. All power pins must be connected to 3.3V supply.
W/$\overline{R}$	23	O R(0) H(Z)	Write/$\overline{Read}$. When the 401GF is bus master, W/$\overline{R}$ is an output (asserted only in address cycle) that is low when data is read from memory or a peripheral and high when data is written to memory or a peripheral.
XTAL1	3	—	Crystal 1 input. XTAL1 is the processor clock input. This pin can be connected to a oscillator or a crystal.
XTAL2	4	—	Crystal 2 output. XTAL2 is connected to the crystal. If XTAL1 is connected to an oscillator instead of a crystal, this pin should be left unconnected.

Connecting to the 401GF Bus

The figure below shows the byte and bit connections for attaching memory or peripheral devices to the 401GF external bus pins, B0:31. Connect 8-bit devices to B0:7. For multibyte devices, connect the least significant bytes (LSB) and most significant bytes (MSB) as indicated below, preserving normal ordering from most significant bit (msb) to least significant bit (lsb) within each byte.



The 401GF external bus pins used for address output and data transfers are shown in the table below. Address bits output by the 401GF are numbered A0:31, with A0 as the most significant bit (msb).

Word address output by 401GF:	A0 (msb):7	A8:15	A16:23	A24:27 (see note)
401GF pins used to output address:	B24 (msb):31	B16:23	B8:15	B0:3

Note: Address bits A28:31 are provided on pins ABus28:29, $\overline{BE1}$[A30], and $\overline{BE0}$[A31], respectively.

Data bytes transferred:	Byte 0	Byte 1	Byte 2	Byte 3
401GF pins used by data transfer:	B0:7	B8:15	B16:23	B24:31

Connect $\overline{BE0}$ and $\overline{BE1}$ to the lsb and second lsb address inputs of an external 8-bit device. Connect $\overline{BE1}$ to the second lsb address input of an external 16-bit device. Connect ABus28:29 to the fourth and third lsb address inputs of an external 32-bit device.

TQFP Mechanical Drawing (Top View)

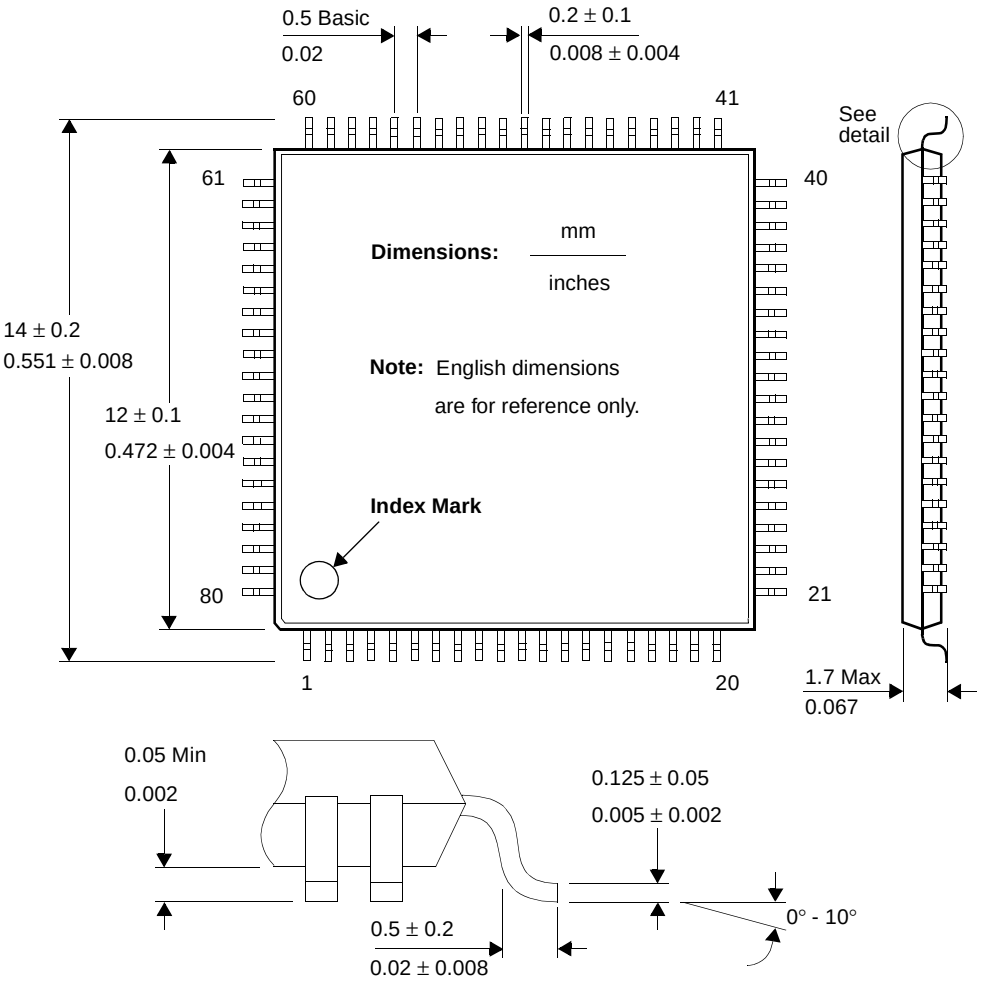


Table 5. Signals Ordered by Pin Number

Pin	Signal Names	Pin	Signal Names	Pin	Signal Names	Pin	Signal Names
1	TDO	21	$\overline{\text{BLast}}$	41	B14	61	B16
2	HoldAck	22	BusReq	42	B13	62	B31
3	XTAL1	23	W/$\overline{\text{R}}$	43	GND	63	B30
4	XTAL2	24	$\overline{\text{BE0}}$[A31]	44	V_{DD}	64	B29
5	MemClk	25	$\overline{\text{BE1}}$[A30]	45	B12	65	B28
6	V_{DD}	26	V_{DD}	46	B11	66	B27
7	BootXtal	27	$\overline{\text{BE2}}$	47	B10	67	B26
8	TDI	28	$\overline{\text{BE3}}$	48	B9	68	B25
9	BootW	29	B7	49	B8	69	GND
10	GND	30	GND	50	GND	70	V_{DD}
11	HoldReq	31	V_{DD}	51	V_{DD}	71	GND
12	$\overline{\text{Ready}}$	32	GND	52	B23	72	B24
13	$\overline{\text{BusError}}$	33	B6	53	B22	73	$\overline{\text{Reset}}$
14	ExtInt	34	B5	54	B21	74	V_{DD}
15	CritInt	35	B4	55	B20	75	GND
16	$\overline{\text{Halt}}$	36	B3	56	B19	76	ALE
17	TMS	37	B2	57	V_{DD}	77	ABus28
18	TCK	38	B1	58	GND	78	ABus29
19	BootClkSpd	39	B0	59	B18	79	BusWidth0
20	TestA	40	B15	60	B17	80	BusWidth1

Package Thermal Specifications

The 401GF is designed to operate within the case temperature range from 0°C to 120°C. Thermal resistance values for the TQFP are shown in Table 6:

Table 6. Thermal Resistance (°C/Watt)

Parameter	Airflow-ft/min (m/sec)		
	0 (0)	100 (0.51)	200 (1.02)
θ_{JC} Junction to case	2	2	2
θ_{CA} Case to ambient (without heatsink)	37.2	31.6	29.8

Notes:
1. Case temperature Tm_C is measured at top center of case surface with device soldered to circuit board.
2. $Tm_A = Tm_C - P \times \theta_{CA}$, where Tm_A is ambient temperature.
3. $Tm_{CMax} = Tm_{JMax} - P \times \theta_{JC}$, where Tm_{JMax} is maximum junction temperature and P is power consumption.
4. The above assumes that the chip is mounted on a card with at least one signal and two power planes.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

The absolute maximum ratings in Table 7 below are stress ratings only. Operation at or beyond these maximum ratings may cause permanent damage to the device.

Table 7. 401GF Maximum Ratings

Parameter	Maximum Rating
Supply voltage with respect to GND	-0.5V to +3.8V
Voltage on other pins with respect to GND	-0.5V to +5.25V (See Note)
Case temperature under bias	0°C to +120°C
Storage temperature	-65°C to +150°C

Note: Maximum input voltage applied to the XTAL1 input pin must not exceed 3.47 V.

Operating Conditions

The 401GF can interface to either 3V or 5V technologies. The range for supply voltages is specified for five-percent margins relative to a nominal 3.3V power supply. Device operation beyond the conditions specified in Table 8 is not recommended. Extended operation beyond the recommended conditions may affect device reliability:

Table 8. Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	3.14	3.47	V
F_{XTAL1}	XTAL1 input frequency	24.975	25.025	MHz
	Input high time	14		ns
	Input low time	14		
Tm_C	Case temperature under bias	0	+85	°C

Note: If used, a 3.3V oscillator should be placed as close as possible to the XTAL1 input.

Power Considerations

Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements. Typical power dissipation for 25MHz external bus operation and 50MHz CPU core operation is estimated as 203 mW at Tm_C = 25 °C, and V_{CC} = 3.3 V, with an average 50pF capacitive load.

Estimated supply current as a function of frequency is shown in the figure, "MemClk Output Derating Curves," on page 22. Derating curves are provided in the section, "Output Derating for Capacitance and Voltage," on page 22.

Recommended Connections

Power and ground pins should all be connected to separate power and ground planes in the circuit board to which the 401GF is mounted. Unused input pins must be tied inactive, either high or low.

MemClk Termination

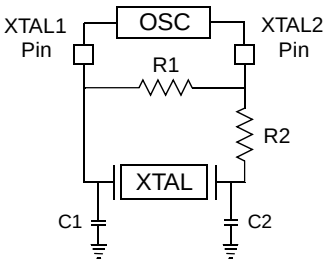
When MemClk Alignment is enabled (IOCR[MCA] = 1), MemClk must be terminated such that voltage spikes on the rising edge of MemClk do not appear at the off-chip driver. These spikes are caused by impedance mismatches. Impedance mismatches between the off-chip driver at MemClk and external loading may result in reflections which distort the positive rising edge of MemClk. The MemClk off-chip driver has an output impedance of 10 ohms.

Connecting a Crystal to the 401GF

Attach a quartz crystal such as a Seiko Epson MA-506 or equivalent across the XTAL1 input and the XTAL2 output. Locate the crystal within 1.2 cm (0.5 inch) of the 401GF pins to minimize stray capacitance that can affect C_{LOAD} capacitance and, in turn, oscillator frequency and stability. The expression at right can be used to determine the C_{LOAD} value.

$$C_{LOAD} = \frac{C_1 C_2}{C_1 + C_2} + C_{STRAY}$$

The figure at right shows details concerning the inclusion of resistors and load capacitors required with the crystal.Typical values for load capacitors C1 and C2 are 5-10pF. Typical values for resistor R1 are in the range of 1-5 megohms. Series resistor R2 is determined by the value of C2 and the OSC output resistance, 150-200 ohms. The Q factor of the RC circuit should be in the range of $2 \leq Q \leq 5$, deriving Q from the expressions below:



$$Q = \frac{R_{OUT} + R2}{X_{C2}}$$

$$R2 = QX_{C2} - R_{OUT}$$

Where: R_{OUT} = OSC output resistance
R2 = resistor value to derive
X_{C2} = C2 capacitive reactance at OSC frequency

R2 functions as a current limiting resistor to the crystal, and also as an oscillation stabilizer in the presence of perturbations induced by moisture, component variations, or other factors.

DC Specifications

Table 9. 401GF DC Characteristics

Symbol	Parameter	Min	Max	Units
V_{IL}	Input low voltage	GND - 0.1	0.8	V
V_{IH}	Input high voltage	2.0 (Note 4)	5.25 (Note 2)	V
V_{OL}	Output low voltage		0.4	V
V_{OH}	Output high voltage	2.0	3.47	V
I_{OH}	Output high current		2	mA
I_{OL}	Output low current		4	mA
I_{LI}	Input leakage current		75	µA
I_{LO}	Output leakage current		10	µA
I_{CC}	Supply current ($I_{CC\ Max}$ at F_C of 25MHz)[1]		90	mA

Notes:
1. $I_{CC\ Max}$ is measured at $T_J = 85°C$, worst-case recommended operating conditions for frequency and voltage as specified in "Operating Conditions," on page 15, and a capacitive load of 50 pF.
2. The maximum V_{IH} level applied to the XTAL1 input pin must not exceed 3.47 V.
3. The maximum V_{IL} level applied to the XTAL1 input pin must not exceed 0.4 V.
4. For reset pin, V_{IH} min is 2.2 V.

Table 10. Nominal Sleep-Mode Power

Mode	PMCR0[1] Value	Description	MCA[2] Power	
			Off	On
1	00004000	Awake: processor halted	41.79mW	47.73mW
2	10004000	Timer doze: timers off	41.13mW	47.07mW
3	20004000	Chip doze: chip clock off	35.89mW	41.83mW
4	30004000	Timer and chip doze: timers and chip clock are off	30.54mW	36.48mW
5	40004000	Nap: only the crystal oscillator is running	5.63mW	—
6	80004000	Deep sleep: everything is off	0mW[3]	—

Notes:
1. Power Management Control Register.
2. MemClk Alignment.
3. Based on tested samples exhibiting no I/O leakage. It is possible for some leakage to be present, but less than the maximum defined by the I/O leakage specification. In such cases, a small amount of power may be consumed.
4. The test conditions were 3.3V, 25 °C, core:bus speed set to 1:1, with MemClk driving a 25pF capacitive load.

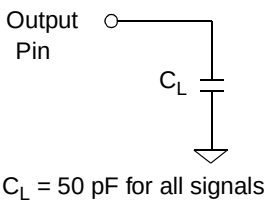
Table 11. 401GF I/O Capacitance

Symbol	Parameter	Min	Max	Units
C_{IN}	Input capacitance		5	pF
C_{OUT}	Output capacitance[1]		7	pF
$C_{I/O}$	I/O pin capacitance		8	pF

Notes:
1. C_{Out} is specified as the load capacitance of a floating output in high impedance.

AC Specifications

Clock timing and switching characteristics are specified in accordance with recommended operating conditions in Table 8. AC specifications are characterized at voltage $3.14V \le V_{DD} \le 3.5V$ and junction temperature $0°C \le T_J \le 85°C$ with the 50pF test load shown in the figure at right. Derating of outputs for capacitive loading is shown in the figure "Output Derating for Capacitance and Voltage," on page 22.



C_L = 50 pF for all signals

MemClk Timing

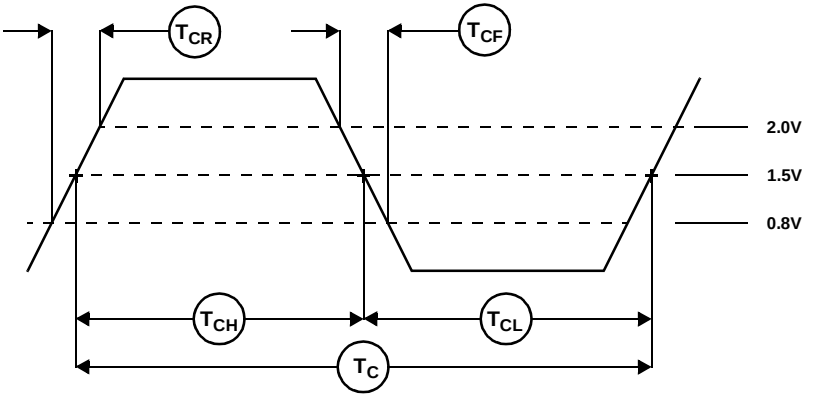


Table 12. 401GF MemClk Timing

Symbol	Parameter	401GF-MC50C2		Units
		Min	Max	
F_C	MemClk clock output frequency	24.975	25.025	MHz
T_C	MemClk clock period	39.96	40.04	ns
T_{CS}	Clock edge stability[1]		± 0.8	ns
T_{CH}	Clock output high time	16		ns
T_{CL}	Clock output low time	16		ns
T_{CR}	Clock output rise time[2]	0.5	2.5	ns
T_{CF}	Clock output fall time[2]	0.5	2.5	ns

Notes:
1. Worst-case clock edge stability is accounted for in the AC I/O timing specification.
2. Rise and fall times measured between 0.8V and 2.0V. Assumes 50 pF capacitive load, V_{DD} = 3.14V and T_J = 85°C

Input Setup and Hold Waveform

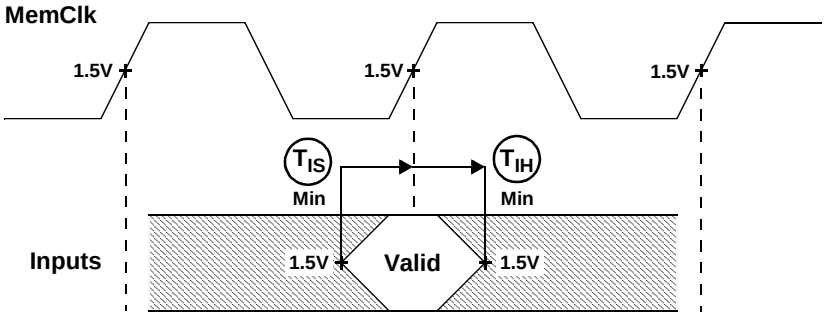


Table 13. 401GF Synchronous Input Timings

Symbol	Parameter		401GF-MC50C2 Min	401GF-MC50C2 Max	Units
T_{IS}	Input setup:				
	T_{IS1}	B0:31	5		ns
	T_{IS2}	$\overline{\text{BusError}}$	8		
	T_{IS3}	HoldReq	5.5		
	T_{IS4}	$\overline{\text{Ready}}$	9		
T_{IH}	Input hold:				
	T_{IH1}	B0:31	1		ns
	T_{IH2}	$\overline{\text{BusError}}$	1		
	T_{IH3}	HoldReq	1		
	T_{IH4}	$\overline{\text{Ready}}$	1		
T_R, T_F	Input rise/fall time		0.5	2.5	ns

Notes:

1. Timings are guaranteed by design and characterization.
2. These I/O timings are valid when the input clock = 25MHz ± 0.1%, the chip is in 2x:1/2x or 1x:1x mode and MemClk Alignment is enabled. When MemClk is not 25MHz, MemClk Alignment should be disabled and the I/O timings should be adjusted by the constants obtained from the "MemClk Output Derating Curves," on page 22. When MemClk Alignment is off, new input setup times (T_{IS}) are derived by adding constant K1 to the setup times in Table 13. $T_{IS(compoff)} = T_{IS} + K1$. When MemClk Alignment is off, new input hold times (T_{IH}) are derived by subtracting constant K2 from the input hold times listed in Table 13. $T_{IH(compoff)} = T_{IH} - K2$.
3. MemClk must be terminated if MemClk Alignment is enabled (IOCR[MCA]=1). See “MemClk Termination” on page 16.

Table 14. 401GF Asynchronous Input Timings

Symbol	Parameter		401GF-MC50C2 Min	401GF-MC50C2 Max	Units
T_{IS}	Input setup time				
	T_{IS10}	CritInt	8		
	T_{IS11}	ExtInt	8		
	T_{IS12}	$\overline{HALT}$	4		ns
	T_{IS13}	$\overline{Reset}$	20		
T_{IH}	Input hold time				
	T_{IH10}	CritInt	Note 2		
	T_{IH11}	ExtInt	Note 2		
	T_{IH12}	$\overline{HALT}$	Note 2		ns
	T_{IH13}	$\overline{Reset}$	Note 3		

Notes:

1. During a system-initiated reset, $\overline{Reset}$ must be taken low for a minimum of one millisecond.
2. External interrupts must be held active until software interrupt handling begins.
3. The BootW input has a maximum rise time requirement of 10 ns when it is tied to $\overline{Reset}$.
4. Input hold times are measured at 3.47V and $T_J = 10^{\circ}C$.
5. These I/O timings are valid when the input clock = 25MHz ± 0.1%, the chip is in 2x:1/2x or 1x:1x mode and MemClk Alignment is enabled. When MemClk is not 25MHz, MemClk Alignment should be disabled and the I/O timings should be adjusted by the constants obtained from the "MemClk Output Derating Curves," on page 22. When MemClk Alignment is off, new input setup times (T_{IS}) are derived by adding constant K1 to the setup times in Table 14. $T_{IS(compoff)} = T_{IS} + K1$. When MemClk Alignment is off, new input hold times (T_{IH}) are derived by subtracting constant K2 from the input hold times listed in Table 14. $T_{IH(compoff)} = T_{IH} - K2$.
6. MemClk must be terminated if MemClk Alignment is enabled (IOCR[MCA]=1). See “MemClk Termination” on page 16.
7. The setup times provided for the asynchronous inputs do not need to be met. If met, two synchronization cycles are used instead of three cycles

Output Delay and Float Timing Waveform

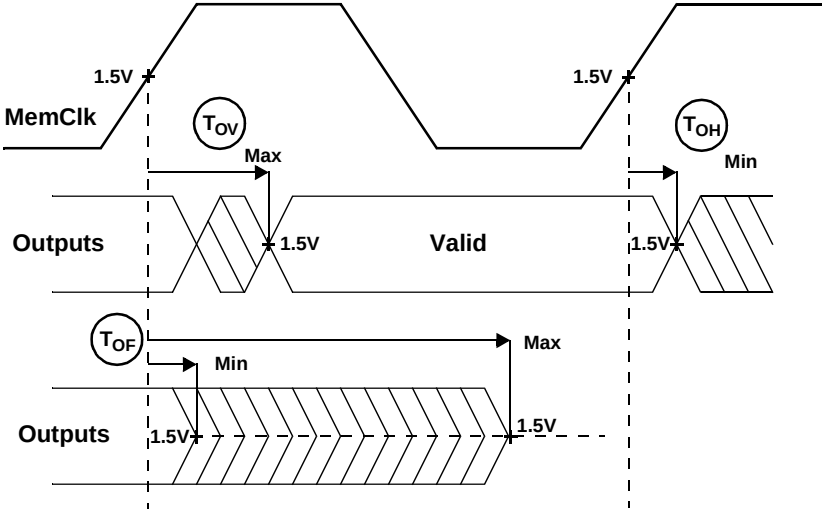


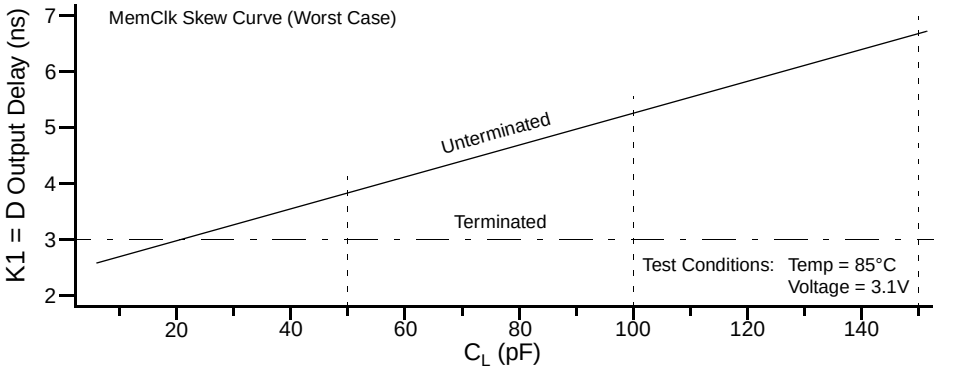
Table 15. 401GF Synchronous Output Timings

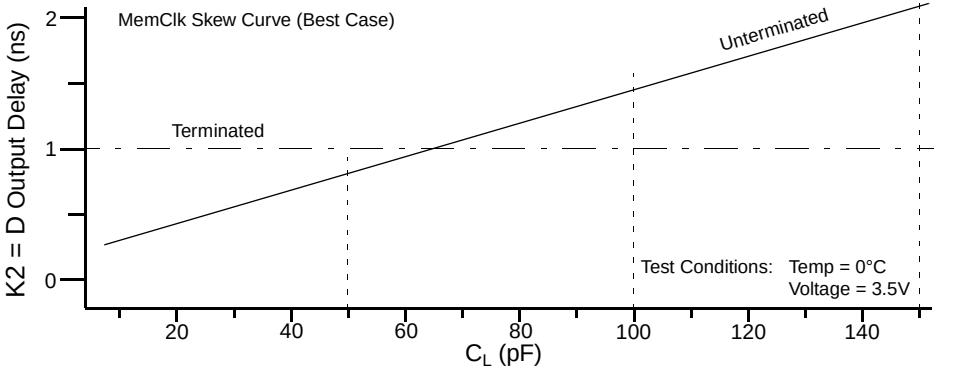
Symbol	Parameter		401GF-MC50C2		Units
T_{OH}, T_{OV}	Output hold, output valid time		T_{OHMin}	T_{OVMax}	
	T_{OH1}, T_{OV1}	ABus28:29	1	10	
	T_{OH2}, T_{OV2}	B0:31	1	12	
	T_{OH3}, T_{OV3}	ALE	1	10	
	T_{OH4}, T_{OV4}	$\overline{\text{BE0[A31]}}$	1	11	
	T_{OH5}, T_{OV5}	$\overline{\text{BE1[A30]}}$	1	11	
	T_{OH6}, T_{OV6}	$\overline{\text{BE2:3}}$	1	11	ns
	T_{OH7}, T_{OV7}	$\overline{\text{BLast}}$	1	11	
	T_{OH8}, T_{OV8}	BusReq	1	11	
	T_{OH9}, T_{OV9}	BusWidth0:1	1	11	
	T_{OH10}, T_{OV10}	HoldAck	1	11	
	T_{OH11}, T_{OV11}	$\overline{\text{Reset}}$	1	12	
	T_{OH12}, T_{OV12}	W/$\overline{\text{R}}$	1	10	
T_{OF}	Output float time		T_{OFMin}	T_{OFMax}	
	T_{OF1}	ABus28:29	1	10	
	T_{OF2}	B0:31	1	10	
	T_{OF3}	ALE	1	10	
	T_{OF4}	$\overline{\text{BE0[A31]}}$	1	10	
	T_{OF5}	$\overline{\text{BE1[A30]}}$	1	10	
	T_{OF6}	$\overline{\text{BE2:3}}$	1	10	ns
	T_{OF7}	$\overline{\text{BLast}}$	1	10	
	T_{OF8}	BusWidth0:1	1	11	
	T_{OF9}	$\overline{\text{Reset}}$	1	9	
	T_{OF10}	W/$\overline{\text{R}}$	1	10	

Notes:

1. ALE T_{OHMin} is with reference to the falling edge of Mem Clock.
2. Refer to the *PowerPC 401GF User's Manual* for detailed information on processor reset and initialization.
3. Output times are measured with a standard 50pF capacitive load, unless otherwise noted. Output hold times are measured at 3.47V and $T_J = 10^{\circ}C$.
4. These I/O timings are valid when the input clock = 25MHz $\pm$ 0.1%, the chip is in 2x:1/2x or 1x:1x mode and MemClk Alignment enabled. When MemClk is not 25MHz, MemClk Alignment should be disabled and the I/O timings should be adjusted by the constants obtained from the "MemClk Output Derating Curves," on page 22. When MemClk Alignment is off, new output valid times (T_{OV}) and new maximum output float times (T_{OFMAX}) are derived by subtracting constant K2 from the values listed in Table 15. $T_{OV(compoff)} = T_{OV} - K1$. $T_{OFMax(compoff)} = T_{OFMax} - K1$. When MemClk Alignment is off new output hold times (T_{OH}) and new minimum output float times (T_{OFMin}) are derived by subtracting constant K1 from the values listed in Table 15. $T_{OH(compoff)} = T_{OH} - K2$. $T_{OFMin(compoff)} = T_{OFMin} - K2$.
5. MemClk must be terminated if MemClk Alignment is enabled (IOCR[MCA]=1). See “MemClk Termination” on page 16.
6. Output hold and float times are guaranteed by design and not tested.
7. T_{OFMax} also represents the amount of time it takes for the drivers to come out of hi-Z state. T_{OFMin} is the amount of hold time the drivers provide when going into the hi-Z state.

MemClk Output Derating Curves





Note:

1. K1 and K2 are independent of loading when using series termination. See “MemClk Termination” on page 16.

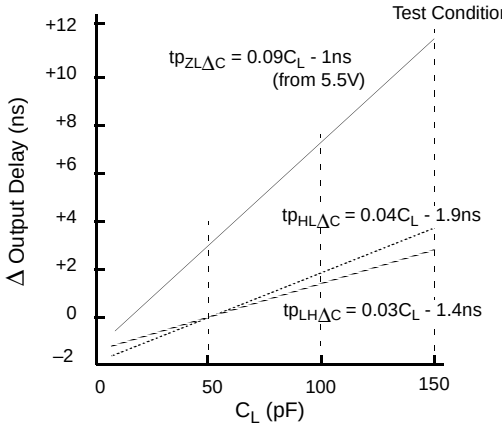
Output Derating for Capacitance and Voltage

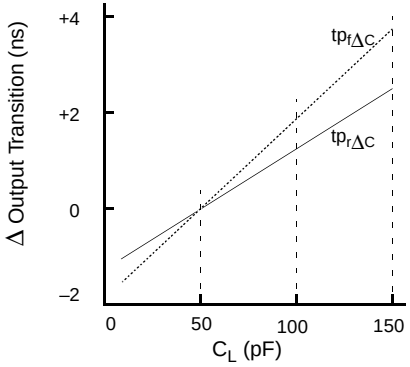
Derating Equations for Output Delays:

1. $\Delta tp_{LH}(C_L, V) = tp_{LH\Delta C} + tp_{LH\Delta V}$
2. $\Delta tp_{HL}(C_L, V) = tp_{HL\Delta C} + tp_{HL\Delta V}$
3. $\Delta tp_{ZL5V}(C_L, V) = tp_{ZL\Delta C} + tp_{HL\Delta V}$

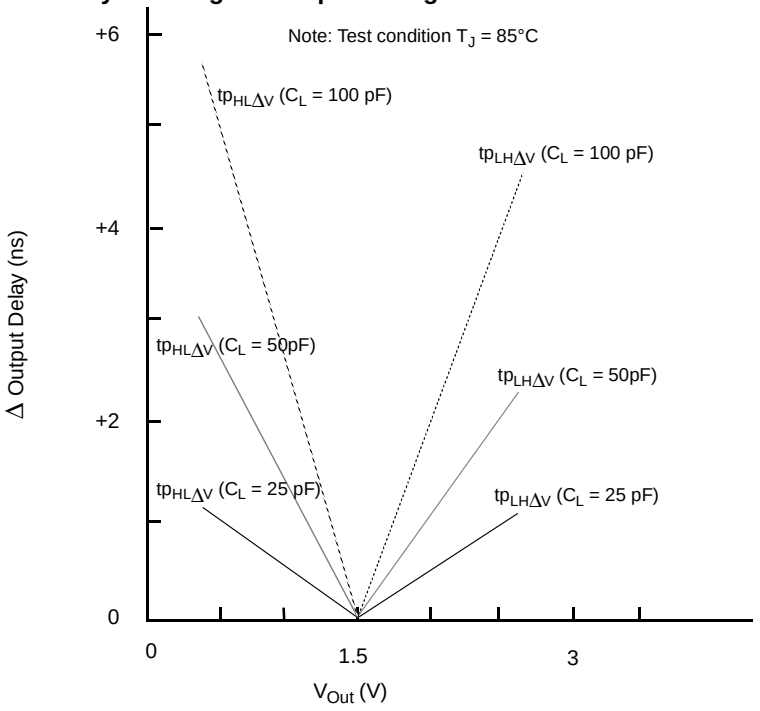
Derating Equations for Output Rise and Fall Times:

4. $t_R(C_L) = 1.5ns + tp_{r\Delta C}$
5. $t_F(C_L) = 2.1ns + tp_{f\Delta C}$





Output Propagation Delay Derating vs. Output Voltage Level



Reset and HoldAck

The following table summarizes the states of signals on output pins when $\overline{\text{Reset}}$ or HoldAck is active.

Table 16. Signal States During Reset or Hold Acknowledge

Signal Names	State When $\overline{\text{Reset}}$ Active	State When HoldAck Active
ABus28:29	Floating	Floating
B0:31	Floating	Floating
ALE	Inactive (low)	Floating
$\overline{\text{BE0}}$[A31]	Inactive (high)	Floating
$\overline{\text{BE1}}$[A30]	Inactive (high)	Floating
$\overline{\text{BE3:2}}$	Inactive (high)	Floating
$\overline{\text{BLast}}$	Inactive (high)	Floating
BusReq	Valid output	Operable (see note 1)
BusWidth0:1	Floating	Floating
HoldAck	Valid output	Active
MemClk	Inactive (high)	Operable (see note 1)
$\overline{\text{Reset}}$	Floating unless initiating system reset	Floating unless initiating system reset
TDO	Floating	Floating
W/$\overline{\text{R}}$	Read (low)	Floating

Note:

1. Signal may be active while HoldAck is asserted, depending on the operation being performed by the 401GF.

BUS WAVEFORMS

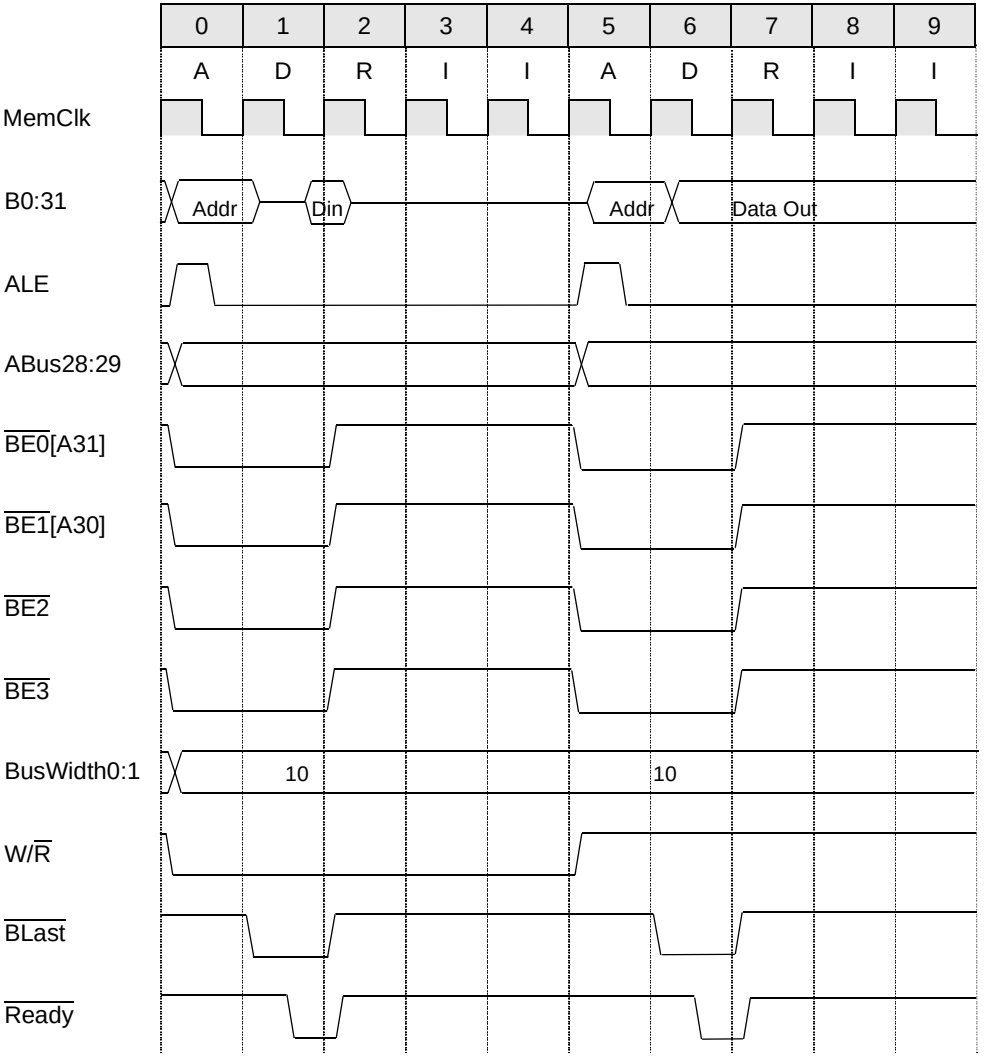
The waveforms in this section represent external bus operations and external master operations.

Nonburst Read and Write Word Transfer (No Wait State, One Recovery State, 32-bit Bus)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **I** = Idle cycle **R** = Recovery cycle

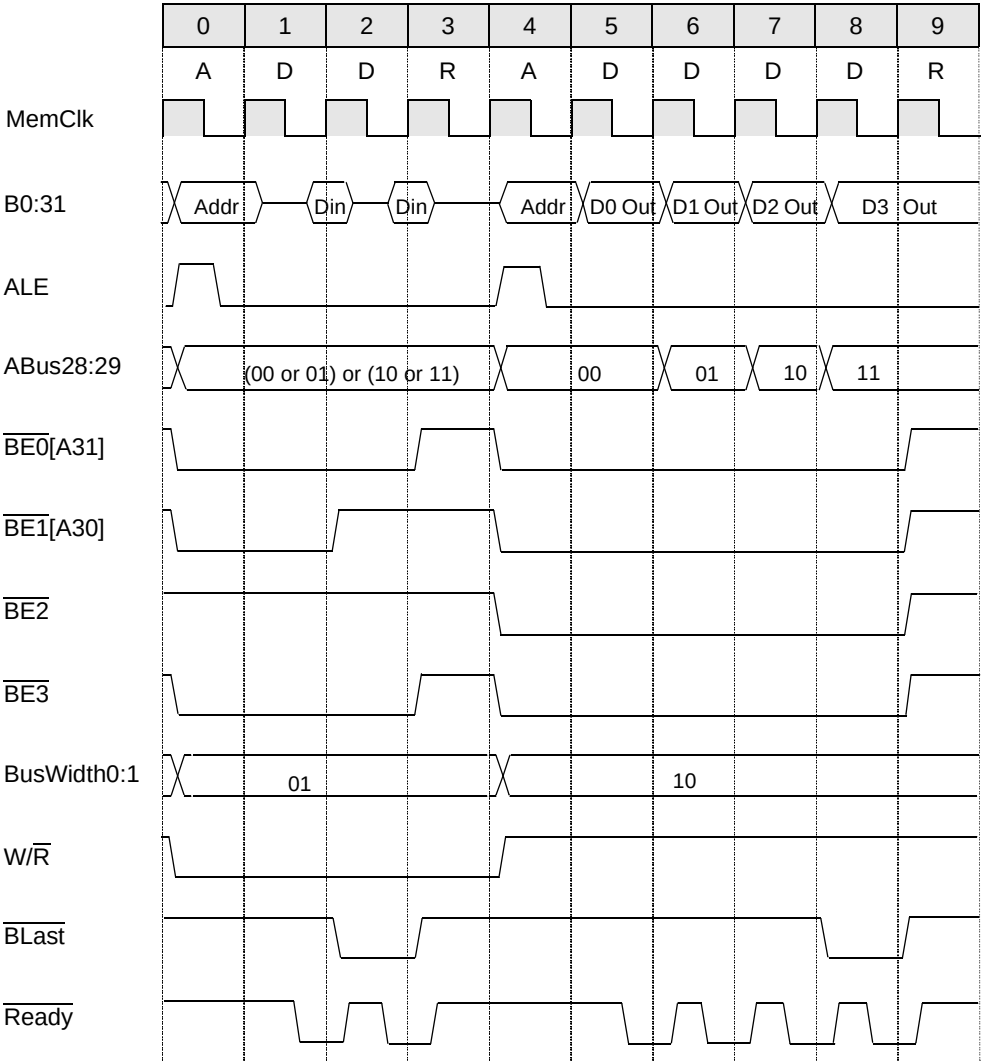
D = Data cycle



Burst Read and Write Line Transfer (No Wait State, One Recovery State)

Cycles in this diagram are labeled according to the following key:

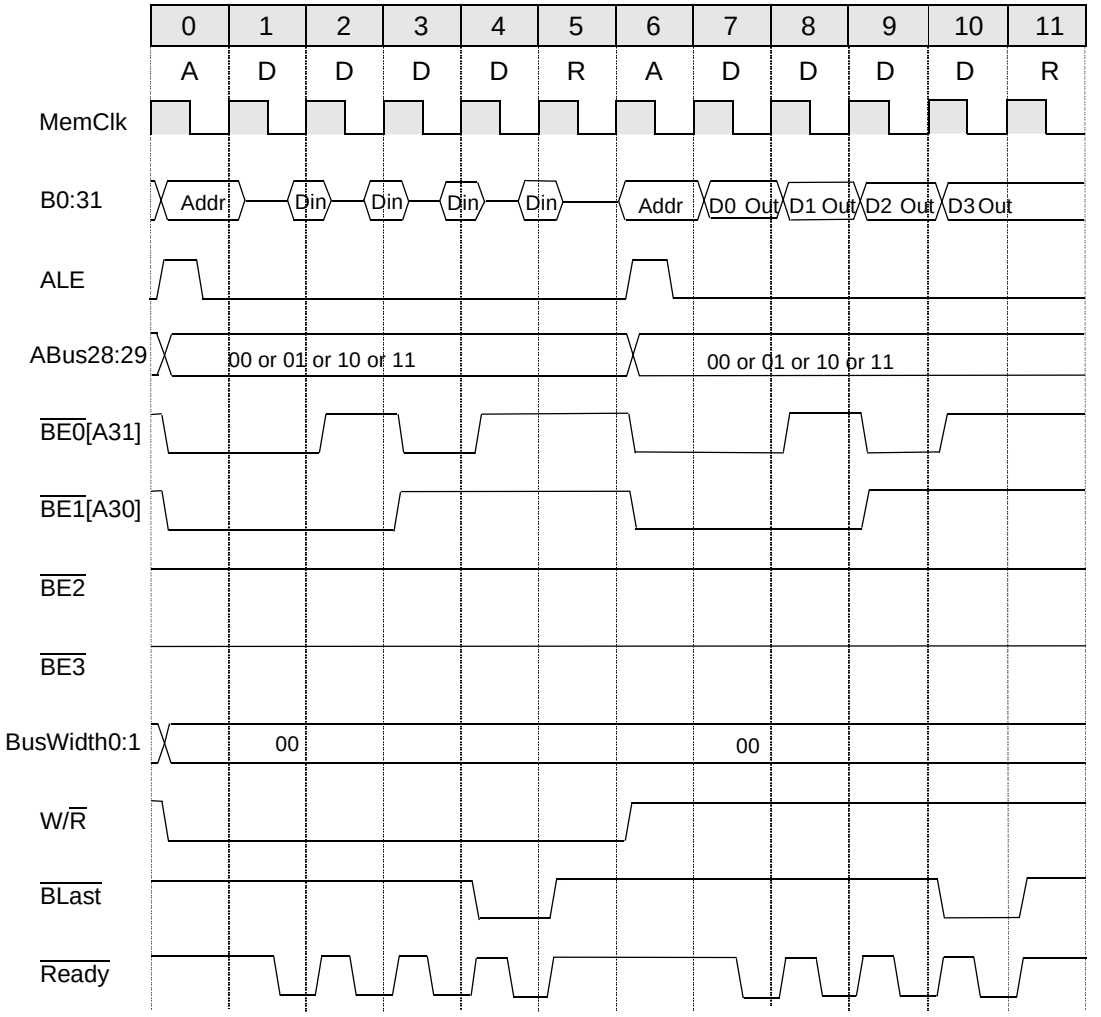
A = Address cycle **D** = Data cycle **R** = Recovery cycle



Four Beat Burst Read and Write Transfer (No Wait State, One Recovery State, 8-bit Bus)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **D** = Data cycle **R** = Recovery cycle

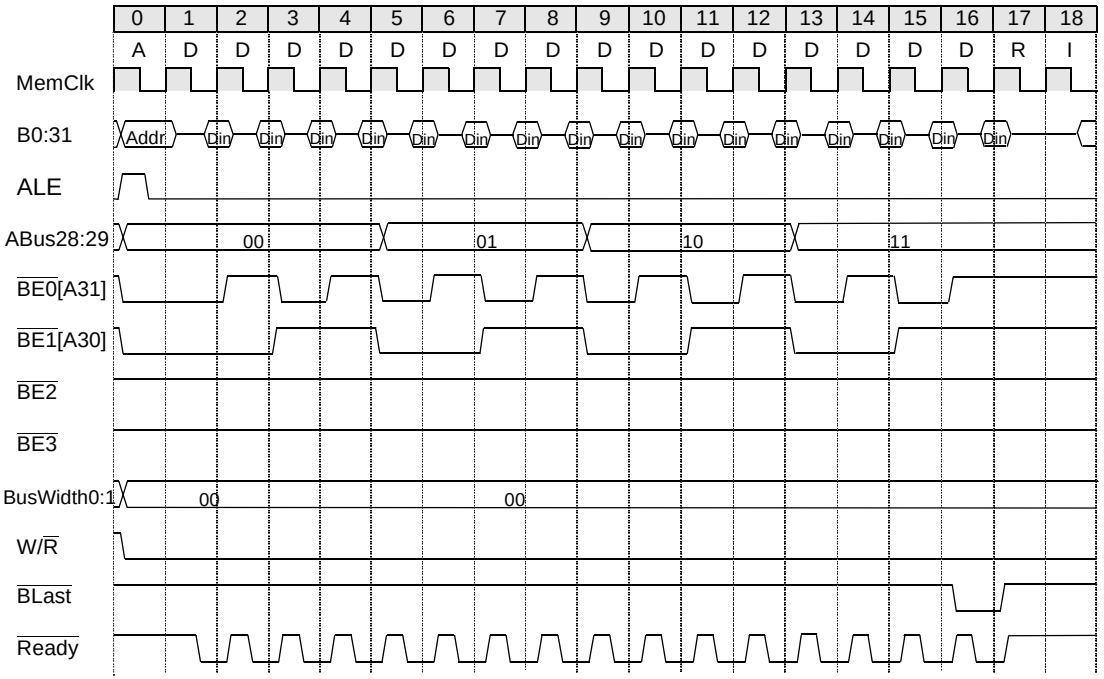


Continuous Burst Read Transfer (No Wait State, One Recovery State, 8-bit Bus)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **I** = Idle cycle **R** = Recovery cycle

D = Data cycle

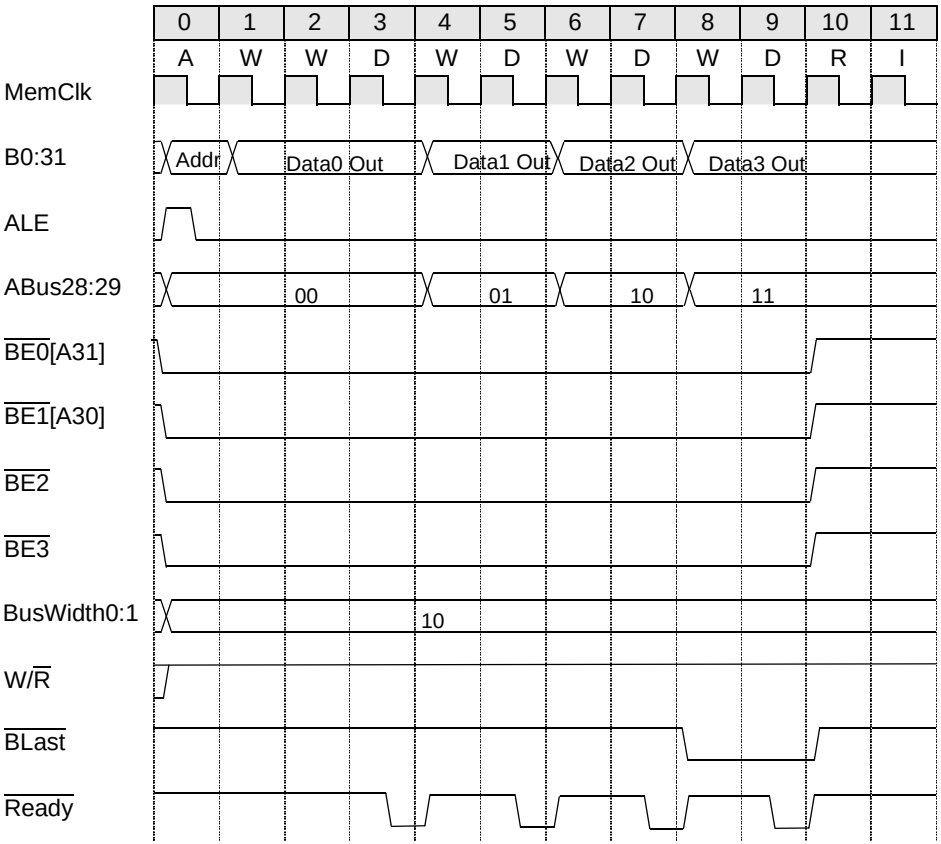


Burst Write Transfer (2-1-1-1 Wait State, One Recovery State, 32-bit Bus)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **I** = Idle cycle **W** = Wait cycle

D = Data cycle **R** = Recovery cycle

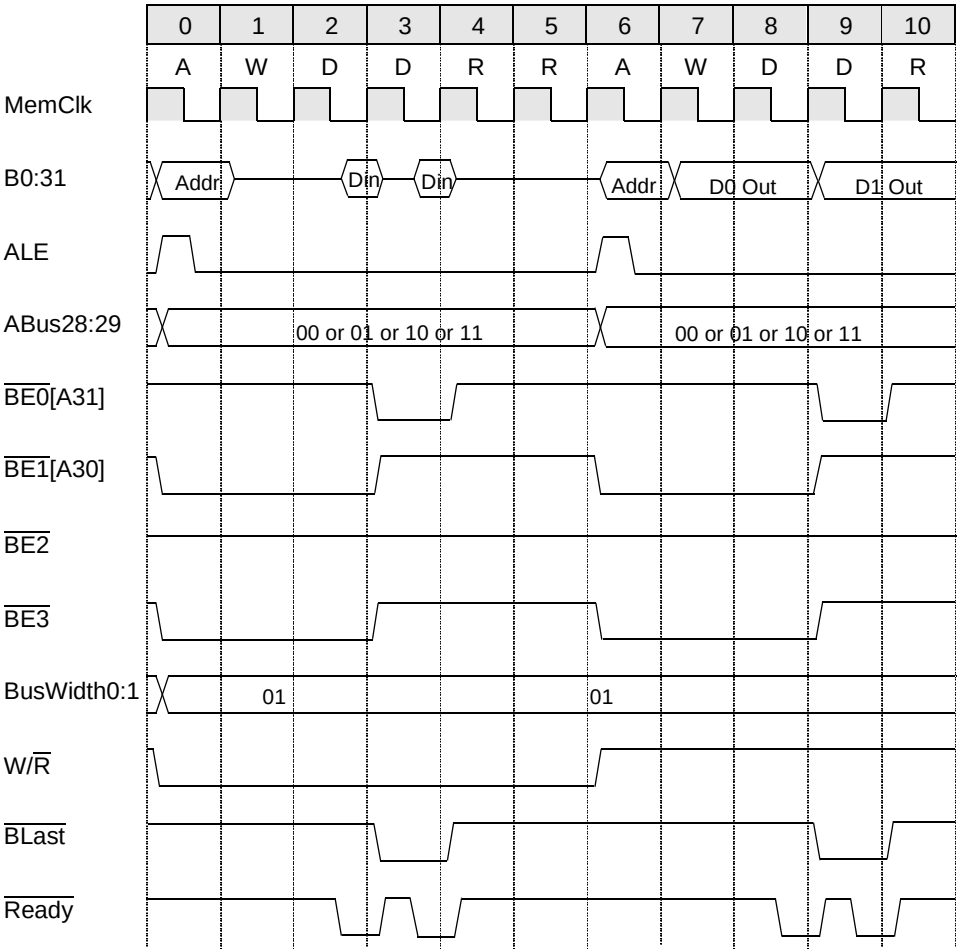


Burst Read/Write Unaligned HW Transfer (1-0 Wait State; 2 Recovery State; 16-bit Bus)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **R** = Recovery cycle **W** = Wait cycle

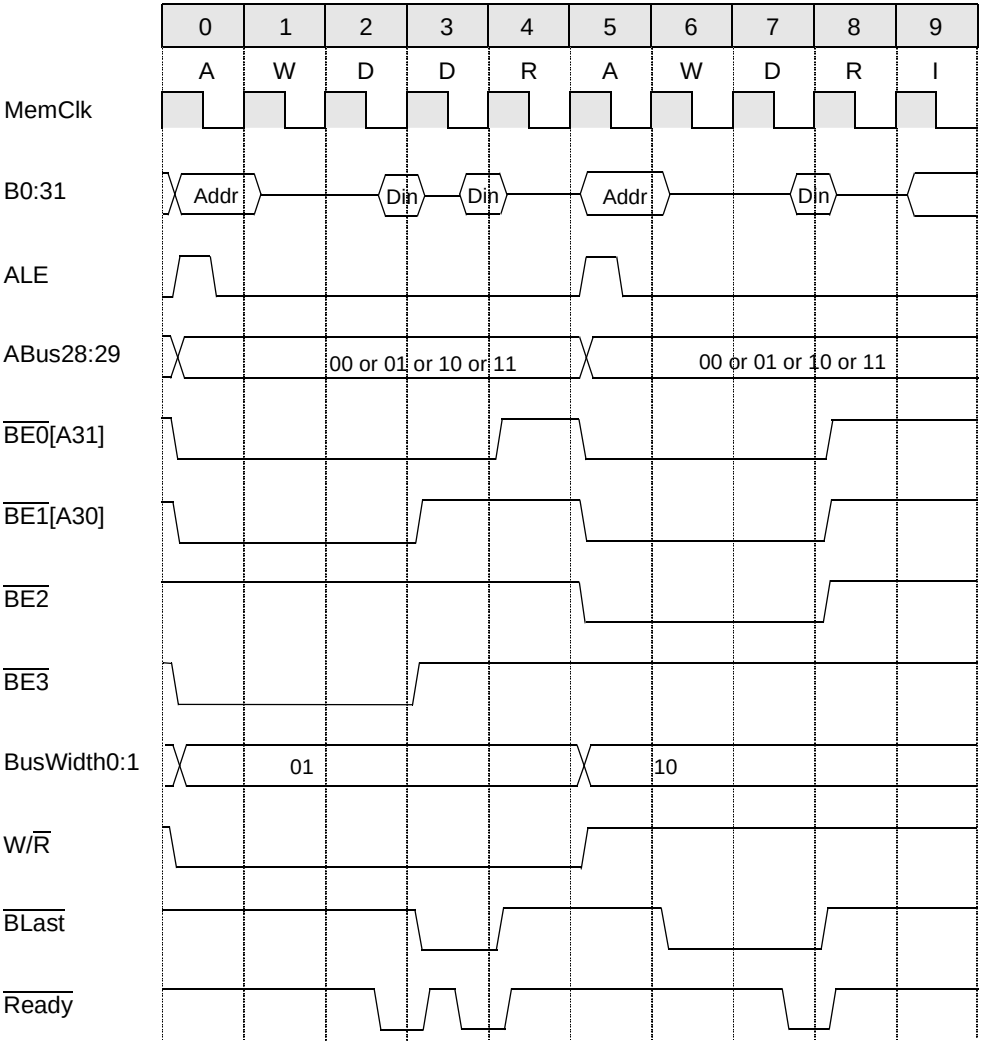
D = Data cycle



3-Byte Transfer Bus Request Starting At Word Address (1-0 Wait State, 1 Recovery State)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **I** = Idle cycle **W** = Wait cycle
D = Data cycle **R** = Recovery cycle

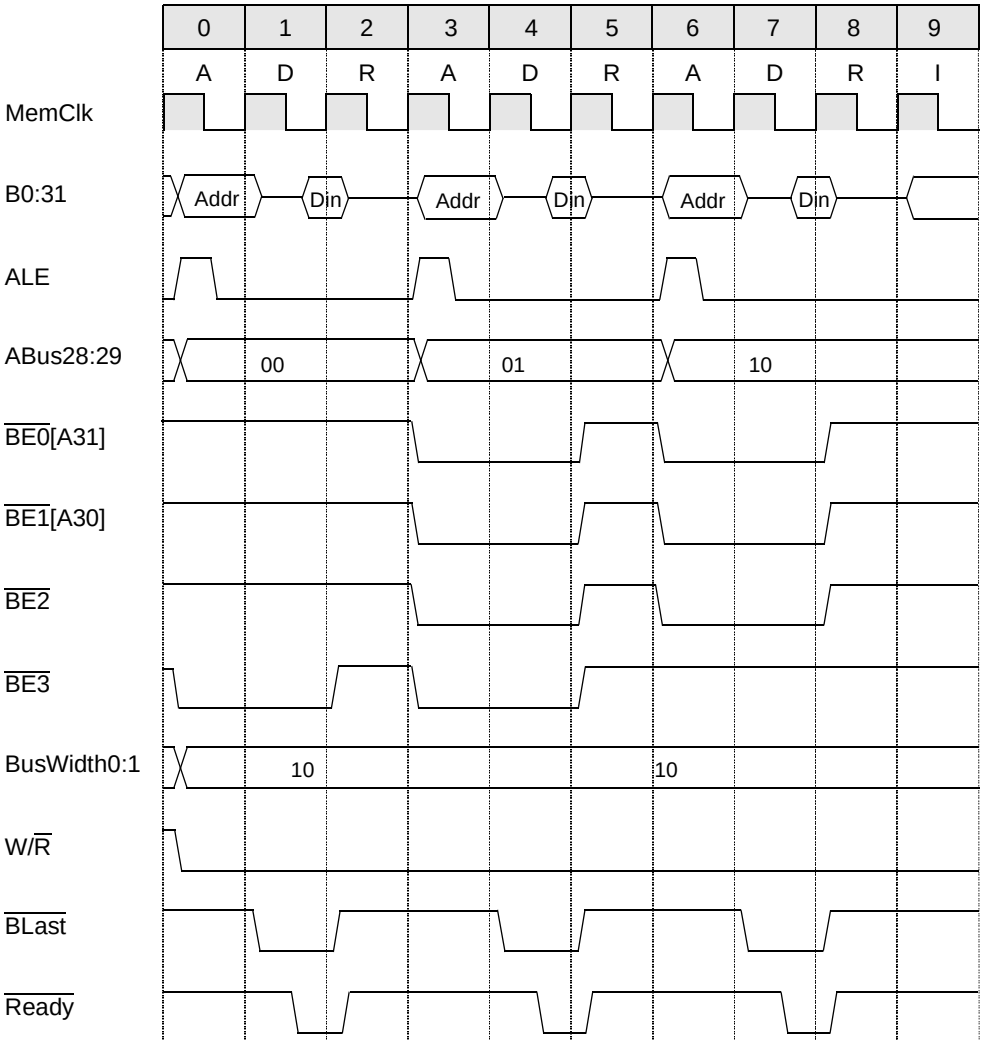


Unaligned Transfer Read Bus Request, Cross Word Boundary (No Wait State, 1 Recovery State, 32-bit Bus)

Cycles in this diagram are labeled according to the following key:

A = Address cycle **I** = Idle cycle **R** = Recovery cycle

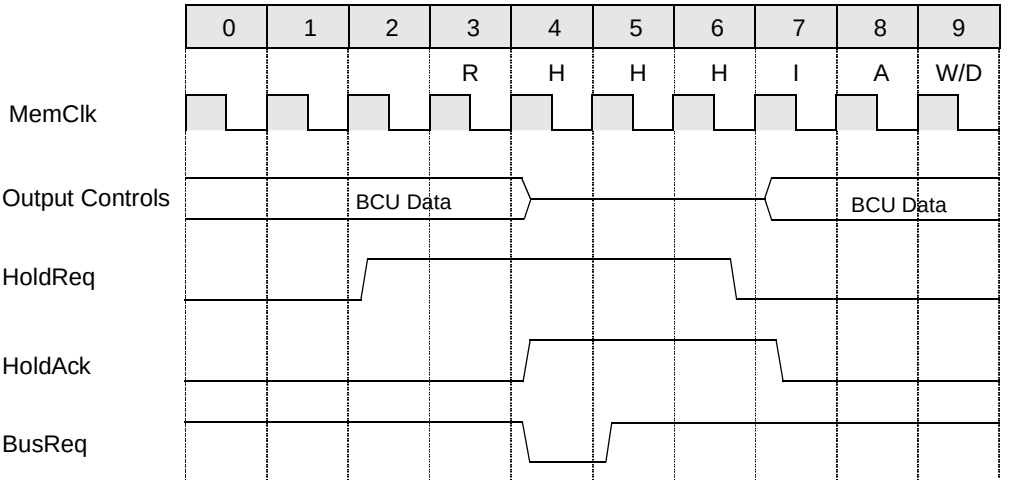
D = Data cycle



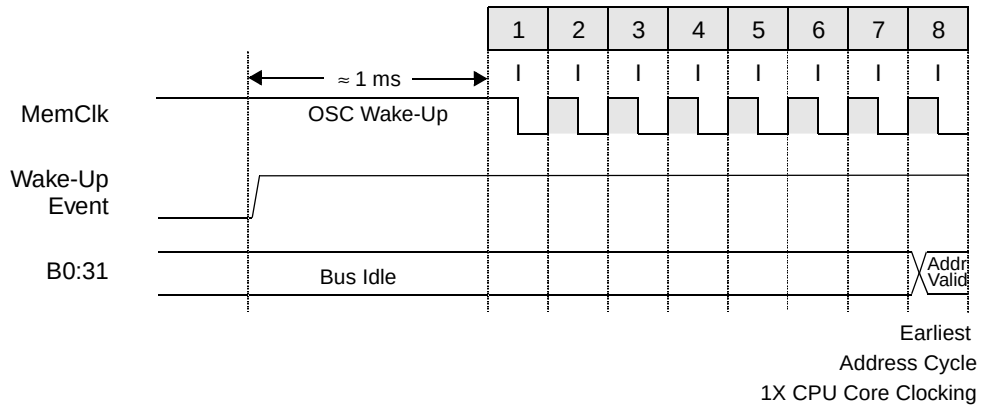
External Master Protocol

Cycles in these diagrams are labeled according to the following key:

A = Address cycle **H** = External master hold **R** = Recovery cycle
D = Data cycle **I** = Idle cycle **W** = Wait cycle



Wake-Up Timing

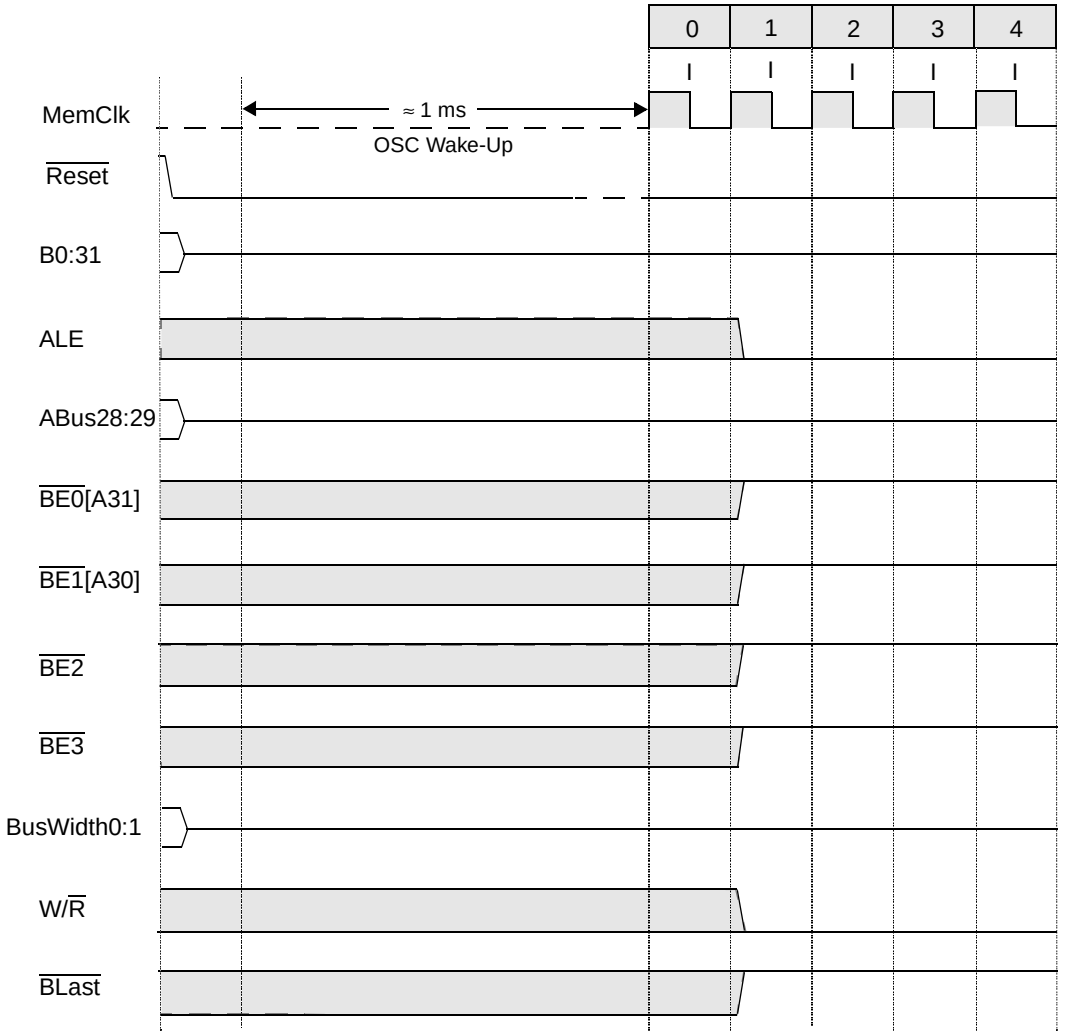


Wake-up events: External interrupt, Critical interrupt, Hold, Reset, Halt

Power-On Reset

Cycles in this diagram are labeled according to the following key:

I = Idle cycle



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