DATA SHEET

XA-S3

XA 16-bit microcontroller

32K/1K OTP/ROM/ROMless, 8-channel 8-bit A/D, low voltage (2.7V–5.5V), I^2C, 2 UARTs, 16MB address range

Objective specification
Supersedes data of 1998 Aug 21
IC25 Data Handbook

1998 Oct 06

Philips
Semiconductors

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GENERAL DESCRIPTION

The XA-S3 device is a member of Philips Semiconductors' XA (eXtended Architecture) family of high performance 16-bit single-chip microcontrollers.

The XA-S3 device combines many powerful peripherals on one chip. With its high performance A/D converter, timers/counters, watchdog, Programmable Counter Array (PCA), I^2C interface, dual UARTs, and multiple general purpose I/O ports, it is suited for general multipurpose high performance embedded control functions.

Specific features of the XA-S3

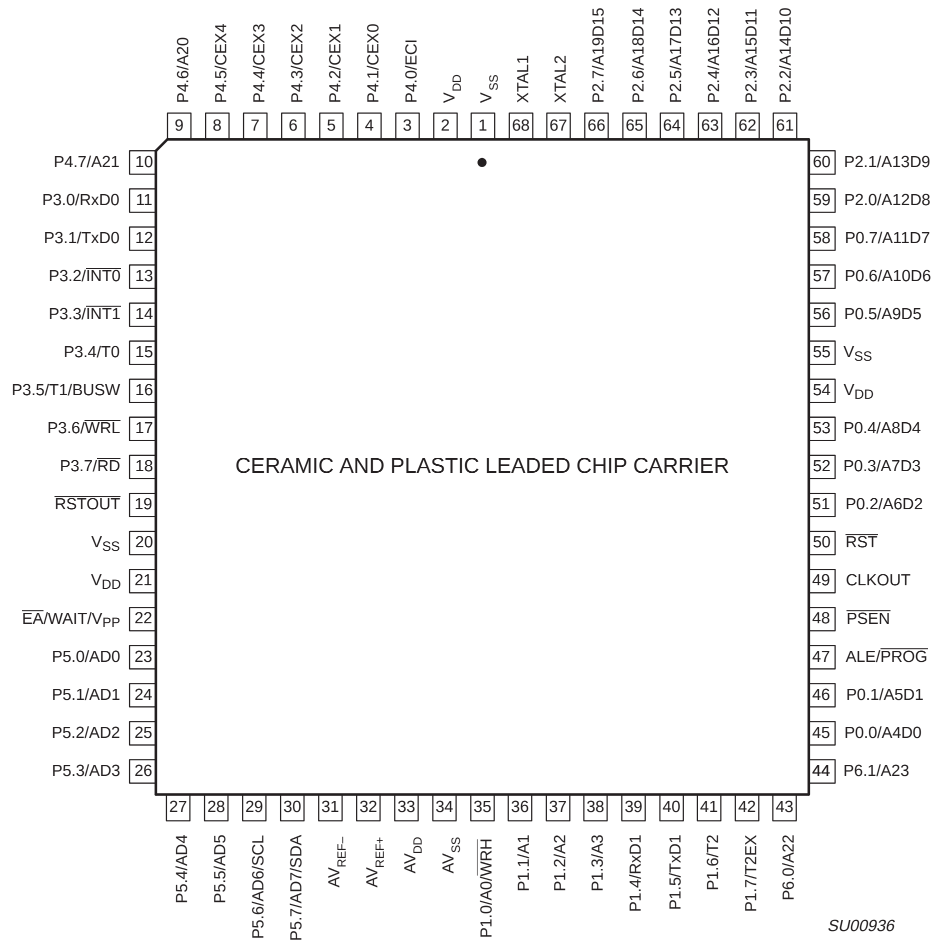
- 2.7 V to 5.5 V operation.
- 32K bytes of on-chip EPROM/ROM program memory.
- 1024 bytes of on-chip data RAM.
- Supports off-chip addressing up to 16 megabytes (24 address lines). A clock output reference is added to simplify external bus interfacing.
- High performance 8-channel 8-bit A/D converter with automatic channel scan and repeated read functions. Completes a conversion in 4.46 microseconds at 30 MHz.
- Three standard counter/timers with enhanced features. All timers have a toggle output capability.
- Watchdog timer.
- 5-channel 16-bit Programmable Counter Array (PCA).
- I^2C-bus serial I/O port with byte-oriented master and slave functions.
- Two enhanced UARTs with independent baud rates.
- Seven software interrupts.
- Active low reset output pin indicates all reset occurrences (external reset, watchdog reset and the RESET instruction). A reset source register allows program determination of the cause of the most recent reset.
- 50 I/O pins, each with 4 programmable output configurations.
- 30 MHz operating frequency at 2.7–5.5V V_{DD} over commercial operating conditions.
- Power saving operating modes: Idle and Power-down. Wake-up from power-down via an external interrupt is supported.
- 68-pin PLCC and 80-pin PQFP packages.

ORDERING INFORMATION

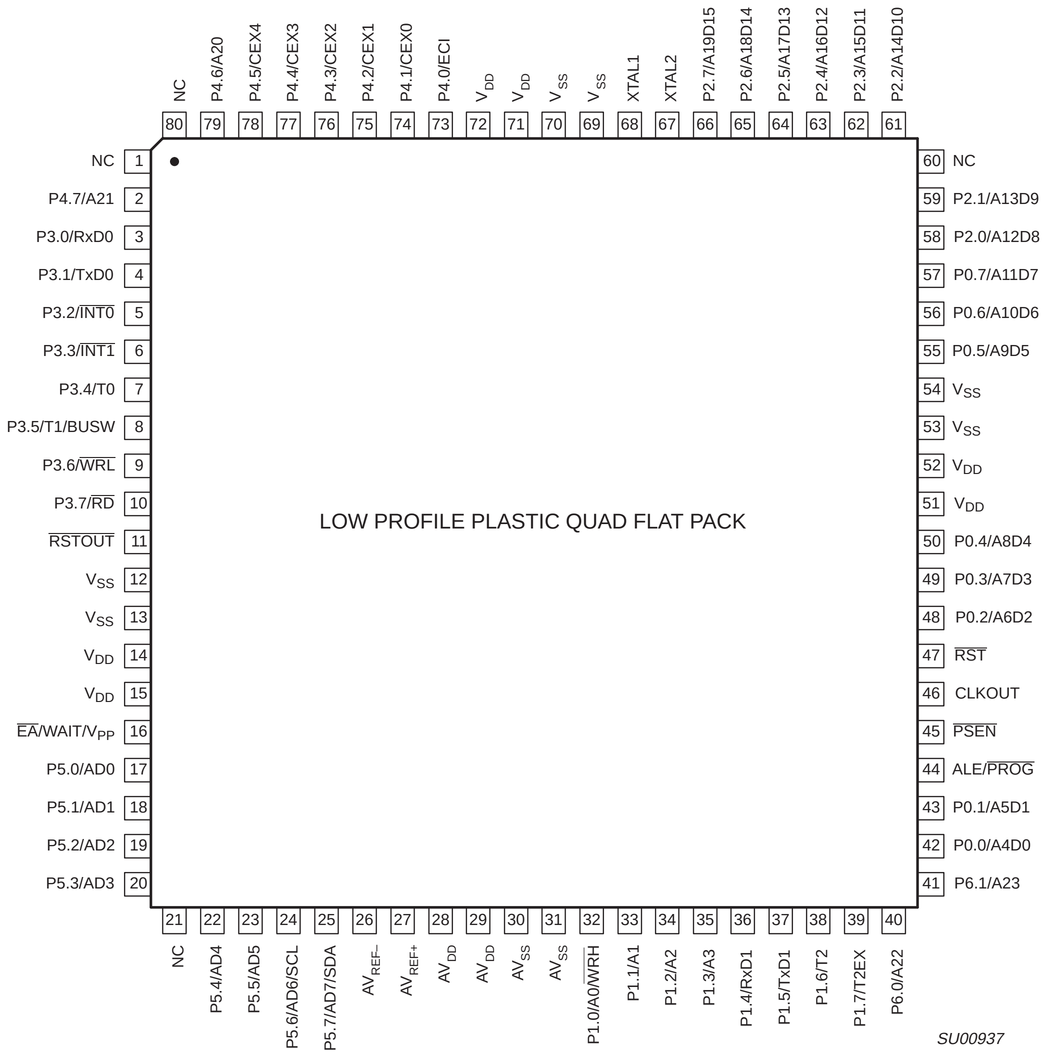
ROMless	ROM	EPROM		TEMPERATURE RANGE (°C) AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
PXAS30KBBA	PXAS33KBBA	PXAS37KBBA	OTP	0 to +70, 68-pin Plastic Leaded Chip Carrier	30	SOT188-3
PXAS30KBBD	PXAS33KBBD	PXAS37KBBE	OTP	0 to +70, 80-pin Plastic Quad Flat Pack	30	SOT315-1

PIN CONFIGURATIONS

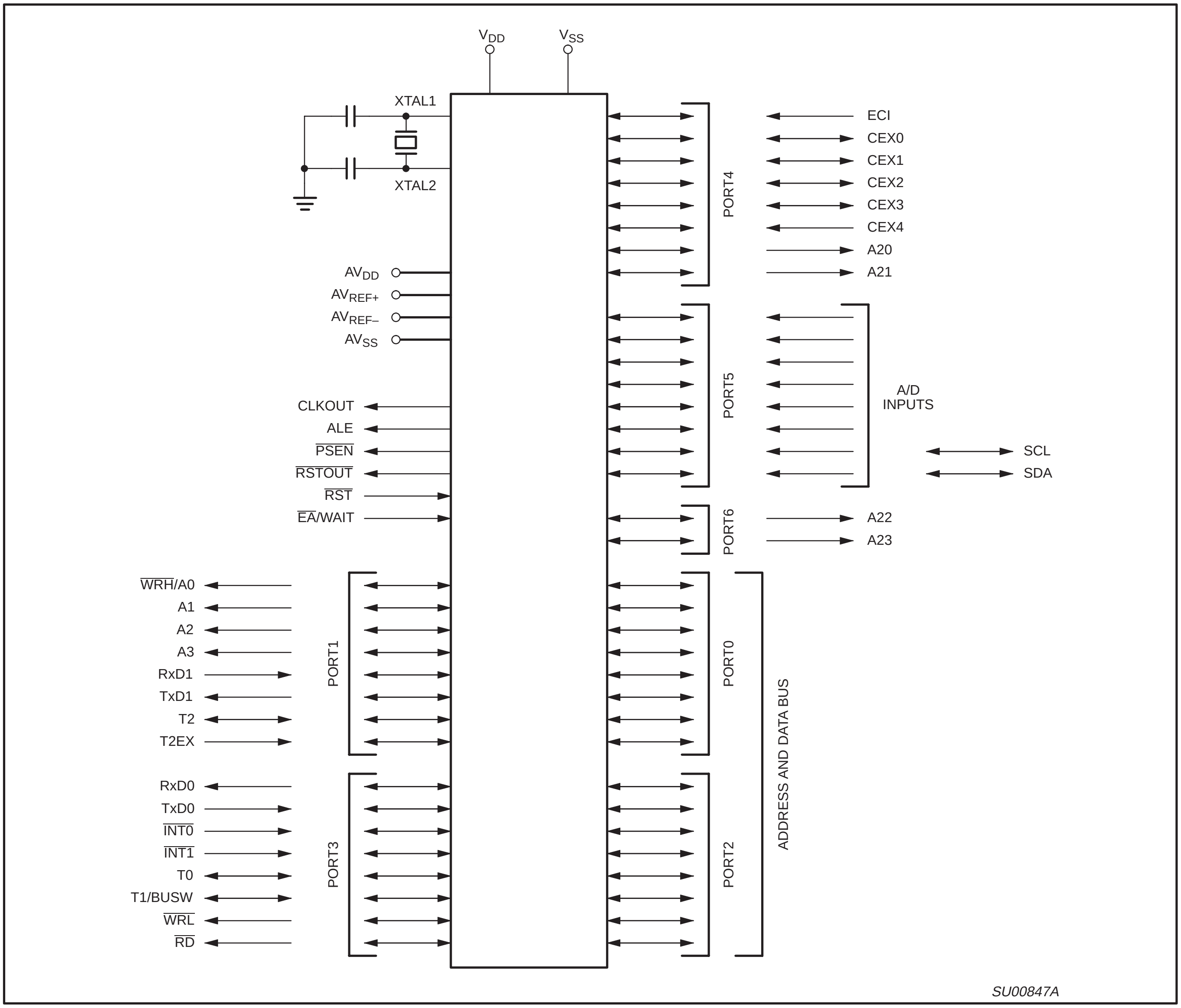
68-pin PLCC package



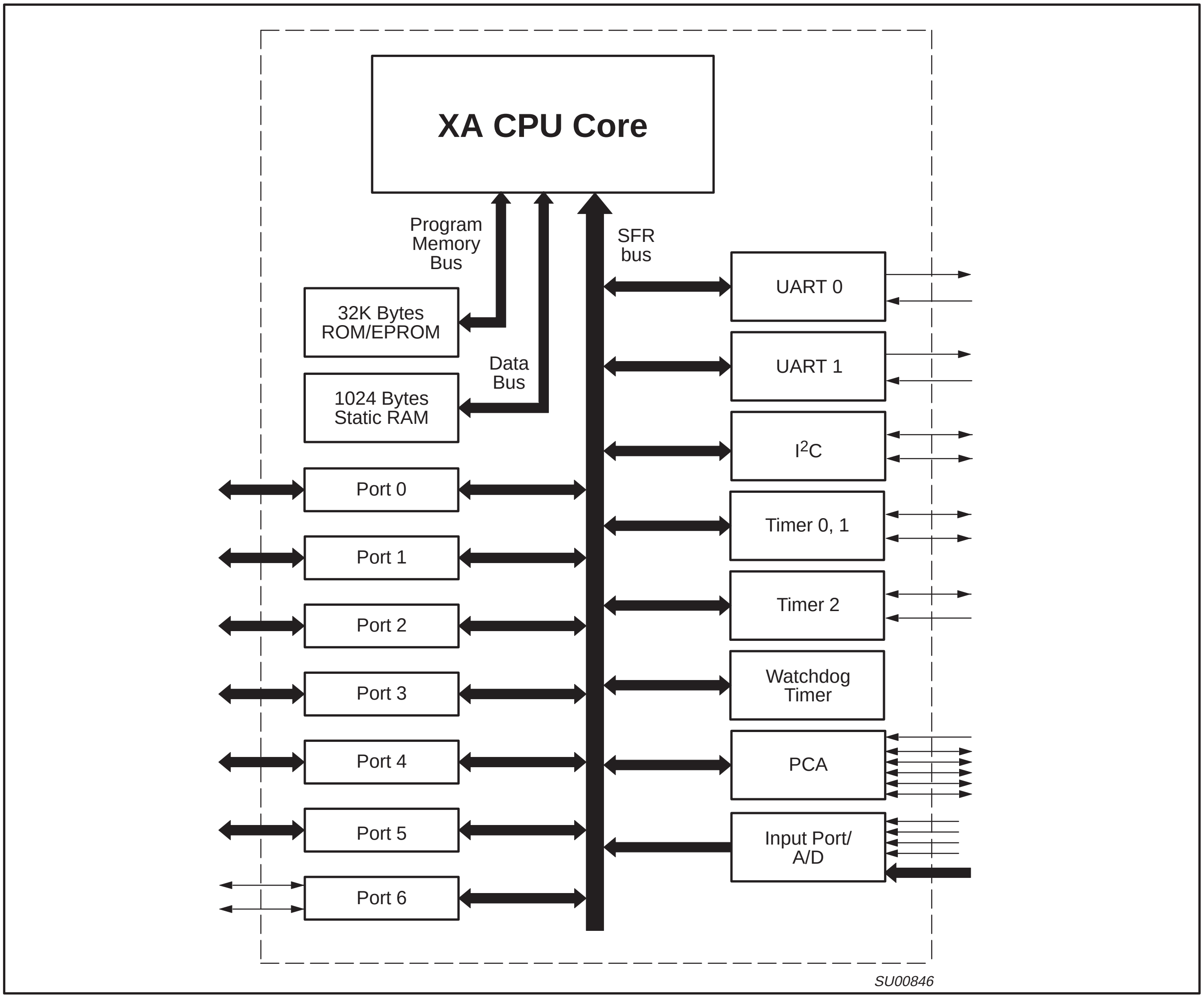
80-pin LQFP package



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER		TYPE	NAME AND FUNCTION
	PLCC	LQFP		
V_{SS}	1, 20, 55	12, 13, 53, 54, 69, 70	I	**Ground:** 0V reference.
V_{DD}	2, 21, 54	14, 15, 51, 52, 71, 72	I	**Power Supply:** This is the power supply voltage for normal, idle, and power down operation.
$\overline{RST}$	50	47	I	**Reset:** A low on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor to begin execution at the address contained in the reset vector.
$\overline{RSTOUT}$	19	11	O	**Reset Output:** This pin outputs a low whenever the XA-S3 processor is reset for any reason. This includes an external reset via the $\overline{RST}$ pin, watchdog reset, and the $\overline{RESET}$ instruction.
ALE/$\overline{PROG}$	47	44	I/O	**Address Latch Enable/Program Pulse:** A high output on the ALE pin signals external circuitry to latch the address portion of the multiplexed address/data bus. A pulse on ALE occurs only when it is needed in order to process a bus cycle.
$\overline{PSEN}$	48	45	O	**Program Store Enable:** The read strobe for external program memory. When the microcontroller accesses external program memory, $\overline{PSEN}$ is driven low in order to enable memory devices. $\overline{PSEN}$ is only active when external code accesses are performed.
$\overline{EA}$/WAIT/V_{PP}	22	16	I	**External Access/Bus Wait:** The $\overline{EA}$ input determines whether the internal program memory of the microcontroller is used for code execution. The value on the $\overline{EA}$ pin is latched as the external reset input is released and applies during later execution. When latched as a 0, external program memory is used exclusively. When latched as a 1, internal program memory will be used up to its limit, and external program memory used above that point. After reset is released, this pin takes on the function of bus WAIT input. If WAIT is asserted high during an external bus access, that cycle will be extended until WAIT is released.
XTAL1	68	68	I	**Crystal 1:** Input to the inverting amplifier used in the oscillator circuit and input to the internal clock generator circuits.
XTAL2	67	67	I	**Crystal 2:** Output from the oscillator amplifier.
CLKOUT	49	46	O	**Clock Output:** This pin outputs a buffered version of the internal CPU clock. The clock output may be used in conjunction with the external bus to synchronize WAIT state generators, etc. The clock output may be disabled by software.
AV_{DD}	33	28, 29	I	**Analog Power Supply:** Positive power supply input for the A/D converter.
AV_{SS}	34	30, 31	I	**Analog Ground.**
AV_{REF+}	32	27	I	**A/D Positive Reference Voltage:** High end reference for the A/D converter.
AV_{REF-}	31	26	I	**A/D Negative Reference Voltage:** Low end reference for the A/D converter.
P0.0 – P0.7	45, 46, 51–53, 56–58	42, 43, 48–50, 55–57	I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. Port 0 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. When the external program/data bus is used, Port 0 becomes the multiplexed low data/instruction byte and address lines 4 through 11.

MNEMONIC	PIN NUMBER PLCC	PIN NUMBER LQFP	TYPE	NAME AND FUNCTION
P1.0 – P1.7	35–42	32–39	I/O	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type. Port 1 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of port 1 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 1 also provides various special functions as described below:
	35	32	O	**A0/$\overline{\text{WRH}}$ (P1.0)** Address bit 0 of the external address bus when the eternal data bus is configured for an 8-bit width. When the external data bus is configured for a 16-bit width, this pin becomes the high byte write strobe.
	36	33	O	**A1 (P1.1):** Address bit 1 of the external address bus.
	37	34	O	**A2 (P1.2):** Address bit 2 of the external address bus.
	38	35	O	**A3 (P1.3):** Address bit 3 of the external address bus.
	39	36	I	**RxD1 (P1.4):** Serial port 1 receiver input.
	40	37	O	**TxD1 (P1.5):** Serial port 1 transmitter output.
	41	38	I/O	**T2 (P1.6):** Timer/counter 2 external count input or overflow output.
	42	39	O	**T2EX (P1.7):** Timer/counter 2 reload/capture/direction control.
P2.0 – P2.7	59–66	58, 59, 61–66	I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. Port 2 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. When the external program/data bus is used in 16-bit mode, Port 2 becomes the multiplexed high data/instruction byte and address lines 12 through 19. When the external data/address bus is used in 8-bit mode, the number of address lines that appear on Port 2 is user programmable in groups of 4 bits.
P3.0 – P3.7	11–18	3–10	I/O	**Port 3:** Port 3 is an 8-bit I/O port with a user-configurable output type. Port 3 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 3 also provides the various special functions as described below:
	11	3	I	**RxD0 (P3.0):** Receiver input for serial port 0.
	12	4	O	**TxD0 (P3.1):** Transmitter output for serial port 0.
	13	5	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0 input.
	14	6	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1 input.
	15	7	I/O	**T0 (P3.4):** Timer/counter 0 external count input or overflow output.
	16	8	I/O	**T1 / BUSW (P3.5):** Timer/counter 1 external count input or overflow output. The value on this pin is latched as an external chip reset is completed and defines the default external data bus width.
	17	9	O	**$\overline{\text{WRL}}$ (P3.6):** External data memory low byte write strobe.
	18	10	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe.
P4.0 – P4.7	3–10	73–79, 2	I/O	**Port 4:** Port 4 is an 8-bit I/O port with a user-configurable output type. Port 4 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of Port 4 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 4 also provides various special functions as described below:
	3	73	I	**ECI (P4.0):** PCA External clock input.
	4	74	I/O	**CEX0 (P4.1):** Capture/compare external I/O for PCA module 0.
	5	75	I/O	**CEX1 (P4.2):** Capture/compare external I/O for PCA module 1.
	6	76	I/O	**CEX2 (P4.3):** Capture/compare external I/O for PCA module 2.
	7	77	I/O	**CEX3 (P4.4):** Capture/compare external I/O for PCA module 3.
	8	78	I/O	**CEX4 (P4.5):** Capture/compare external I/O for PCA module 4.
	9	79	O	**A20 (P4.6):** Address bit 20 of the external address bus.
	10	2	O	**A21 (P4.7):** Address bit 21 of the external address bus.

MNEMONIC	PIN NUMBER		TYPE	NAME AND FUNCTION	
	PLCC	LQFP			
P5.0 – P5.7	23–30	17–20, 22–25	I/O	**Port 5:** Port 5 is an 8-bit I/O port with a user-configurable output type. Port 5 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of Port 5 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 5 also provides various special functions as described below. Port 5 pins used as A/D inputs must be configured by the user to the high impedance mode.	
	23	17	I	**AD0 (P5.0):**	A/D channel 0 input.
	24	18	I	**AD1 (P5.1):**	A/D channel 1 input.
	25	19	I	**AD2 (P5.2):**	A/D channel 2 input.
	26	20	I	**AD3 (P5.3):**	A/D channel 3 input.
	27	22	I	**AD4 (P5.4):**	A/D channel 4 input.
	28	23	I	**AD5 (P5.5):**	A/D channel 5 input.
	29	24	I/O	**AD6/SCL (P5.6):**	A/D channel 6 input. I²C serial clock input/output.
	30	25	I/O	**AD7/SDA (P5.7):**	A/D channel 7 input. I²C serial data input/output.
P6.0 – P6.7	43, 44	40, 41	I/O	**Port 6:** Port 6 is a 2-bit I/O port with a user-configurable output type. Port 6 latches have 1s written to them and are configured in the quasi-bidirectional mode during reset. The operation of Port 6 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 6 also provides special functions as described below:	
	43	40	O	**A22 (P6.0):**	Address bit 22 of the external address bus.
	44	41	O	**A23 (P6.1):**	Address bit 23 of the external address bus.

Table 1. Special Function Registers

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	Reset Value
			3F7	3F6	3F5	3F4	3F3	3F2	3F1	3F0	
ADCON#*	A/D control register	43E	–	–	–	–	–	ADMOD	ADSST	ADINT	00h
			3FF	3FE	3FD	3FC	3FB	3FA	3F9	3F8	
ADCS#*	A/D channel select register	43F	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	00h
ADCFG#	A/D timing configuration	4B9	–	–	–	–	A/D Timing Configuration				0Fh
ADRSH0#	A/D high byte result, channel 0	4B0									xx
ADRSH1#	A/D high byte result, channel 1	4B1									xx
ADRSH2#	A/D high byte result, channel 2	4B2									xx
ADRSH3#	A/D high byte result, channel 3	4B3									xx
ADRSH4#	A/D high byte result, channel 4	4B4									xx
ADRSH5#	A/D high byte result, channel 5	4B5									xx
ADRSH6#	A/D high byte result, channel 6	4B6									xx
ADRSH7#	A/D high byte result, channel 7	4B7									xx
BCR#	Bus configuration register	46A	–	–	CLKD	WAITD	BUSD	BC2	BC1	BC0	Note 1
BTRH	Bus timing register high byte	469	DW1	DW0	DWA1	DWA0	DR1	DR0	DRA1	DRA0	FFh
BTRL	Bus timing register low byte	468	WM1	WM0	ALEW	–	CR1	CR0	CRA1	CRA0	EFh

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	Reset Value
			2D7	2D6	2D5	2D4	2D3	2D2	2D1	2D0	
CCON#*	PCA counter control	41A	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	00h
CMOD#	PCA mode control	490	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00h
CH#	PCA counter high byte	48B									00h
CL#	PCA counter low byte	48A									00h
CCAPM0#	PCA module 0 mode	491	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	00h
CCAPM1#	PCA module 1 mode	492	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	00h
CCAPM2#	PCA module 2 mode	493	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	00h
CCAPM3#	PCA module 3 mode	494	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	00h
CCAPM4#	PCA module 4 mode	495	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	00h
CCAP0H#	PCA module 0 capture high byte	497									xx
CCAP1H#	PCA module 1 capture high byte	499									xx
CCAP2H#	PCA module 2 capture high byte	49B									xx
CCAP3H#	PCA module 3 capture high byte	49D									xx
CCAP4H#	PCA module 4 capture high byte	49F									xx
CCAP0L#	PCA module 0 capture low byte	496									xx
CCAP1L#	PCA module 1 capture low byte	498									xx
CCAP2L#	PCA module 2 capture low byte	49A									xx
CCAP3L#	PCA module 3 capture low byte	49C									xx
CCAP4L#	PCA module 4 capture low byte	49E									xx
CS	Code segment	443									00h
DS	Data segment	441									00h
ES	Extra segment	442									00h
			367	366	365	364	363	362	361	360	
I2CON#*	I^2C control register	42C	CR2	ENA	STA	STO	SI	AA	CR1	CR0	00h
I2STAT#	I^2C status register	46C	I^2C Status Code/Vector					0	0	0	F8h
I2DAT#	I^2C data register	46D									xx
I2ADDR#	I^2C address register	46E	I^2C Slave Address							GC	00h
			33F	33E	33D	33C	33B	33A	339	338	
IEH*	Interrupt enable high byte	427	–	–	–	–	ETI1	ERI1	ETI0	ERI0	00h
			337	336	335	334	333	332	331	330	
IEL#*	Interrupt enable low byte	426	EA	EAD	EPC	ET2	ET1	EX1	ET0	EX0	00h
			377	376	375	374	373	372	371	370	
IELB#*	Interrupt enable B low byte	42E	–	–	EI2	EC4	EC3	EC2	EC1	EC0	00h
IPA0	Interrupt priority A0	4A0	PT0				PX0				00h
IPA1	Interrupt priority A1	4A1	PT1				PX1				00h
IPA2#	Interrupt priority A2	4A2	PPC				PT2				00h
IPA3#	Interrupt priority A3	4A3	–				PAD				00h
IPA4	Interrupt priority A4	4A4	PTI0				PRI0				00h

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	Reset Value
IPA5	Interrupt priority A5	4A5	PTI1				PRI1				00h
IPB0#	Interrupt priority B0	4A8	PC1				PC0				00h
IPB1#	Interrupt priority B1	4A9	PC3				PC2				00h
IPB2#	Interrupt priority B2	4AA	PI2				PC4				00h
			387	386	385	384	383	382	381	380	
P0*	Port 0	430	A11D7	A10D6	A9D5	A8D4	A7D3	A6D2	A5D1	A4D0	FFh
			38F	38E	38D	38C	38B	38A	389	388	
P1*	Port 1	431	T2EX	T2	TxD1	RxD1	A3	A2	A1	A0/WRH	FFh
			397	396	395	394	393	392	391	390	
P2*	Port 2	432	A19D15	A18D14	A17D13	A16D12	A15D11	A14D10	A13D9	A12D8	FFh
			39F	39E	39D	39C	39B	39A	399	398	
P3*	Port 3	433	RD	WRL	T1	T0	INT1	INT0	TxD0	RxD0	FFh
			3A7	3A6	3A5	3A4	3A3	3A2	3A1	3A0	
P4#*	Port 4	434	A21	A20	CEX4	CEX3	CEX2	CEX1	CEX0	ECI	FFh
			3AF	3AE	3AD	3AC	3AB	3AA	3A9	3A8	
P5#*	Port 5	435	AD7/SDA	AD6/SCL	AD5	AD4	AD3	AD2	AD1	AD0	FFh
									3B1	3B0	
P6#*	Port 6	436	–	–	–	–	–	–	A23	A22	FFh
P0CFGA	Port 0 configuration A	470									Note 5
P1CFGA	Port 1 configuration A	471									Note 5
P2CFGA	Port 2 configuration A	472									Note 5
P3CFGA	Port 3 configuration A	473									Note 5
P4CFGA#	Port 4 configuration A	474									Note 5
P5CFGA#	Port 5 configuration A	475									Note 5
P6CFGA#	Port 6 configuration A	476	–	–	–	–	–	–			Note 5
P0CFGB	Port 0 configuration B	4F0									Note 5
P1CFGB	Port 1 configuration B	4F1									Note 5
P2CFGB	Port 2 configuration B	4F2									Note 5
P3CFGB	Port 3 configuration B	4F3									Note 5
P4CFGB#	Port 4 configuration B	4F4									Note 5
P5CFGB#	Port 5 configuration B	4F5									Note 5
P6CFGB#	Port 6 configuration B	4F6	–	–	–	–	–	–			Note 5
			227	226	225	224	223	222	221	220	
PCON*	Power control register	404	–	–	–	–	–	–	PD	IDL	00h
			20F	20E	20D	20C	20B	20A	209	208	
PSWH*	Program status word (high byte)	401	SM	TM	RS1	RS0	IM3	IM2	IM1	IM0	Note 2
			207	206	205	204	203	202	201	200	
PSWL*	Program status word (low byte)	400	C	AC	–	–	–	V	N	Z	Note 2
			217	216	215	214	213	212	211	210	
PSW51*	80C51 compatible PSW	402	C	AC	F0	RS1	RS0	V	F1	P	Note 3

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	Reset Value
RSTSRC#	Reset source register	463	–	–	–	–	–	R_WD	R_CMD	R_EXT	Note 7
RTH0	Timer 0 reload register, high byte	455									00h
RTH1	Timer 1 reload register, high byte	457									00h
RTL0	Timer 0 reload register, low byte	454									00h
RTL1	Timer 1 reload register, low byte	456									00h
			307	306	305	304	303	302	301	300	
S0CON*	Serial port 0 control register	420	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00h
			30F	30E	30D	30C	30B	30A	309	308	
S0STAT#*	Serial port 0 extended status	421	–	–	–	ERR0	FE0	BR0	OE0	STINT0	00h
S0BUF	Serial port 0 data buffer register	460									xx
S0ADDR	Serial port 0 address register	461									00h
S0ADEN	Serial port 0 address enable	462									00h
			327	326	325	324	323	322	321	320	
S1CON*	Serial port 1 control register	424	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00H
			32F	32E	32D	32C	32B	32A	329	328	
S1STAT#*	Serial port 1 extended status	425	–	–	–	ERR1	FE1	BR1	OE1	STINT1	00h
S1BUF	Serial port 1 data buffer register	464									xx
S1ADDR	Serial port 1 address register	465									00h
S1ADEN	Serial port 1 address enable	466									00h
SCR	System configuration register	440	–	–	–	–	PT1	PT0	CM	PZ	00h
			21F	21E	21D	21C	21B	21A	219	218	
SSEL*	Segment selection register	403	ESWEN	R6SEG	R5SEG	R4SEG	R3SEG	R2SEG	R1SEG	R0SEG	00h
SWE	Software interrupt enable	47A	–	SWE7	SWE6	SWE5	SWE4	SWE3	SWE2	SWE1	00h
			357	356	355	354	353	352	351	350	
SWR*	Software interrupt request	42A	–	SWR7	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1	00h
			2C7	2C6	2C5	2C4	2C3	2C2	2C1	2C0	
T2CON*	Timer 2 control register	418	TF2	EXF2	RCLK0	TCLK0	EXEN2	TR2	C/T2	CP/RL2	00h
			2CF	2CE	2CD	2CC	2CB	2CA	2C9	2C8	
T2MOD*	Timer 2 mode control	419	–	–	RCLK1	TCLK1	–	–	T2OE	DCEN	00h
TH2	Timer 2 high byte	459									00h
TL2	Timer 2 low byte	458									00h
T2CAPH	Timer 2 capture, high byte	45B									00h
T2CAPL	Timer 2 capture, low byte	45A									00h
			287	286	285	284	283	282	281	280	
TCON*	Timer 0 and 1 control register	410	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	Reset Value
TH0	Timer 0 high byte	451									00h
TH1	Timer 1 high byte	453									00h
TL0	Timer 0 low byte	450									00h
TL1	Timer 1 low byte	452									00h
TMOD	Timer 0 and 1 mode control	45C	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
			28F	28E	28D	28C	28B	28A	289	288	
TSTAT*	Timer 0 and 1 extended status	411	–	–	–	–	–	T1OE	–	T0OE	00h
			2FF	2FE	2FD	2FC	2FB	2FA	2F9	2F8	
WDCON*	Watchdog control register	41F	PEW2	PRE1	PRE0	–	–	WDRUN	WDTOF	–	Note 6
WDL	Watchdog timer reload	45F									00h
WFEED1	Watchdog feed 1	45D									xx
WFEED2	Watchdog feed 2	45E									xx

NOTES:

* SFRs are bit addressable.

\# SFRs are modified from or added to XA-G3 SFRs.

1. At reset, the BCR is loaded with the binary value 00000a11, where “a’ is the value on the BUSW pin. This defaults the address bus size to 24 bits.
2. SFR is loaded from the reset vector.
3. All bits except F1, F0, and P are loaded from the reset vector. Those bits are all 0.
4. Unimplemented bits in SFRs are X (unknown) at all times. Ones should not be written to these bits since they may be used for other purposes in future XA derivatives. The reset value shown for these bits is 0.
5. Port configurations default to quasi-bidirectional when the XA begins execution from internal code memory after reset, based on the condition found on the $\overline{EA}$ pin. Thus, all PnCFGA registers will contain FF, and PnCFGB register will contain 00 when the XA begins execution using internal code memory. When the XA begins execution using external code memory, the default configuration for pins that are associated with the external bus will be push-pull. The PnCFGA and PnCFGB register contents will reflect this difference.
6. The WDCON reset value is E6 for a Watchdog reset, E4 for all other reset causes.
7. The RSTSRC register reflects the cause of the last XA-S3 reset. One bit will be set to 1, the others will be cleared to 0.
8. The XA guards writes to certain bits (typically interrupt flags) that may be altered directly by a peripheral function. This prevents loss of an interrupt or other status if a bit was written directly by a peripheral action during the time between the read and write portions of an instruction that performs a read-modify-write operation. Examples of such instructions are:

```
and     s0con,#$fb
clr     tr0
setb    ti_0
```

   XA-S3 SFR bits that are guarded in this manner are: ADINT (in ADCON); CF, CCF4, CCF3, CCF2, CCF1, and CCF0 (in CCON); SI (in I2CON); TI_0 and RI_0 (in S0CON); TI_1 and RI_1 (in S1CON); FE0, BR0, and OE0 (in S0STAT); FE1, BR1, and OE1 (in S1STAT); TF2 (in T2CON); TF1, TF0, IE1, and IE0 (in TCON); and WDTOF (in WDCON).
9. The XA-S3 implements an 8-bit SFR bus, as stated in *Chapter 8* of the *XA User Guide*. All SFR accesses must be 8-bit operations. Attempts to write 16 bits to an SFR will actually write only the lower 8 bits. Sixteen bit SFR reads will return undefined data in the upper byte.

FUNCTIONAL DESCRIPTION

Details of XA-S3 functions will be described in the following sections.

Analog to Digital converter

The XA-S3 has an 8-channel, 8-bit A/D converter with 8 sets of result registers, single scan and multiple scan operating modes. The A/D input range is limited to 0 to AV_{DD} (3.3V max.). The A/D inputs are on Port 5. Analog Power and Ground as well as AV_{REF+} and AV_{REF-} must be supplied in order for the A/D converter to be used. Prior to enabling the A/D converter or driving analog signals into the A/D inputs, the port configurations for the pins being used as A/D inputs must be set to the “off” (high impedance, input only) mode.

A/D timing can be adapted to the application clock frequency in order to provide the fastest possible conversion.

A/D converter operation is controlled through the ADCON (A/D Control) register, see Figure 1. Bits in ADCON start and stop the A/D, flag conversion completion, and select the converter operating modes.

A/D Conversion Modes

The A/D converter supports a single scan mode and a continuous scan mode. In either mode, one or more A/D channels may be converted. The ADCS register determines which channels are converted. If the corresponding bit in the ADCS register is set, that channel is selected for conversions, otherwise that channel is skipped. The ADCS register is detailed in Figure 2.

For any A/D conversion, the results are stored in ADRSHn, corresponding to the A/D channel just converted.

A/D conversions are begun by setting the A/D Start and STatus bit in ADCON. In the single scan mode, all of the channels selected by bits in the ADCS register will be converted once. The ADINT flag is set when the last channel is converted. In the continuous scan mode, the A/D converter continuously converts all A/D channels selected by bits in the ADCS register. The ADINT flag is set when all channels have been converted once.

The A/D converter can generate an interrupt when the ADINT flag is set. This will occur if the A/D interrupt is enabled (via the EAD bit in IEL), the interrupt system is enabled (via the EA bit in IEL), and the A/D interrupt priority (specified in IPA3 bits 3 to 0) is higher than the currently running code (PSW bits IM3 through IM0) and any other pending interrupt. ADINT must be cleared by software.

A/D Timing Configuration

The A/D sampling and conversion timing may be optimized for the particular oscillator frequency and input drive characteristics of the application. Because A/D operation is mostly dependent on real-time effects (charging time of sampling capacitors, settling time of the comparator, etc.), A/D conversion times are not necessarily much longer at slower clock frequencies. The A/D timing is controlled by the ADCFG register, as shown in Figure 3 and Table 2.

The primary effect of ADCFG settings is to adjust the A/D sample and hold time to be relatively constant over various clock frequencies. Two settings (value 6 and B) are provided to allow fast conversions with a lower external source driving the A/D inputs. These settings provide double the sample time at the same frequency. Of course, settings intended for lower frequencies may also be used at higher frequencies in order to increase the A/D sampling time, but this method has the side effect of significantly increasing A/D conversion times.

ADCON Address:43Eh
Bit Addressable
Reset Value: 00h

MSB							LSB
—	—	—	—	—	ADMOD	ADSST	ADINT

BIT	SYMBOL	FUNCTION
ADCON.7	—	Reserved for future use. Should not be set to 1 by user programs.
ADCON.6	—	Reserved for future use. Should not be set to 1 by user programs.
ADCON.5	—	Reserved for future use. Should not be set to 1 by user programs.
ADCON.4	—	Reserved for future use. Should not be set to 1 by user programs.
ADCON.3	—	Reserved for future use. Should not be set to 1 by user programs.
ADCON.2	ADMOD	A/D mode select. 1 = continuous scan of selected inputs after a start of the A/D. 0 = single scan of selected inputs after a start of the A/D.
ADCON.1	ADSST	A/D start and status. Setting this bit by software starts the A/D conversion of the selected A/D inputs. ADSST remains set as long as the A/D is in operation. In continuous conversion mode, ADSST will remain set unless the A/D is stopped by software. While ADSST is set, new start commands are ignored. An A/D conversion is progress may be aborted by software clearing ADSST.
ADCON.0	ADINT	A/D conversion complete/interrupt flag. This flag is set when all selected A/D channels are converted in either the single scan or continuous scan modes. Must be cleared by software.

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Figure 1. A/D Control Register (ADCON)

ADCS Address:43Fh
Bit Addressable
Reset Value: 00h

MSB LSB

ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0

BIT	SYMBOL	FUNCTION
ADCS.7	ADCS7	A/D channel 7 select bit.
ADCS.6	ADCS6	A/D channel 6 select bit.
ADCS.5	ADCS5	A/D channel 5 select bit.
ADCS.4	ADCS4	A/D channel 4 select bit.
ADCS.3	ADCS3	A/D channel 3 select bit.
ADCS.2	ADCS2	A/D channel 2 select bit.
ADCS.1	ADCS1	A/D channel 1 select bit.
ADCS.0	ADCS0	A/D channel 0 select bit.

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Figure 2. A/D Channel Select Register (ADCS)

ADCFG Address:4B9h
Not bit Addressable
Reset Value: 00h

MSB LSB

—	—	—	—	A/D Timing Configuration			

BIT	SYMBOL	FUNCTION
ADCFG.7	—	Reserved for future use. Should not be set to 1 by user programs.
ADCFG.6	—	Reserved for future use. Should not be set to 1 by user programs.
ADCFG.5	—	Reserved for future use. Should not be set to 1 by user programs.
ADCFG.4	—	Reserved for future use. Should not be set to 1 by user programs.
ADCFG.3–0	ADCFG	A/D timing configuration (see text and table).

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Figure 3. A/D Timing Configuration Register (ADCFG)

Table 2. A/D Timing Configuration

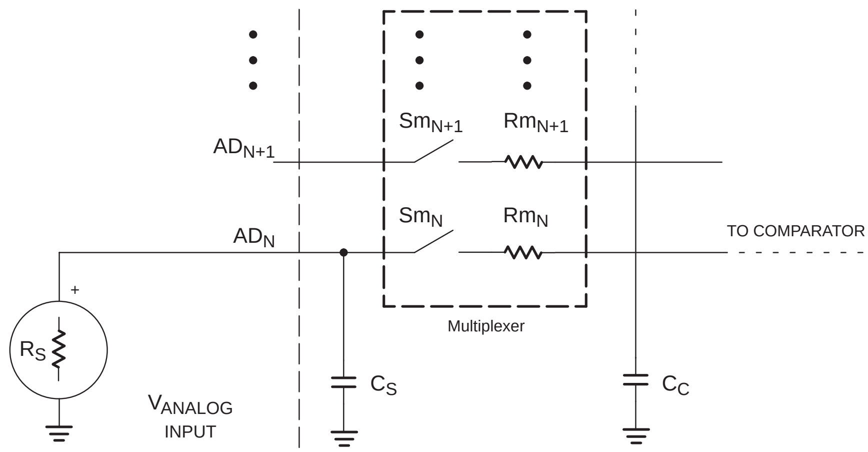
ADCFG.3–0	Max. Oscillator Frequency (MHz)	Conversion Time		Sampling Time (Osc. Clocks)
		Osc. Clocks	µsec at max. Osc.	
0h (0000)	6.66	70	11.11	4
1h (0001)	10	78	7.8	6
2h (0010)	11.11	82	7.38	8
3h (0011)	13.33	98	7.35	8
4h (0100)	16.66	102	6.12	10
5h (0101)	20	106	5.3	12
6h (0110)[1]	20	118	5.9	24
7h (0111)	22.2	102	4.95	14
8h (1000)	23.3	126	5.4	14
9h (1001)	26.6	130	4.88	16
Ah (1010)	30	134	4.46	18
Bh (1011)[1]	30	148	4.93	32
Ch (1100)	32	138	4.31	20
Dh (1101)	33.3	152	4.56	20
Eh (1110)	36.6	172	4.69	22
Fh (1111)	40	176	4.4	24

NOTE:
1. These settings provide additional A/D input sampling time, in order to allow accurate readings with a higher external source impedance.

A/D Inputs

In order to obtain accurate measurements with the A/D Converter, the source drive must be sufficient to adequately charge the sampling capacitor during the sampling time. Figure 4 shows the equivalent resistance and capacitance related to the A/D inputs.

A/D timing configurations indicated in Table 1 allow for full A/D accuracy (according to the A/D specifications) assuming a source resistance of less than or equal to 20kΩ. Larger source resistances may be accommodated by increasing the sampling time with a different A/D timing configuration.



R_m (multiplexer resistance)	=	3 kΩ maximum
C_S (pin capacitance)	=	10 pF maximum
C_C (sampling capacitor)	=	2 pF maximum
R_S (source resistance)	=	Recommended less than 20kΩ for full specified accuracy. This allows time for the sampling capacitor (C_C) to fully charge while the multiplexer switch is closed. Please note that sampling causes the analog input to present a varying load to the pin.

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Figure 4. A/D Input: Equivalent Circuit

I2CON Address:42Ch
Bit Addressable
Reset Value: 00h

MSB							LSB
CR2	ENA	STA	STO	SI	AA	CR1	CR0

BIT	SYMBOL	FUNCTION
I2CON.7	CR2	I^{2}C Rate Control, with CR1 and CR0. See text and table.
I2CON.6	ENA	Enable I^{2}C port. When ENA = 1, the I^{2}C port is enabled.
I2CON.5	STA	Start flag. Setting STA to 1 causes the I^{2}C interface to attempt to gain mastership of the bus by generating a Start condition.
I2CON.4	STO	Stop flag. Setting STO to 1 causes the I^{2}C interface to attempt to generate a Stop condition.
I2CON.3	SI	Serial Interrupt. SI is set by the I^{2}C hardware when a new I^{2}C state is entered, indicating that software needs to respond. SI causes an I^{2}C interrupt if enabled and of sufficient priority.
I2CON.2	AA	Assert Acknowledge. Setting AA to 1 causes the I^{2}C hardware to automatically generate acknowledge pulses for various conditions (see text).
I2CON.1	CR1	I^{2}C Rate Control, with CR2 and CR0. See text and table.
I2CON.0	CR0	I^{2}C Rate Control, with CR2 and CR1. See text and table.

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Figure 5. I^{2}C Control Register (I2CON)

I^{2}C Interface

The I^{2}C interface on the XA-S3 is identical to the standard byte-style I^{2}C interface found on devices such as the 8xC552 except for the rate selection. ***The I^{2}C interface conforms to the 100 kHz I^{2}C specification, but may be used at rates up to 400 kHz (non-conforming).***

Important: Before the I^{2}C interface may be used, the port pins P5.6 and 5.7, which correspond to the I^{2}C functions SCL and SDA respectively, must be set to the open drain mode.

The processor interfaces to the I^{2}C logic via the following four special function registers: I2CON (I^{2}C control register), I2STA (I^{2}C status register), I2DAT (I^{2}C data register), and I2ADR (I^{2}C slave address register). The I^{2}C control logic interfaces to the external I^{2}C bus via two port 5 pins: P5.6/SCL (serial clock line) and P5.7/SDA (serial data line).

The Control Register, I2CON
This register is shown in Figure 5. Two bits are affected by the I^{2}C hardware: the SI bit is set when a serial interrupt is requested, and the STO bit is cleared when a STOP condition is present on the I^{2}C bus. The STO bit is also cleared when ENA = “0”.

ENA, the I^{2}C Enable Bit
ENA = 0: When ENA is “0”, the SDA and SCL outputs are not driven. SDA and SCL input signals are ignored, SIO1 is in the “not addressed” slave state, and the STO bit in I2CON is forced to “0”. No other bits are affected. P5.6 and P5.7 may be used as open drain I/O ports.

ENA = 1: When ENA is “1”, SIO1 is enabled. The P5.6 and P5.7 port latches must be set to logic 1.

ENA should not be used to temporarily release the I^{2}C-bus since, when ENA is reset, the I^{2}C-bus status is lost. The AA flag should be used instead (see description of the AA flag in the following text).

In the following text, it is assumed the ENA = “1”.

STA, the START flag
STA = 1: When the STA bit is set to enter a master mode, the I^{2}C hardware checks the status of the I^{2}C bus and generates a START condition if the bus is free. If the bus is not free, the I^{2}C interface waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal serial clock generator.

If STA is set while the I^{2}C interface is already in a master mode and one or more bytes are transmitted or received, the hardware transmits a repeated START condition. STA may be set at any time. STA may also be set when the I^{2}C interface is an addressed slave.

STA = 0: When the STA bit is reset, no START condition or repeated START condition will be generated.

STO, the STOP flag
STO = 1: When the STO bit is set while the I^{2}C interface is in a master mode, a STOP condition is transmitted to the I^{2}C bus. When the STOP condition is detected on the bus, the hardware clears the STO flag. In a slave mode, the STO flag may be set to recover from an error condition. In this case, no STOP condition is transmitted to the I^{2}C bus. However, the hardware behaves as if a STOP condition has been received and switches to the defined “not addressed” slave receiver mode. The STO flag is automatically cleared by hardware.

If the STA and STO bits are both set, then a STOP condition is transmitted to the I^{2}C bus if the interface is in a master mode (in a slave mode, the hardware generates an internal STOP condition which is not transmitted). The I^{2}C interface then transmits a START condition.

STO = 0: When the STO bit is reset, no STOP condition will be generated.

SI, the Serial Interrupt flag
SI = 1: When the SI flag is set, and the EA (interrupt system enable) and EI2 (I^{2}C interrupt enable) bits are also set, an I^{2}C interrupt is requested. SI is set by hardware when one of 25 of the 26 possible I^{2}C interface states is entered. The only state that does not cause SI to be set is state F8H, which indicates that no relevant state information is available.

While SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. A high level on the SCL line is unaffected by the serial interrupt flag. SI must be reset by software.

SI = 0: When the SI flag is reset, no serial interrupt is requested, and there is no stretching of the serial clock on the SCL line.

AA, the Assert Acknowledge flag

AA = 1: If the AA flag is set, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when:

- The “own slave address” has been received.
- The general call address has been received while the general call bit (GC) in I2ADR is set.
- A data byte has been received while the I²C interface is in the master receiver mode.
- A data byte has been received while the I²C interface is in the addressed slave receiver mode.

AA = 0: If the AA flag is reset, a not acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line when:

- A data byte has been received while the I²C interface is in the master receiver mode.
- A data byte has been received while the I²C interface is in the addressed slave receiver mode.

When the I²C interface is in the addressed slave transmitter mode, state C8H will be entered after the last serial data byte is transmitted. When SI is cleared, the I²C interface leaves state C8H, enters the not addressed slave receiver mode, and the SDA line remains at a high level. In state C8H, the AA flag can be set again for future address recognition.

When the I²C interface is in the not addressed slave mode, its own slave address and the general call address are ignored. Consequently, no acknowledge is returned, and a serial interrupt is not requested. Thus, the hardware can be temporarily released from the I²C bus while the bus status is monitored. While the hardware is released from the bus, START and STOP conditions are detected, and serial data is shifted in. Address recognition can be resumed at any time by setting the AA flag. If the AA flag is set when the part’s own slave address or the general call address has been partly received, the address will be recognized at the end of the byte transmission.

CR0, CR1, and CR2, the Clock Rate Bits

These three bits determine the serial clock frequency when the I²C interface is in a master mode. An I²C rate of 100kHz or lower is typical and can be derived from many oscillator frequencies. The various serial rates are shown in Table 3. A variable bit rate may also be used if Timer 1 is not required for any other purpose while the I²C hardware is in a master mode. The frequencies shown in Table 3 are unimportant when the I²C hardware is in a slave mode. In the slave modes, the hardware will automatically synchronize with the incoming clock frequency.

The I²C Status Register, I2STA

I2STA is an 8-bit read-only special function register. The three least significant bits are always zero. The five most significant bits contain the status code. There are 26 possible status codes. When I2STA contains F8H, no relevant state information is available and no serial interrupt is requested. All other I2STA values correspond to defined hardware interface states. When each of these states is entered, a serial interrupt is requested (SI = “1”).

NOTE: A detailed I²C interface description and usage information, including example driver code, will be provided in a separate document.

Table 3. I²C Rate Control

Frequency Select (CR2, CR1, CR0)	Clock Divisor	Example I²C Rates at Specific Oscillator Frequencies					
		8 MHz	12 MHz	16 MHz	20 MHz	24 MHz	30 MHz
0h (0000)	20	(400)[1]	–	–	–	–	–
1h (0001)	40	(200)[1]	(300)[1]	(400)[1]	–	–	–
2h (0010)	68	(116.65)[1]	(176.46)[1]	(235.29)[1]	(294.12)[1]	(352.94)[1]	–
3h (0011)	88	90.91	(136.36)[1]	(181.82)[1]	(227.27)[1]	(272.73)[1]	(340.91)[1]
4h (0100)	160	50	75	100	(125)[1]	(150)[1]	(187.5)[1]
5h (0101)	272	29.41	44.12	58.82	73.53	88.24	(110.29)[1]
6h (0110)	352	22.73	34.09	45.45	56.82	68.18	85.23
7h (0111)	(Timer 1)[2]	(Timer 1)[2]	(Timer 1)[2]	(Timer 1)[2]	(Timer 1)[2]	(Timer 1)[2]	(Timer 1)[2]

NOTES:
1. The XA-S3 I²C interface does not conform to the 400kHz I²C specification (which applies to rates greater than 100kHz) in all details, but may be used with care where higher rates are required by the application.
2. The timer 1 overflow is used to clock the I²C interface. The resulting bit rate is 1/2 of the timer overflow rate.

XA-S3 Timer/Counters

The XA-S3 has three general purpose counter/timers, two of which may also be used as baud rate generators for either or both of the UARTs.

Timer 0 and 1
These are identical to the standard XA-G3 timer 0 and 1.

Timer 2
This is identical to the standard XA-G3 timer 2.

PCA

This is a standard 80C51FC-style PCA counter/timer. The XA uses TCLK (the global peripheral clock which is Osc/4, Osc/16, or Osc/64), Timer 0 overflow, and External (ECI pin). When the ECI input is used, the falling edge clocks the PCA counter. The maximum rate for the counter in this mode on the XA is Osc/4. Each PCA module has its own interrupt (in addition to the standard global PCA interrupt).

CPS1	CPS0	PCA Clock Source
0	x	TCLK (osc/4, osc/16, or osc/64
1	0	Timer 0 Overflow
1	1	ECI (PCA External Clock Input)

Watchdog Timer

This is a standard XA-G3 watchdog timer. This watchdog timer always comes up running at reset. The watchdog acts the same on EPROM, ROM, and ROMless parts, as in the XA-G3.

UARTs

Standard XA-G3 UART0 and UART1 with double buffered transmit register. A flag has been added to SnSTAT that is set if any of the status flags (BRn, FEn, or OEn) is set for the corresponding UART channel. This allows polling for UART errors quickly at the interrupt service routine. Baud rate sources may be timer 1 or timer 2.

Clocking / Baud Rate Generation

Same as for the XA-G3.

I/O Port Output Configuration

Port output configurations are the same as for the XA-G3: open drain, quasi-bidirectional, push-pull, and off.

External Bus

The external bus operates in the same manner as the XA-G3, but all 24 address lines are brought out to the outside world. This allows for a maximum of 16 Mbytes of code memory and 16 Mbytes of data memory.

Clock Output

The CLKOUT pin allows easier external bus interfacing in some situations. This output reflects the X1 clock input to the XA, but is delayed to match the external bus outputs and strobes. The default is for CLKOUT to be on at reset, but it may be turned off via the CLKD bit that has been added to the BCR register.

Reset

Active low reset input, the same as the XA-G3.

The associated $\overline{RSTOUT}$ pin provides an external indication via an active low open drain output when an internal reset occurs. The $\overline{RSTOUT}$ pin will be driven low when the $\overline{RST}$ pin is driven low, when a Watchdog reset occurs or the RESET instruction is executed. This signal may be used to inform other devices in a system that the XA-S3 has been reset.

The latched values of $\overline{EA}$ and BUSW are NOT automatically updated when an internal reset occurs. $\overline{RSTOUT}$ may be used to apply an external reset to the XA-S3 in order to update the previously latched $\overline{EA}$ and BUSW values. However, since $\overline{RSTOUT}$ reflects ALL reset sources, it cannot simply be fed back into the $\overline{RST}$ pin without other logic.

The reset source identification register (RSTSRC) indicates the cause of the most recent XA reset. The cause may have been an externally applied reset signal, execution of the RESET instruction, or a Watchdog reset. Figure 6 shows the fields in the RSTSRC register.

Power Reduction Modes

The XA-S3 supports Idle and Power Down modes of power reduction. The idle mode leaves some peripherals running in order to allow them to activate the processor when an interrupt is generated. The power down mode stops the oscillator in order to absolutely minimize power. The processor can be made to exit power down mode via a reset or one of the external interrupt inputs (INT0 or INT1). This will occur if the interrupt is enabled and its priority is higher than that defined by IM3 through IM0. In power down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM, register, and SFR contents at the point where power down mode was entered. V_{DD} must be raised to within the operating range before power down mode is exited.

RSTSRC Address:463h
Not bit Addressable
Reset Value: see below

MSB … LSB

—	—	—	—	—	R_WD	R_CMD	R_EXT

BIT	SYMBOL	FUNCTION
RSTSRC.7	—	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.6	—	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.5	—	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.4	—	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.3	—	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.2	R_WD	Indicates that the last reset was caused by a watchdog timer overflow.
RSTSRC.1	R_CMD	Indicates that the last reset was caused by execution of the RESET instruction.
RSTSRC.0	R_EXT	Indicates that the last reset was caused by the external $\overline{RST}$ input.

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Figure 6. Reset source register (RSTSRC)

INTERRUPTS

XA-S3 interrupt sources include the following:

- External interrupts 0 and 1 (2)
- Timer 0, 1, and 2 interrupts (3)
- PCA: 1 global and 5 channel interrupts (6)
- A/D interrupt (1)
- UART 0 transmitter and receiver interrupts (2)
- UART 1 transmitter and receiver interrupts (2)
- I^{2}C interrupt (1)
- Software interrupts (7)

There are a total of 17 **hardware** interrupt sources, enable bits, priority bit sets, etc.

EXCEPTION/TRAPS PRECEDENCE

DESCRIPTION	VECTOR ADDRESS	ARBITRATION RANKING
Reset (h/w, watchdog, s/w)	0000–0003	0 (High)
Breakpoint	0004–0007	1
Trace	0008–000B	1
Stack Overflow	000C–000F	1
Divide by 0	0010–0013	1
User RETI	0014–0017	1
TRAP 0–15 (software)	0040–007F	1

EVENT INTERRUPTS

DESCRIPTION	FLAG BIT	VECTOR ADDRESS	ENABLE BIT	INTERRUPT PRIORITY	ARBITRATION RANKING
External Interrupt 0	IE0	0080–0083	EX0	IPA0.3–0 (PX0)	2
Timer 0 Interrupt	TF0	0084–0087	ET0	IPA0.7–4 (PT0)	3
External Interrupt 1	IE1	0088–008B	EX1	IPA1.3–0 (PX1)	4
Timer 1 Interrupt	TF1	008C–008F	ET1	IPA1.7–4 (PT1)	5
Timer 2 Interrupt	TF2 (EXF2)	0090–0093	ET2	IPA2.3–0 (PT2)	6
PCA Interrupt	CCF0–CCF4, CF	0094–0097	EPC	IPA2.7–4 (PPC)	7
A/D Interrupt	ADINT	0098–009B	EAD	IPA3.3–0 (PAD)	8
Serial Port 0 Rx	RI_0	00A0–00A3	ERI0	IPA4.3–0 (PRI0)	9
Serial Port 0 Tx	TI_0	00A4–00A7	ETI0	IPA4.7–4 (PTI0)	10
Serial Port 1 Rx	RI_1	00A8–00AB	ERI1	IPA5.3–0 (PRI1)	11
Serial Port 1 Tx	TI_1	00AC–00AF	ETI1	IPA5.7–4 (PTI1)	12
PCA channel 0	CCF0	00C0–00C3	EC0	IPB0.3–0 (PC0)	17
PCA channel 1	CCF1	00C4–00C7	EC1	IPB0.7–4 (PC1)	18
PCA channel 2	CCF2	00C8–00CB	EC2	IPB1.3–0 (PC2)	19
PCA channel 3	CCF3	00CC–00CF	EC3	IPB1.7–4 (PC3)	20
PCA channel 4	CCF4	00D0–00D3	EC4	IPB2.3–0 (PC4)	21
I^{2}C Interrupt	SI	00D4–00D7	EI2	IPB2.7–4 (PI2)	22

SOFTWARE INTERRUPTS

DESCRIPTION	FLAG BIT	VECTOR ADDRESS	ENABLE BIT	INTERRUPT PRIORITY
Software Interrupt 1	SWR1	0100–0103	SWE1	(fixed at 1)
Software Interrupt 2	SWR2	0104–0107	SWE2	(fixed at 2)
Software Interrupt 3	SWR3	0108–010B	SWE3	(fixed at 3)
Software Interrupt 4	SWR4	010C–010F	SWE4	(fixed at 4)
Software Interrupt 5	SWR5	0110–0113	SWE5	(fixed at 5)
Software Interrupt 6	SWR6	0114–0117	SWE6	(fixed at 6)
Software Interrupt 7	SWR7	0118–011B	SWE7	(fixed at 7)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5V	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, unless otherwise specified.
T_{amb} = 0 to +70°C for commercial unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{DD}	Power supply current, operating	5.0V, 30MHz			80	mA
I_{ID}	Power supply current, Idle mode	5.0V, 30MHz			35	mA
I_{PD}	Power supply current, Power Down mode	5.0V, 3.0V		5	50	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage		–0.5		0.22 V_{DD}	V
V_{IH}	Input high voltage, except XTAL1, $\overline{RST}$	V_{DD} = 5.0V	2.2			V
		V_{DD} = 3.0V	2.0			V
V_{IH1}	Input high voltage to XTAL1, $\overline{RST}$	For both 3.0V and 5.0V	0.7 V_{DD}			V
V_{OL}	Output low voltage, all ports, ALE, $\overline{PSEN}$[4]	I_{OL} = 3.2mA, V_{DD} = 5.0V			0.5	V
		I_{OL} = 1.0mA, V_{DD} = 3.0V			0.4	V
V_{OH1}	Output high voltage, all ports, ALE, $\overline{PSEN}$[2]	I_{OH} = –100µA, V_{DD} = 4.5V	2.4			V
		I_{OH} = –30µA, V_{DD} = 2.7V	2.0			V
V_{OH2}	Output high voltage, all ports ALE, $\overline{PSEN}$[3]	I_{OH} = –3.2mA, V_{DD} = 4.5V	2.4			V
		I_{OH} = –1.0mA, V_{DD} = 2.7V	2.2			V
C_{IO}	Input/Output pin capacitance[1]				15	pF
I_{IL}	Logical 0 input current, all ports[7]	V_{IN} = 0.45V			–50	µA
I_{LI}	Input leakage current, all ports[6]	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{TL}	Logical 1 to 0 transition current, all ports[5]	At V_{DD} = 5.5V			–650	µA
		At V_{DD} = 2.7V			–250	µA

NOTES:
1. Maximum 15pF for $\overline{EA}/V_{PP}$.
2. Ports in quasi-bidirectional mode with weak pullup (applies to ALE, $\overline{PSEN}$ only during $\overline{RESET}$).
3. Ports in PUSH-PULL mode, both pullup and pulldown assumed to be the same strength.
4. In all output modes.
5. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2V.
6. Measured with port in high impedance mode.
7. Measured with port in quasi-bidirectional mode.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

A/D CONVERTER DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 to +70°C for commercial unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
AV_{DD}	Analog supply voltage		2.7	3.3	V
AI_{DD}	Analog supply current (operating)	Port 5 = 0 to AV_{DD}		2.5	mA
AI_{ID}	Analog supply current (Idle mode)			2.5	µA
AI_{PD}	Analog supply current (Power-Down mode)			NA	µA
AV_{IN}	Analog input voltage		AV_{SS} –0.2	AV_{DD} +0.2	V
R_{REF}	Resistance between V_{REF+} and V_{REF-}		125	225	kΩ
C_{IA}	Analog input capacitance			15	pF
DL_e	Differential non-linearity[1, 2, 3]			±1	LSB
IL_e	Integral non-linearity[1, 4]			±1	LSB
OS_e	Offset error[1, 5]			±4	LSB
COS_e	Compensated offset error[1, 5, 9]			±2	LSB
G_e	Gain error[1, 6]			±1	LSB
A_e	Absolute voltage error[1, 7]			±4	LSB
CA_e	Compensated absolute voltage error[1, 7, 9]			±2.5	LSB
M_{CTC}	Channel-to-channel matching			±1	LSB
C_t	Crosstalk between inputs of port[8]	0 – 100kHz		–60	dB

NOTES:
1. Conditions: AV_{REF-} = 0V; AV_{REF+} = 3.07V.
2. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. See Figure 7.
3. The ADC is monotonic, there are no missing codes.
4. The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.
5. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and the straight line which fits the ideal transfer curve. See Figure 7.
6. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. See Figure 7.
7. The absolute voltage error (A_e) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
8. This should be considered when both analog and digital signals are input simultaneously to Port 5. Parameter is guaranteed by design.
9. Compensated values are the direct ADC result minus the result of a calibration operation.

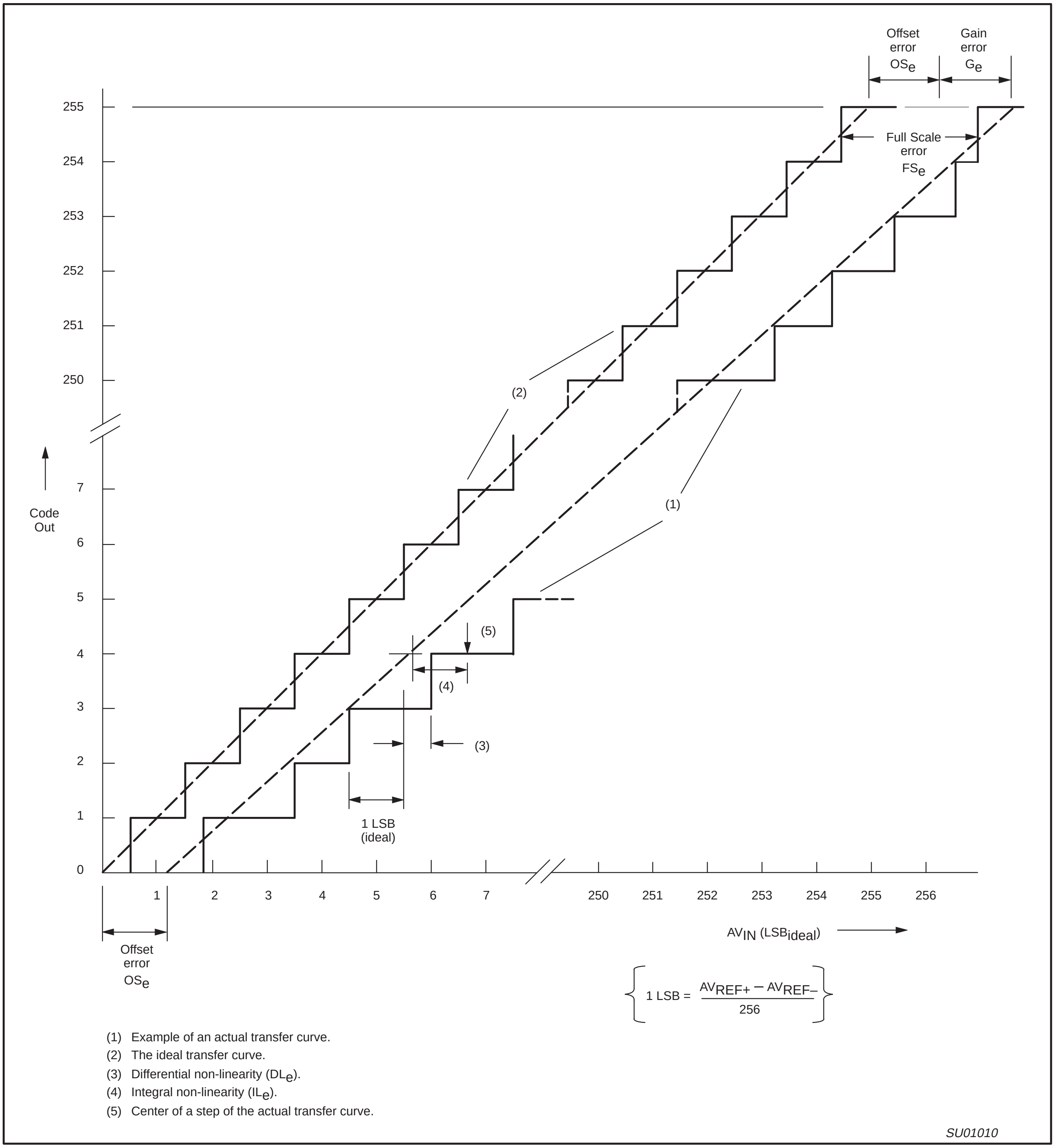

Figure 7. ADC Conversion Characteristic

AC ELECTRICAL CHARACTERISTICS (5V)

V_{DD} = 4.5V to 5.5V; T_{amb} = 0 to +70°C for commercial.

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
External Clock					
f_C	14	Oscillator frequency	0	30	MHz
t_C	14	Clock period and CPU timing cycle	$1/f_C$		ns
t_{CHCX}	14	Clock high-time	t_C * 0.5		ns
t_{CLCX}	14	Clock low time	t_C * 0.4		ns
t_{CLCH}	14	Clock rise time		5	ns
t_{CHCL}	14	Clock fall time		5	ns
Address Cycle					
t_{LHLL}	8, 10, 12	ALE pulse width (programmable)	(V1 * t_C) – 6		ns
t_{AVLL}	8, 10, 12	Address valid to ALE de-asserted (set-up)	(V1 * t_C) – 12		ns
t_{LLAX}	8, 10, 12	Address hold after ALE de-asserted	(t_C/2) – 10		ns
Code Read Cycle					
t_{PLPH}	8	$\overline{PSEN}$ pulse width	(V2 * t_C) – 10		ns
t_{LLPL}	8	ALE de-asserted to $\overline{PSEN}$ asserted	(t_C/2) – 7		ns
t_{AVIVA}	8	Address valid to instruction valid, ALE cycle (access time)		(V3 * t_C) – 36	ns
t_{AVIVB}	9	Address valid to instruction valid, non-ALE cycle (access time)		(V4 * t_C) – 29	ns
t_{PLIV}	8	$\overline{PSEN}$ asserted to instruction valid (enable time)		(V2 * t_C) – 29	ns
t_{PHIX}	8	Instruction hold after $\overline{PSEN}$ de-asserted	0		ns
t_{PHIZ}	8	Bus 3-State after $\overline{PSEN}$ de-asserted		t_C – 8	ns
t_{IXUA}	8	Hold time of unlatched part of address after instruction latched	0		ns
Data Read Cycle					
t_{RLRH}	10	$\overline{RD}$ pulse width	(V7 * t_C) – 10		ns
t_{LLRL}	10	ALE de-asserted to $\overline{RD}$ asserted	(t_C/2) – 7		ns
t_{AVDVA}	10	Address valid to data input valid, ALE cycle (access time)		(V6 * t_C) – 36	ns
t_{AVDVB}	11	Address valid to data input valid, non-ALE cycle (access time)		(V5 * t_C) – 29	ns
t_{RLDV}	10	$\overline{RD}$ low to valid data in (enable time)		(V7 * t_C) – 29	ns
t_{RHDX}	10	Data hold time after $\overline{RD}$ de–asserted	0		ns
t_{RHDZ}	10	Bus 3-State after $\overline{RD}$ de-asserted (disable time)		t_C – 8	ns
t_{DXUA}	10	Hold time of unlatched part of address after data latched	0		ns
Data Write Cycle					
t_{WLWH}	12	$\overline{WR}$ pulse width	(V8 * t_C) – 10		ns
t_{LLWL}	12	ALE falling edge to $\overline{WR}$ asserted	(V12 * t_C) – 10		ns
t_{QVWX}	12	Data valid before $\overline{WR}$ asserted (data set-up time)	(V13 * t_C) – 22		ns
t_{WHQX}	12	Data hold time after $\overline{WR}$ de-asserted (Note 6)	(V11 * t_C) – 5		ns
t_{AVWL}	12	Address valid to $\overline{WR}$ asserted (address set-up time) (Note 5)	(V9 * t_C) – 22		ns
t_{UAWH}	12	Hold time of unlatched part of address after $\overline{WR}$ is de-asserted	(V11 * t_C) – 7		ns
Wait Input					
t_{WTH}	13	WAIT stable after bus strobe ($\overline{RD}$, $\overline{WR}$, or $\overline{PSEN}$) asserted		(V10 * t_C) – 30	ns
t_{WTL}	13	WAIT hold after bus strobe ($\overline{RD}$, $\overline{WR}$, or $\overline{PSEN}$) asserted	(V10 * t_C) – 5		ns

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AC ELECTRICAL CHARACTERISTICS (5V) (continued)

This set of parameters is referenced to the XA-S3 clock output.

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
Address Cycle					
t_{CHLH}	8	Delay from CLKOUT rising edge to ALE rising edge	10	40	ns
t_{CLLL}	8	Delay from CLKOUT falling edge to ALE falling edge			ns
t_{CHAV}	8	Delay from CLKOUT rising edge to address valid			ns
t_{CHAX}	8	Address hold after CLKOUT rising edge			ns
Code Read Cycle					
t_{CHPL}	8	Delay from CLKOUT rising edge to $\overline{PSEN}$ asserted			ns
t_{CHPH}	8	Delay from CLKOUT rising edge to $\overline{PSEN}$ de-asserted			ns
t_{IVCH}	8	Instruction valid to CLKOUT rising edge			ns
t_{CHIX}	8	Instruction hold from CLKOUT rising edge			ns
t_{CHIZ}	8	Bus 3-State after CLKOUT rising edge (code read)			ns
Data Read Cycle					
t_{CHRL}	10	Delay from CLKOUT rising edge to $\overline{RD}$ asserted			ns
t_{CHRH}	10	Delay from CLKOUT rising edge to $\overline{RD}$ de-asserted			ns
t_{DVCH}	10	Data valid to CLKOUT rising edge			ns
t_{CHDX}	10	Data hold after CLKOUT rising edge			ns
t_{CHDZ}	10	Bus 3-State after CLKOUT rising edge (data read)			ns
Data Write Cycle					
t_{CHWL}	12	Delay from CLKOUT rising edge to $\overline{WR}$ asserted			ns
t_{CHWH}	12	Delay from CLKOUT rising edge to $\overline{WR}$ de-asserted			ns
t_{QVCH}	12	Data valid to CLKOUT rising edge			ns
t_{CHQX}	12	Data hold after CLKOUT rising edge			ns
t_{CHQZ}	12	Bus 3-State after CLKOUT rising edge (data write)			ns
Wait Input					
t_{CHWTH}	13	WAIT stable before CLKOUT rising edge			ns
t_{CHWTL}	13	WAIT hold after CLKOUT rising edge			ns

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AC ELECTRICAL CHARACTERISTICS (3V)

V_{DD} = 2.7V to 4.5V; T_{amb} = 0 to +70°C for commercial.

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
Address Cycle					
t_{LHLL}	8, 10, 12	ALE pulse width (programmable)	(V1 * t_C) – 10		ns
t_{AVLL}	8, 10, 12	Address valid to ALE de-asserted (set-up)	(V1 * t_C) – 18		ns
t_{LLAX}	8, 10, 12	Address hold after ALE de-asserted	(t_C/2) – 12		ns
Code Read Cycle					
t_{PLPH}	8	$\overline{PSEN}$ pulse width	(V2 * t_C) – 12		ns
t_{LLPL}	8	ALE de-asserted to $\overline{PSEN}$ asserted	(t_C/2) – 9		ns
t_{AVIVA}	8	Address valid to instruction valid, ALE cycle (access time)		(V3 * t_C) – 58	ns
t_{AVIVB}	9	Address valid to instruction valid, non-ALE cycle (access time)		(V4 * t_C) – 52	ns
t_{PLIV}	8	$\overline{PSEN}$ asserted to instruction valid (enable time)		(V2 * t_C) – 52	ns
t_{PHIX}	8	Instruction hold after $\overline{PSEN}$ de-asserted	0		ns
t_{PHIZ}	8	Bus 3-State after $\overline{PSEN}$ de-asserted		t_C – 8	ns
t_{IXUA}	8	Hold time of unlatched part of address after instruction latched	0		ns
Data Read Cycle					
t_{RLRH}	10	$\overline{RD}$ pulse width	(V7 * t_C) – 12		ns
t_{LLRL}	10	ALE de-asserted to $\overline{RD}$ asserted	(t_C/2) – 9		ns
t_{AVDVA}	10	Address valid to data input valid, ALE cycle (access time)		(V6 * t_C) – 58	ns
t_{AVDVB}	11	Address valid to data input valid, non-ALE cycle (access time)		(V5 * t_C) – 52	ns
t_{RLDV}	10	$\overline{RD}$ low to valid data in (enable time)		(V7 * t_C) – 52	ns
t_{RHDX}	10	Data hold time after $\overline{RD}$ de–asserted	0		ns
t_{RHDZ}	10	Bus 3-State after $\overline{RD}$ de-asserted (disable time)		t_C – 8	ns
t_{DXUA}	10	Hold time of unlatched part of address after data latched	0		ns
Data Write Cycle					
t_{WLWH}	12	$\overline{WR}$ pulse width	(V8 * t_C) – 12		ns
t_{LLWL}	12	ALE falling edge to $\overline{WR}$ asserted	(V12 * t_C) – 10		ns
t_{QVWX}	12	Data valid before $\overline{WR}$ asserted (data set-up time)	(V13 * t_C) – 28		ns
t_{WHQX}	12	Data hold time after $\overline{WR}$ de-asserted (Note 6)	(V11 * t_C) – 8		ns
t_{AVWL}	12	Address valid to $\overline{WR}$ asserted (address set-up time) (Note 5)	(V9 * t_C) – 28		ns
t_{UAWH}	12	Hold time of unlatched part of address after $\overline{WR}$ is de-asserted	(V11 * t_C) – 10		ns
Wait Input					
t_{WTH}	13	WAIT stable after bus strobe ($\overline{RD}$, $\overline{WR}$, or $\overline{PSEN}$) asserted		(V10 * t_C) – 40	ns
t_{WTL}	13	WAIT hold after bus strobe ($\overline{RD}$, $\overline{WR}$, or $\overline{PSEN}$) asserted	(V10 * t_C) – 5		ns

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AC ELECTRICAL CHARACTERISTICS (3V) (continued)

This set of parameters is referenced to the XA-S3 clock output.

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
Address Cycle					
t_{CHLH}	8	Delay from CLKOUT rising edge to ALE rising edge	15	60	ns
t_{CLLL}	8	Delay from CLKOUT falling edge to ALE falling edge			ns
t_{CHAV}	8	Delay from CLKOUT rising edge to address valid			ns
t_{CHAX}	8	Address hold after CLKOUT rising edge			ns
Code Read Cycle					
t_{CHPL}	8	Delay from CLKOUT rising edge to $\overline{PSEN}$ asserted			ns
t_{CHPH}	8	Delay from CLKOUT rising edge to $\overline{PSEN}$ de-asserted			ns
t_{IVCH}	8	Instruction valid to CLKOUT rising edge			ns
t_{CHIX}	8	Instruction hold from CLKOUT rising edge			ns
t_{CHIZ}	8	Bus 3-State after CLKOUT rising edge (code read)			ns
Data Read Cycle					
t_{CHRL}	10	Delay from CLKOUT rising edge to $\overline{RD}$ asserted			ns
t_{CHRH}	10	Delay from CLKOUT rising edge to $\overline{RD}$ de-asserted			ns
t_{DVCH}	10	Data valid to CLKOUT rising edge			ns
t_{CHDX}	10	Data hold after CLKOUT rising edge			ns
t_{CHDZ}	10	Bus 3-State after CLKOUT rising edge (data read)			ns
Data Write Cycle					
t_{CHWL}	12	Delay from CLKOUT rising edge to $\overline{WR}$ asserted			ns
t_{CHWH}	12	Delay from CLKOUT rising edge to $\overline{WR}$ de-asserted			ns
t_{QVCH}	12	Data valid to CLKOUT rising edge			ns
t_{CHQX}	12	Data hold after CLKOUT rising edge			ns
t_{CHQZ}	12	Bus 3-State after CLKOUT rising edge (data write)			ns
Wait Input					
t_{CHWTH}	13	WAIT stable before CLKOUT rising edge			ns
t_{CHWTL}	13	WAIT hold after CLKOUT rising edge			ns

NOTES:
1. Load capacitance for all outputs = 50pF.
2. Variables V1 through V13 reflect programmable bus timing, which is programmed via the Bus Timing registers (BTRH and BTRL). Refer to the *XA User Guide* for details of the bus timing settings.
   - V1) This variable represents the programmed width of the ALE pulse as determined by the ALEW bit in the BTRL register. V1 = 0.5 if the ALEW bit = 0, and 1.5 if the ALEW bit = 1.
   - V2) This variable represents the programmed width of the $\overline{PSEN}$ pulse as determined by the CR1 and CR0 bits or the CRA1, CRA0, and ALEW bits in the BTRL register.
     - For a bus cycle with **no** ALE, V2 = 1 if CR1/0 = 00, 2 if CR1/0 = 01, 3 if CR1/0 = 10, and 4 if CR1/0 = 11. Note that during burst mode code fetches, $\overline{PSEN}$ does not exhibit transitions at the boundaries of bus cycles. V2 still applies for the purpose of determining peripheral timing requirements.
     - For a bus cycle **with** an ALE, V2 = the total bus cycle duration (2 if CRA1/0 = 00, 3 if CRA1/0 = 01, 4 if CRA1/0 = 10, and 5 if CRA1/0 = 11) minus the number of clocks used by ALE (V1 + 0.5) = 2.
       Example: if CRA1/0 = 10 and ALEW = 1, the V2 = 4 – (1.5 + 0.5) = 2.
   - V3) This variable represents the programmed length of an entire code read cycle **with** ALE. This time is determined by the CRA1 and CRA0 bits in the BTRL register. V3 = the total bus cycle duration (2 if CRA1/0 = 00, 3 if CRA1/0 = 01, 4 if CRA1/0 = 10, and 5 if CRA1/0 = 11).
   - V4) This variable represents the programmed length of an entire code read cycle with **no** ALE. This time is determined by the CR1 and CR0 bits in the BTRL register. V4 = 1 if CR1/0 = 00, 2 if CR1/0 = 01, 3 if CR1/0 = 10, and 4 if CR1/0 = 11.
   - V5) This variable represents the programmed length of an entire data read cycle with **no** ALE. This time is determined by the DR1 and DR0 bits in the BTRH register. V5 = 1 if DR1/0 = 00, 2 if DR1/0 = 01, 3 if DR1/0 = 10, and 4 if DR1/0 = 11.
   - V6) This variable represents the programmed length of an entire data read cycle **with** ALE. The time is determined by the DRA1 and DRA0 bits in the BTRH register. V6 = the total bus cycle duration (2 if DRA1/0 = 00, 3 if DRA1/0 = 01, 4 if DRA1/0 = 10, and 5 if DRA1/0 = 11).

V7) This variable represents the programmed width of the $\overline{RD}$ pulse as determined by the DR1 and DR0 bits or the DRA1, DRA0 in the BTRH register, and the SLEW bit in the BTRL register. Note that during a 16-bit operation on an 8-bit external bus, $\overline{RD}$ remains low and does not exhibit a transition between the first and second byte bus cycles. V7 still applies for the purpose of determining peripheral timing requirements. The timing for the first byte is for a bus cycle with ALE, the timing for the second byte is for a bus cycle with no ALE.
- For a bus cycle with **no** ALE, V7 = 1 if DR1/0 = 00, 2 if DR1/0 = 01, 3 if DR1/0 = 10, and 4 if DR1/0 = 11.
- For a bus cycle **with** an ALE, V7 = the total bus cycle duration (2 if DRA1/0 = 00, 3 if DRA1/0 = 01, 4 if DRA1/0 = 10, and 5 if DRA1/0 = 11) minus the number of clocks used by ALE (V1 + 0.5).
  Example: if DRA1/0 = 00 and ALEW = 0, then V7 = 2 – (0.5 +0.5) = 1.

V8) This variable represents the programmed width of the $\overline{WRL}$ and/or $\overline{WRH}$ pulse as determined by the WM1 bit in the BTRL register. V8 = 1 if WM1 = 0, and 2 if WM1 = 1.

V9) This variable represents the programmed address setup time for a write as determined by the data write cycle duration (defined by DW1 and DW0 or the DWA1 and DWA0 bits in the BTRH register), the WM0 bit in the BTRL register, and the value of V8.
- For a bus cycle **with** an ALE, V9 = the total bus write cycle duration (2 if DWA1/0 = 00, 3 if DWA1/0 = 01, 4 if DWA1/0 = 10, and 5 if DWA1/0 = 11) minus the number of clocks used by the $\overline{WRL}$ and/or $\overline{WRH}$ pulse (V8) minus the number of clocks used by data hold time (0 if WM0 = 0 and 1 if WM0 = 1).
  Example: If DWA1/0 = 10, WM0 = 1, and WM1 = 1, then V9 = 4 – 1 – 2 = 1.
- For a bus cycle with **no** ALE, V9 = the total bus cycle duration (2 if DW1/0 = 00, 3 if DW1/0 = 01, 4 if DW1/0 = 10, and 5 if DW1/0 = 11) minus the number of clocks used by the $\overline{WRL}$ and/or $\overline{WRH}$ pulse (V8), minus the number of clocks used by data hold time (0 if WMo = 0 and 1 if WM0 = 1).
  Example: If DW1/0 = 11, WM0 = 1, and WM1 = 0, then V9 = 5 – 1 – 1 = 3.

V10) This variable represents the length of a bus strobe for calculation of WAIT set-up and hold times. The strobe may be $\overline{RD}$ (for data read cycles), $\overline{WRL}$ and/or $\overline{WRH}$ (for data write cycles), or $\overline{PSEN}$ (for code read cycles), depending on the type of bus cycle being widened by WAIT. V10 = 2 for WAIT associated with a code read cycle using $\overline{PSEN}$. V10 = V8 for a data write cycle using $\overline{WRL}$ and/or $\overline{WRH}$. V10 = V7 – 1 for a data read cycle using $\overline{RD}$. This means that a single clock data read cycle cannot be stretched using WAIT. If WAIT is used to vary the duration of data read cycles, the $\overline{RD}$ strobe width must be set to be at least two clocks in duration. Also see Note 4.

V11) This variable represents the programmed write hold time as determined by the WM0 bit in the BTRL register. V11 0 if the WM0 bit = 0, and 1 if the WM0 bit = 1.

V12) this variable represents the programmed period between the end of the ALE pulse and the beginning of the $\overline{WRL}$ and/or $\overline{WRH}$ pulse as determined by the data write cycle duration (defined by the DWA1 and DWA0 bits in the BTRH register), the WM0 bit in the BTRL register, and the values of V1 and V8. V12 = the total bus cycle duration (2 if DWA1/0 = 00, 3 if DWA1/0 = 01, 4 if DWA1/0 = 10, and 5 if DWA1/0 = 11) minus the number of clocks used by the $\overline{WRL}$ and/or $\overline{WRH}$ pulse (V8), minus the number of clocks used by data hold time (0 if WM0 = 0 and 1 if WM0 = 1), minus the width of the ALE pulse (V1).
Example: If SWA1/0 = 11, WM0 = 1, WM1 = 0, and ALEW = 1, then V12 = 5 – 1 – 1 – 1.5 = 1.5.

V13) This variable represents the programmed data setup time for a write as determined by the data write cycle duration (defined by DW1 and DW0 or the DWA1 and DWA0 bits in the BTRH register), the WM0 bit in the BTRL register, and the values of V1 and V8.
- For a bus cycle **with** an ALE, V13 = the total bus cycle duration (2 if DWA1/0 = 00, 3 if DWA1/0 = 01, 4 if DWA1/0 = 10, and 5 if DWA1/0 = 11) minus the number of clocks used by the $\overline{WRL}$ and/or $\overline{WRH}$ pulse (V8), minus the number of clocks used by data hold time (0 if WM0 = 0 and 1 if WM0 = 1), minus the number of clocks used by ALE (V1 + 0.5).
  Example: If DWA1/0 = 11, WM0 = 1, WM1 = 1, and ALEW = 0, then V13 = 5 – 1 – 2 – 1 = 1.
- For a bus cycle with **no** ALE, V13 = the total bus cycle duration (2 if DW1/0 = 00, 3 if DW1/0 = 01, 4 if DW1/0 = 10, and 5 if DW1/0 = 11) minus the number of clocks used by the $\overline{WRL}$ and/or $\overline{WRH}$ pulse (V8), minus the number of clocks used by data hold time (0 if WM0 = 0 and 1 if WM0 = 1).
  Example: If DW1/0 = 01, WM0 = 1, and WM1 = 0, then V13 = 3 – 1 – 1 = 1.

3. Not all combinations of bus timing configuration values result in valid bus cycles. Please refer to the *XA User Guide* section on the External Bus for details.
4. When code is being fetched for execution on the external bus, a burst mode fetch is used that dows not have $\overline{PSEN}$ edges in every fetch cycle. This would be A3–A0 for an 8-bit bus, and A3–A1 for a 16-bit bus. Also, a 16-bit read operation conducted on an 8-bit wide bus similarly does not include two separate $\overline{RD}$ strobes. So, a rising edge on the low order address line (A0) must be used to trigger a WAIT in the second half of such a cycle.
5. This parameter is provided for peripherals that have the data clocked in on the falling edge of the $\overline{WR}$ strobe. This is not usually the case and in most applications this parameter is not used.
6. Please note that the XA-S3 requires that extended data bus hold time (WM0 = 1) to be used with external bus write cycles.

AC WAVEFORMS

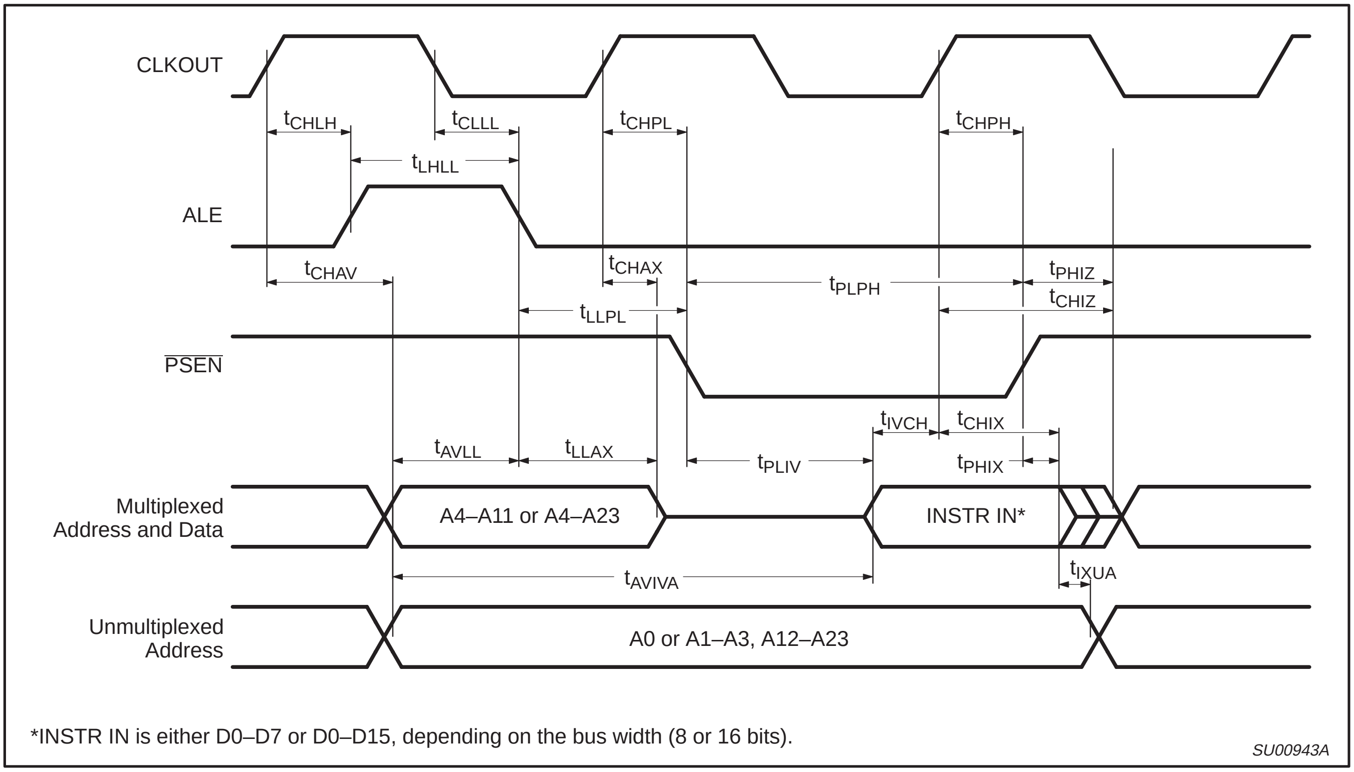


Figure 8. External Program Memory Read Cycle (ALE Cycle)

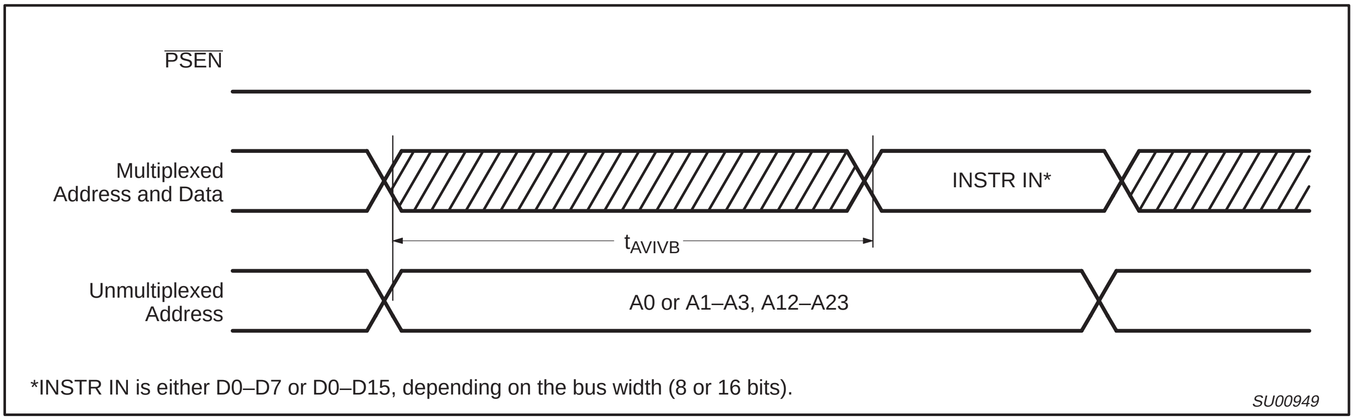


Figure 9. External Program Memory Read Cycle (Non-ALE Cycle)

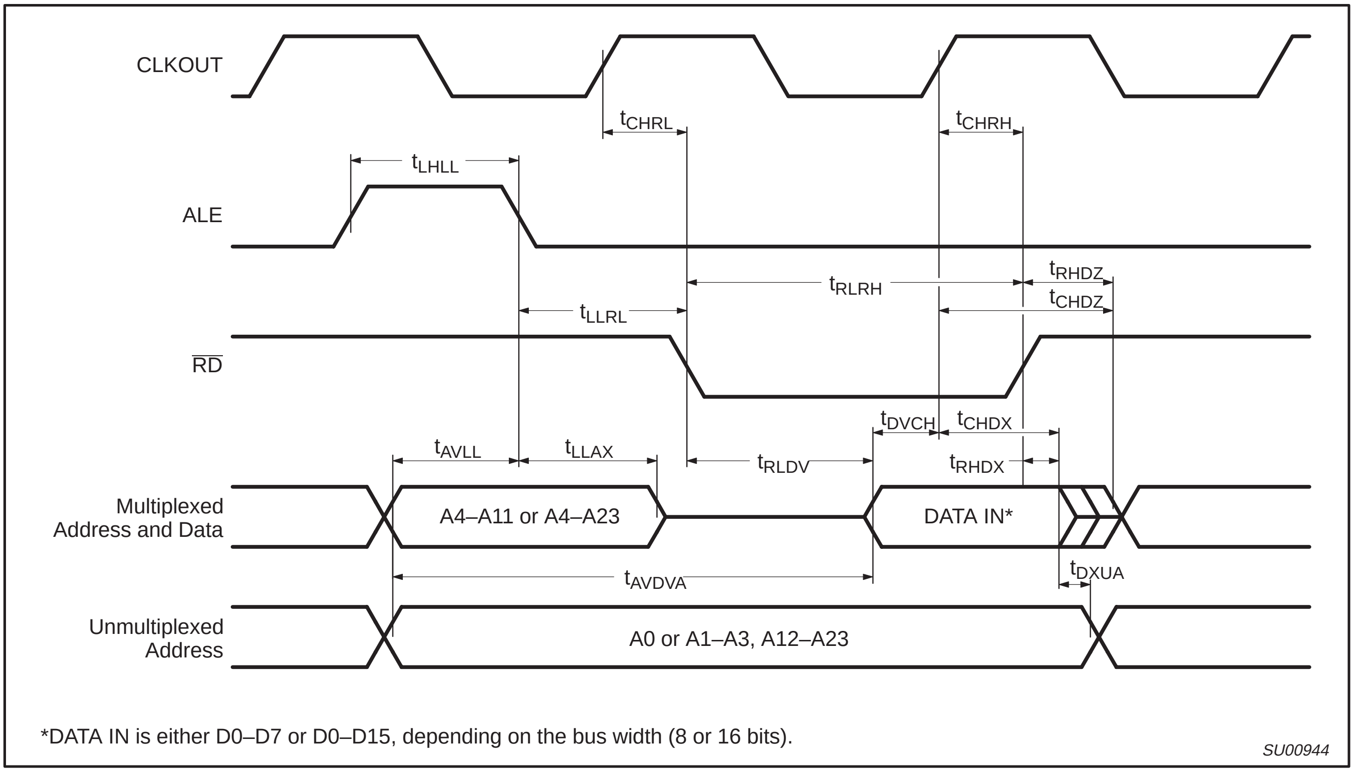


Figure 10. External Data Memory Read Cycle (ALE Cycle)

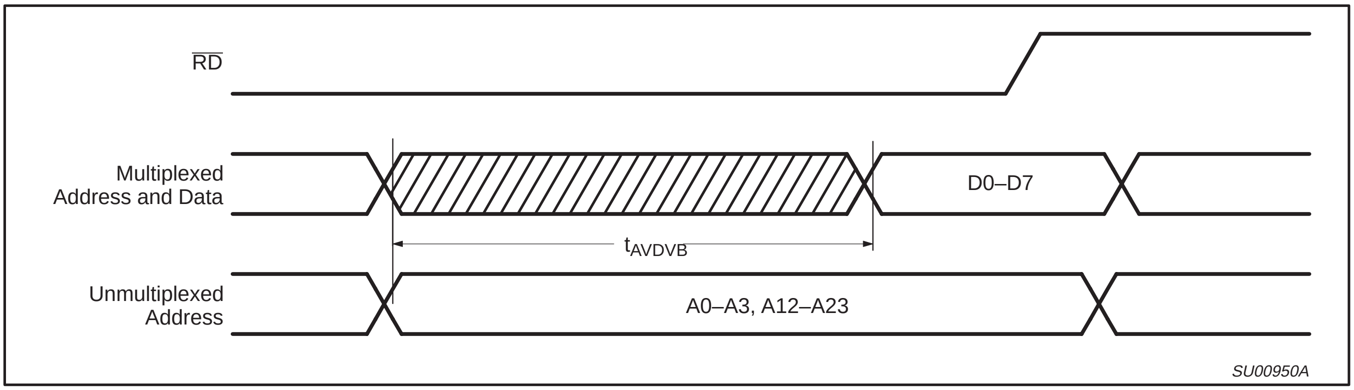


Figure 11. External Data Memory Read Cycle (Non-ALE Cycle)

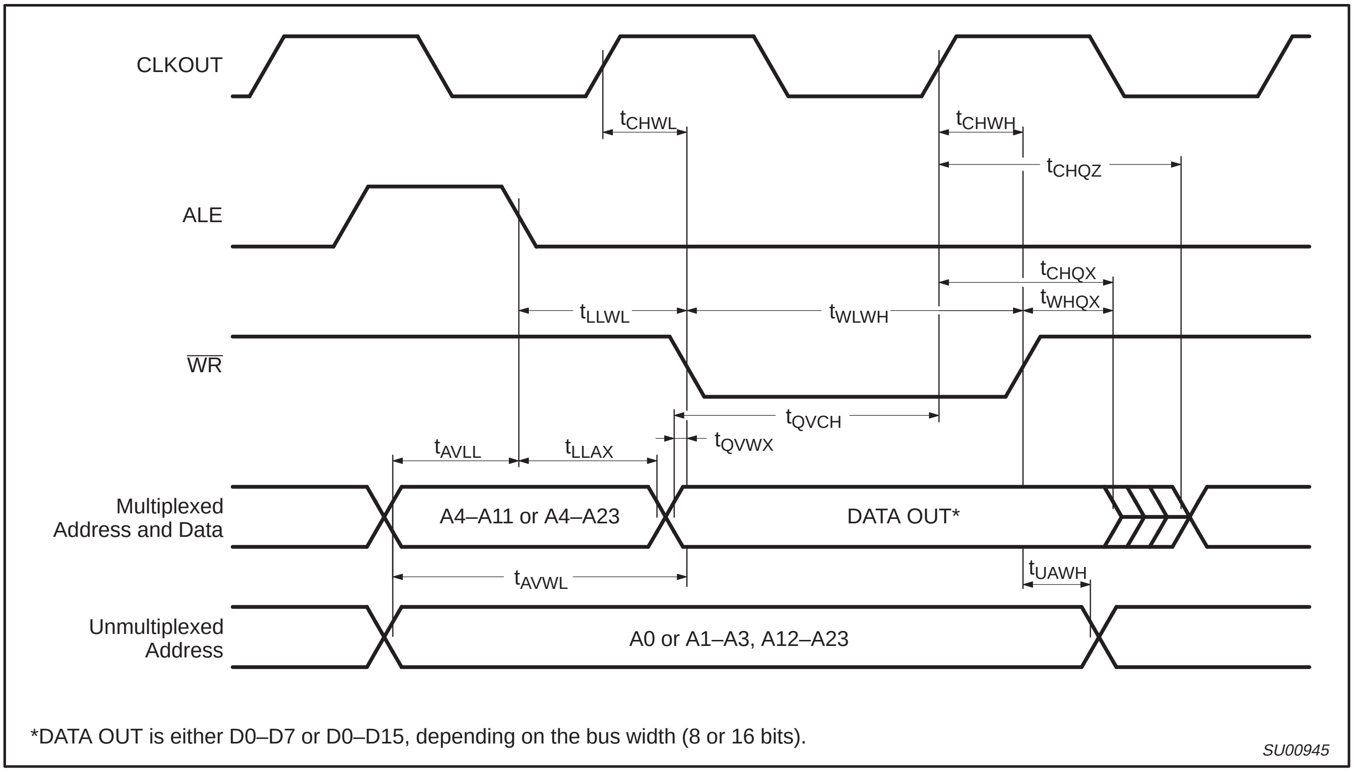


Figure 12. External Data Memory Write Cycle

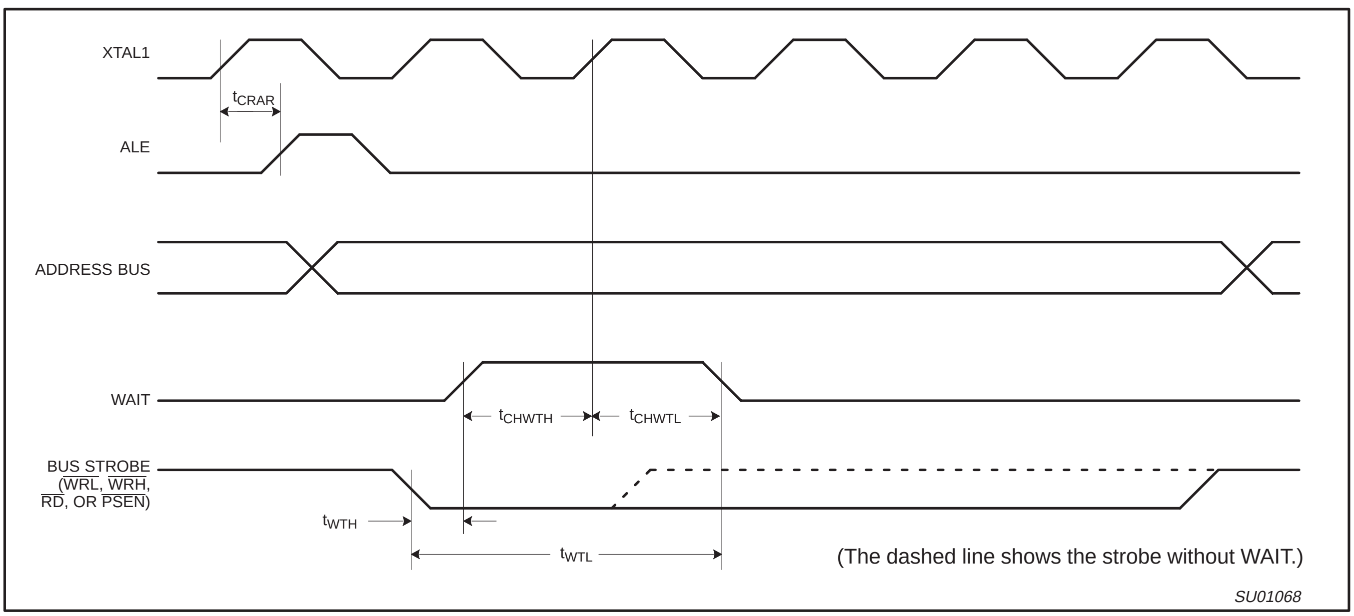


Figure 13. WAIT Signal Timing

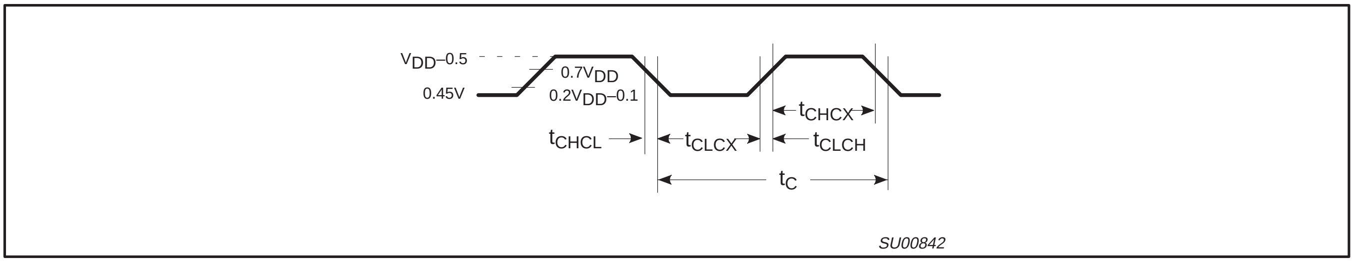


Figure 14. External Clock Drive

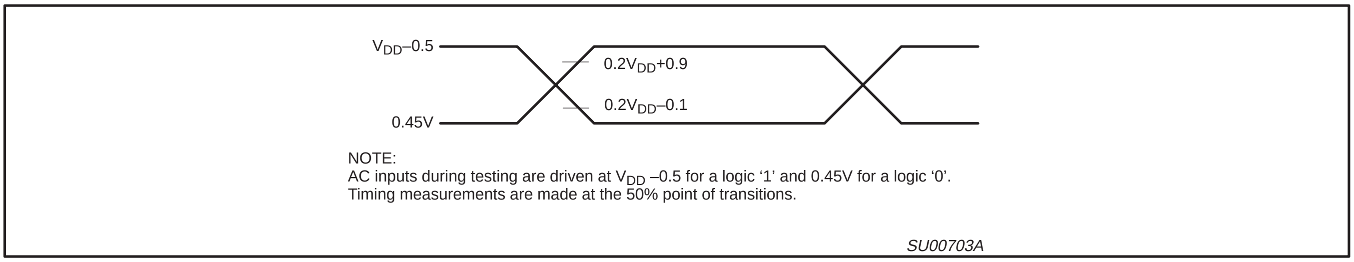


Figure 15. AC Testing Input/Output

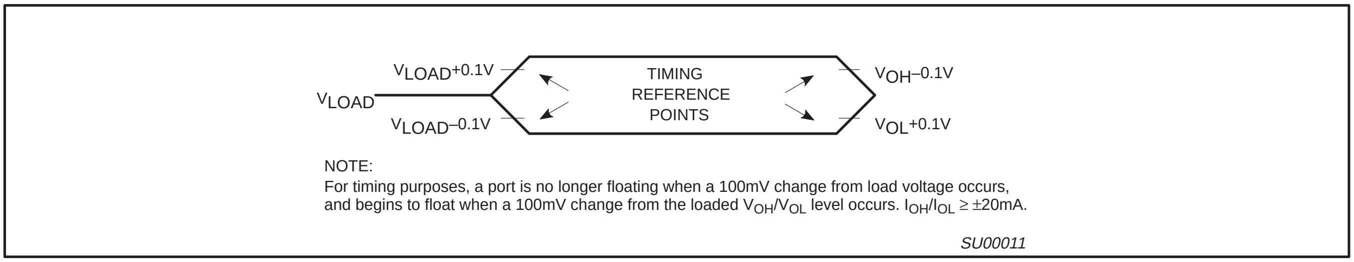


Figure 16. Float Waveform

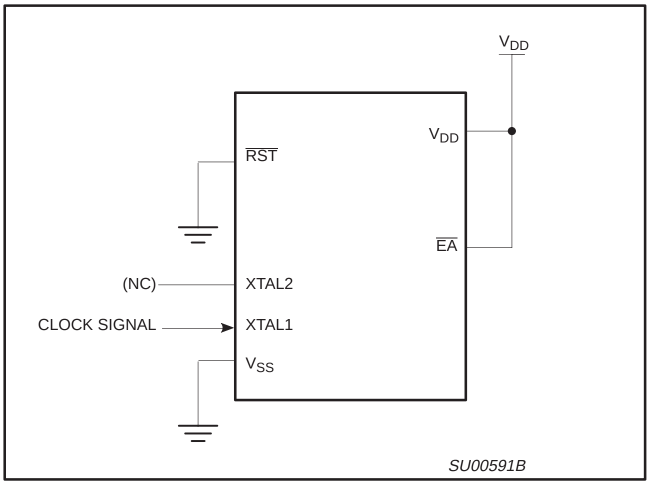


Figure 17. I_{DD} Test Condition, Active Mode
All other pins are disconnected

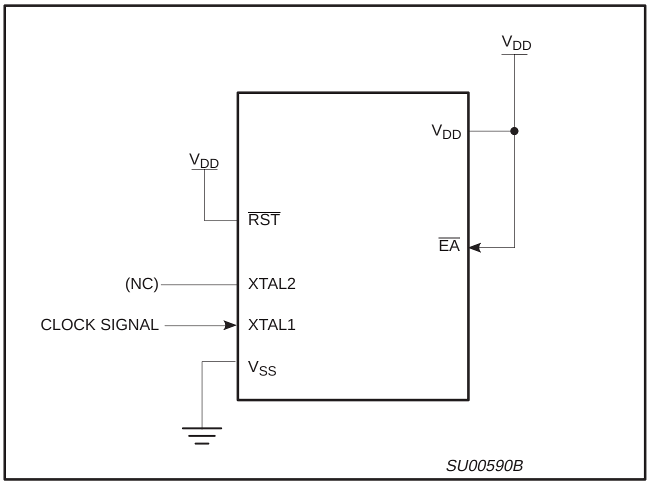


Figure 18. I_{DD} Test Condition, Idle Mode
All other pins are disconnected

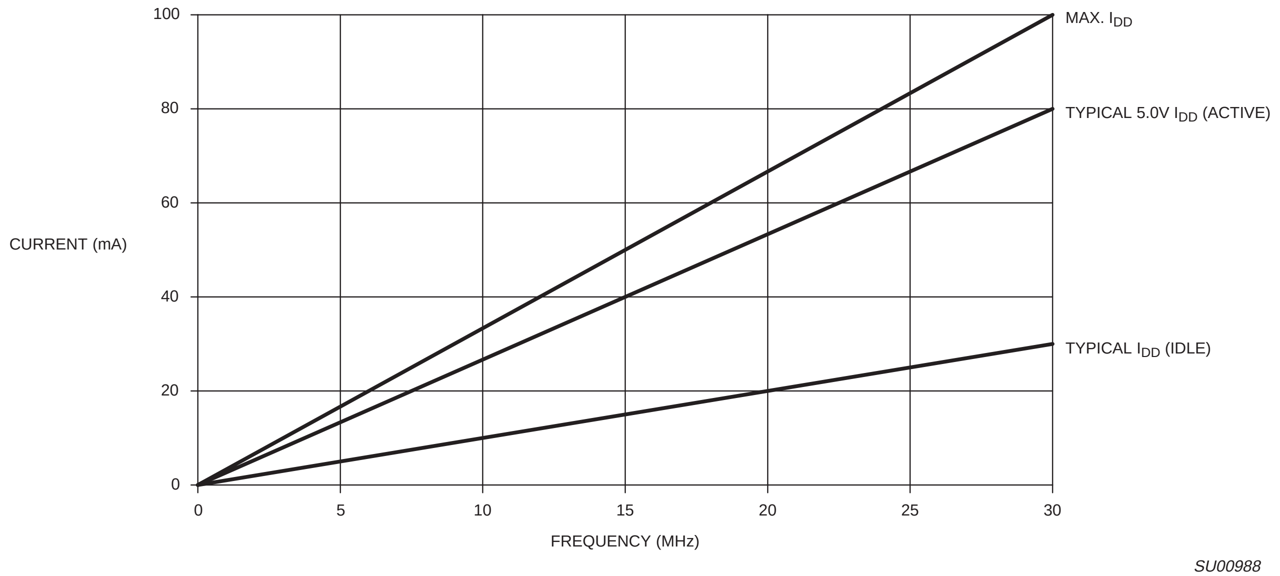


Figure 19. I_{DD} vs. Frequency
Valid only within frequency specification of the device under test.

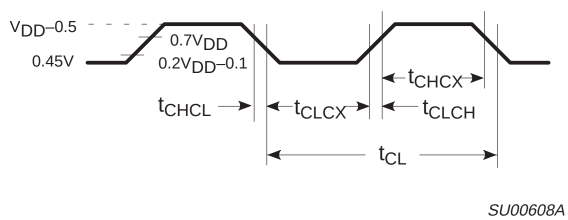


Figure 20. Clock Signal Waveform for I_{DD} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

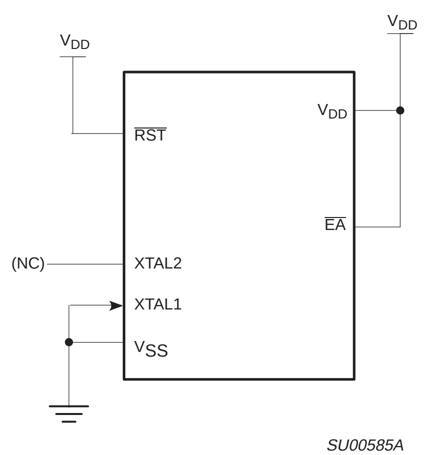


Figure 21. I_{DD} Test Condition, Power Down Mode
All other pins are disconnected. V_{DD}=2V to 5.5V

EPROM CHARACTERISTICS

The XA-S3 is programmed by using a modified Improved Quick-Pulse Programming™ algorithm. This algorithm is essentially the same as that used by 80C51 family EPROM parts. However different pins are used for many programming functions.

Detailed EPROM programming information may be obtained from the Internet at www.philipsmcu.com/ftp.html.

The XA-S3 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an XA-S3 manufactured by Philips.

Security Bits

With none of the security bits programmed the code in the program memory can be verified. When only security bit 1 is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. All further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled. (See Table 4.)

Table 4. Program Security Bits

PROGRAM LOCK BITS				
	SB1	SB2	SB3	PROTECTION DESCRIPTION
1	U	U	U	No Program Security features enabled.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled. Internal data RAM is not accessible.

NOTES:
1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

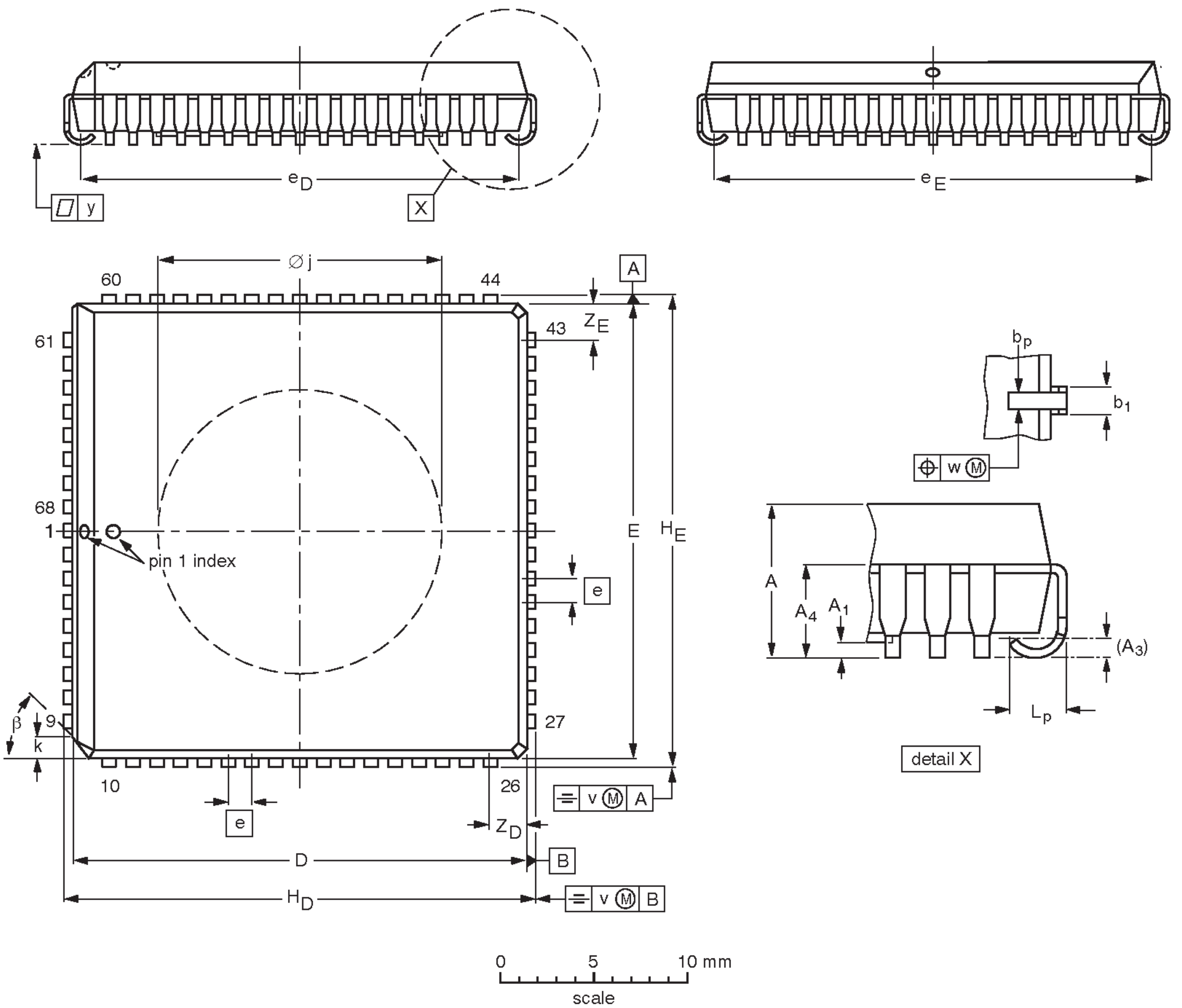
ROM CODE SUBMISSION

When submitting ROM code for the XA-S3, the following must be specified:
1. 32k byte user ROM data
2. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 7FFFH	DATA	7:0	User ROM Data
8020H	SEC	0	ROM Security Bit 1
8020H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security
8020H	SEC	3	ROM Security Bit 3 0 = enable security 1 = disable security

™Trademark phrase of Intel Corporation.

PLCC68: plastic leaded chip carrier; 68 leads; pedestal — SOT188-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

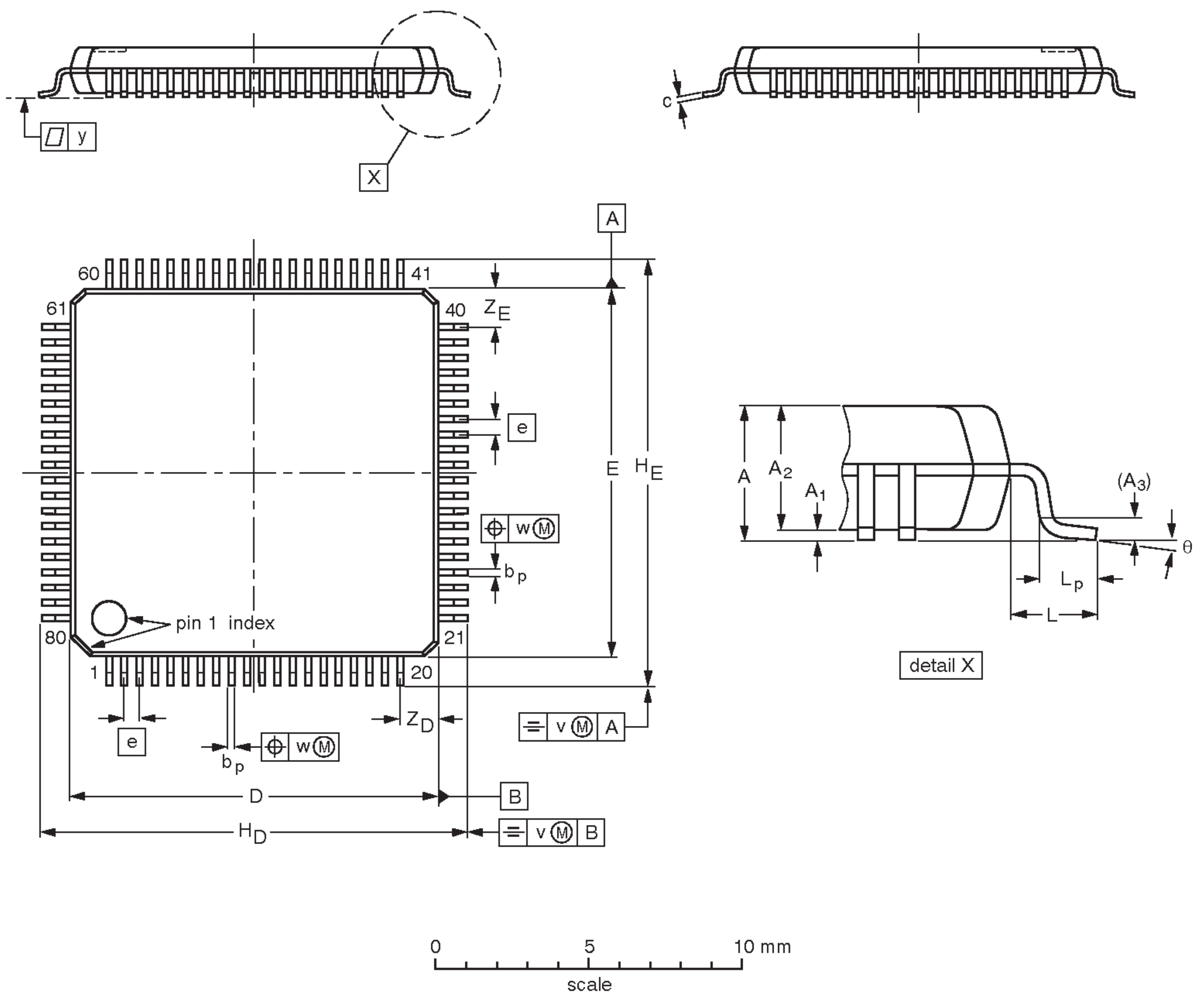
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	D(1)	E(1)	e	e_D	e_E	H_D	H_E	k	Ø j	L_p	v	w	y	Z_D(1) max.	Z_E(1) max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	15.34 15.19	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.604 0.598	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-3	112E10	MO-047AE				~~95-02-25~~ 97-12-16

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm SOT315-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~95-12-19~~ 97-07-15

NOTES

XA 16-bit microcontroller
32K/1K OTP/ROM/ROMless, 8-channel 8-bit A/D, low voltage (2.7V–5.5V), I^2C, 2 UARTs, 16MB address range

XA-S3

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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