PC910H0NSZ

High Speed Response , High CMR OPIC Photocoupler

■ Features

1. High resistance to noise due to high common rejection voltage (CMR:MIN. 10kV/μs)
2. High speed response (t_{pHL}, t_{pLH} MAX. 75ns)
3. Isolation voltage between input and output (Viso (rms):2.5kV)
4. 8-pin DIP package

■ Applications

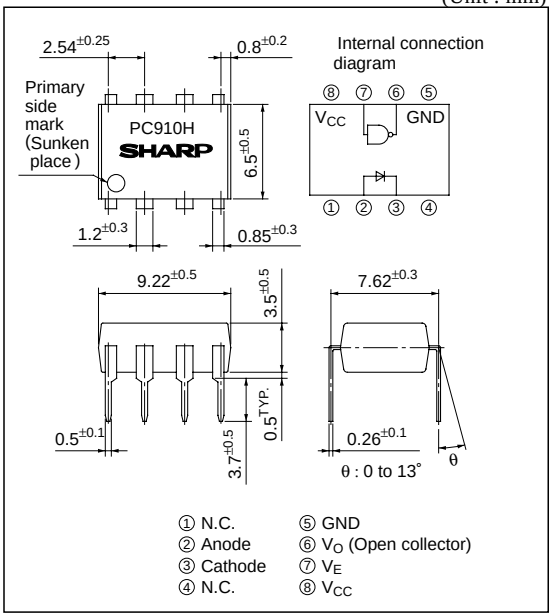
1. Programmable controllers
2. Inverters

■ Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Rating	Unit
Input	*1 Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P	40	mW
Output	Supply voltage	V_{CC}	7	V
	*2 Enable voltage	V_E	5.5	V
	High level output voltage	V_{OH}	7	V
	Low level output current	I_{OL}	50	mA
	*3 Collector power dissipation	P_C	85	mW
*4 Isolation voltage		$V_{iso\ (rms)}$	2.5	kV
Operating temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−55 to +125	°C
*5 Soldering temperature		T_{sol}	260	°C

*1 Refer to Fig.5
*2 Shall not exceed 500mV from supply voltage (V_{CC})
*3 Refer to Fig.7
*4 40 to 60%RH, AC for 1 min
*5 For 10 s

■ Outline Dimensions (Unit : mm)



* "OPIC"(Optical IC) is a trademark of the SHARP Corporation. An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Electro-optical Characteristics *6

(Unless otherwise spesified, Ta=–40 to 85°C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	Ta=25˚C, I_F=10mA	–	1.6	1.9	V
	Reverse current		I_R	Ta=25˚C, V_R=5V	–	–	10	μA
	Terminal capacitance		C_t	Ta=25˚C, V_F=0V, f=1MHz	–	60	150	pF
Output	High level output current		I_{OH}	V_{CC}=V_O=5.5V, V_E=2.0V, I_F=250μA	–	0.02	100	μA
	Low level output voltage		V_{OL}	V_{CC}=5.5V, V_E=2.0V, I_F=5mA, I_{OL}=13mA	–	0.4	0.6	V
	High level enable current		I_{EH}	V_{CC}=5.5V, V_E=2.0V	–	–0.5	–1.6	mA
	Low level enable current		I_{EL}	V_{CC}=5.5V, V_E=0.5V	–	–0.7	–1.6	mA
	High level supply current		I_{CCH}	V_{CC}=5.5V, I_F=0mA, V_E=2V	–	5	10	mA
				V_{CC}=5.5V, I_F=0mA, V_E=0.5V	–	5	–	mA
	Low level supply current		I_{CCL}	V_{CC}=5.5V, I_F=10mA, V_E=2V	–	7	13	mA
				V_{CC}=5.5V, I_F=10mA, V_E=0.5V	–	5.5	–	mA
Transfer characteristics	"High→Low" threshold input current		I_{FHL}	V_{CC}=5V, V_E=2.0V, V_O=0.8V, R_L=350Ω	–	2.5	5	mA
	Isolation resistance		R_{ISO}	Ta=25˚C, DC=500V, 40 to 60%RH	5×10^{10}	1×10^{11}	–	Ω
	Floating capacitance		C_f	Ta=25˚C, V=0V, f=1MHz	–	0.6	5	pF
	Response time	"High→Low" propagation delay time	t_{pHL}	Fig.3 Ta=25˚C, V_{CC}=5V, R_L=350Ω, C_L=15pF, I_F=7.5mA	25	48	75	ns
		"Low→High" propagation delay time	t_{pLH}		25	50	75	ns
		Rise time	t_r		–	10	–	ns
		Fall time	t_f		–	20	–	ns
		*7Pulse width distortion	t_W		–	–	35	ns
		"High→Low" enable propagation delay time	t_{EHL}	Fig.4 Ta=25˚C, V_{CC}=5V, R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3V, V_{EL}=0.5V	–	15	–	ns
		"Low→High" enable propagation delay time	t_{ELH}		–	10	–	ns
	CMR	Instantaneous common mode rejection voltage "Output : High level"	CM_H	Fig.5 Ta=25˚C, V_{CC}=5V, $V_{CM\ (P-P)}$=1kV, R_L=350Ω, I_F=0mA, V_O(Min)=2V	10	20	–	kV/μs
		Instantaneous common mode rejection voltage "Output : Low level"	CM_L	Fig.5 Ta=25˚C, V_{CC}=5V, $V_{CM\ (P-P)}$=1kV, R_L=350Ω, I_F=5mA, V_O(Max)=0.8V	–10	–20	–	kV/μs

*6 When measuring output and transfer characteristics, connect a by-pass capacitor (0.01μF or more) between V_{CC} ⑧ and GND ⑤ near the **PC910H0NSZ**

*7 *5 Pulse width distortion Δ tw=$|t_{pHL}-t_{pLH}|$

All typical values:at Ta=25˚C, V_{CC}=5V

Fig.1 Block Diagram

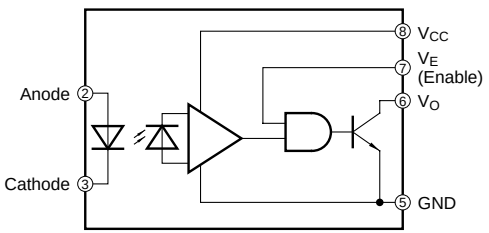
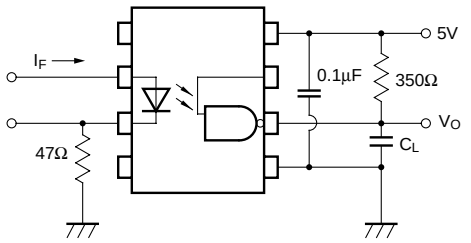


Fig.2 Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

L : Logic (0)
H : Logic (1)

Fig.3 Test Circuit for t_{pHL}, t_{pLH}, t_r and t_f



*C_L includes the probe and wiring capacitance.

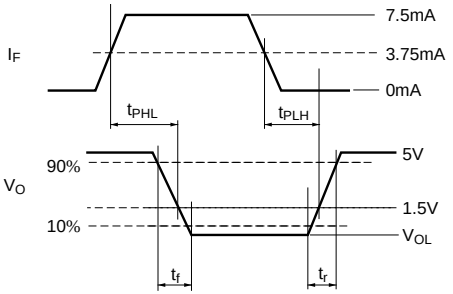
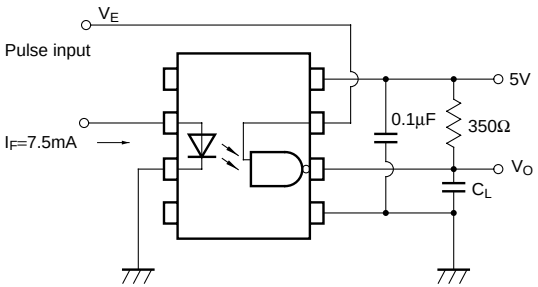


Fig.4 Test Circuit for t_{EHL} and t_{ELH}



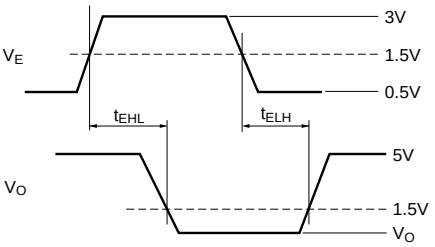
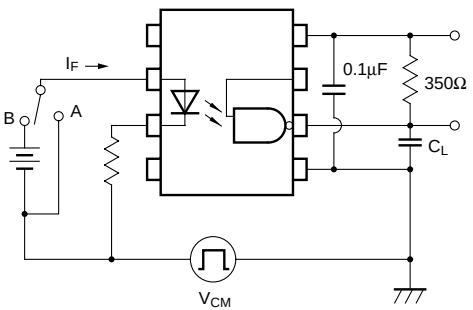


Fig.5 Test Circuit for CM_H and CM_L



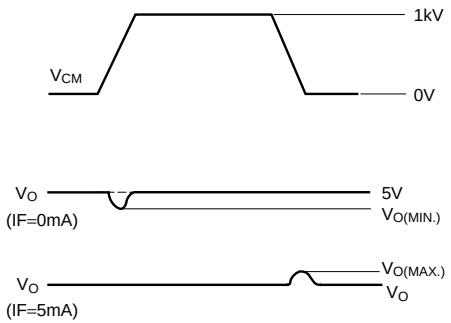


Fig.6 Forward Current vs. Ambient Temperature

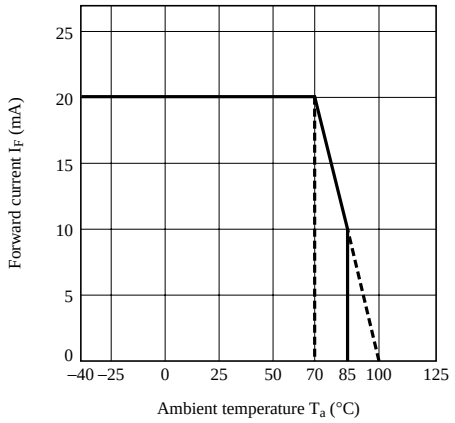
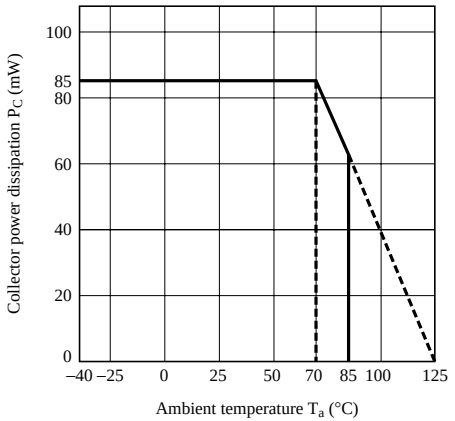


Fig.7 Collector Power Dissipation vs. Ambient Temperature



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