

PGA206
PGA207

High-Speed Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAINS:**
PGA206: $G=1, 2, 4, 8V/V$
PGA207: $G=1, 2, 5, 10V/V$
- **TRUE INSTRUMENTATION AMP INPUT**
- **FAST SETTLING:** $3.5\mu s$ to 0.01%
- **FET INPUT:** $I_B = 100pA$ max
- **INPUT PROTECTION:** $\pm 40V$
- **LOW OFFSET VOLTAGE:** $1.5mV$ max
- **16-PIN DIP, SOL-16 SOIC PACKAGES**

APPLICATIONS

- **MULTIPLE-CHANNEL DATA ACQUISITION**
- **MEDICAL, PHYSIOLOGICAL AMPLIFIER**
- **PC-CONTROLLED ANALOG INPUT BOARDS**

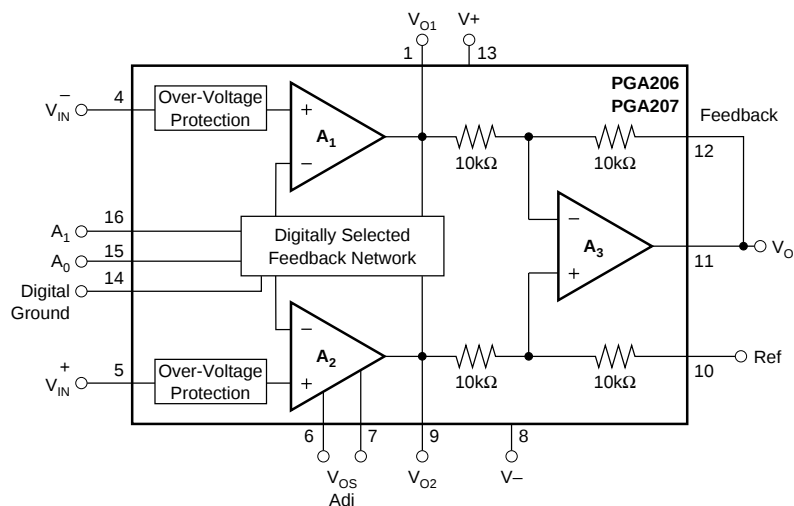
DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

The PGA206 and PGA207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate I_B errors due to analog multiplexer series resistance.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to $\pm 40V$, even with the power supplies off. The PGA206 and PGA207 are laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for $-40^\circ C$ to $+85^\circ C$ operation.



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Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

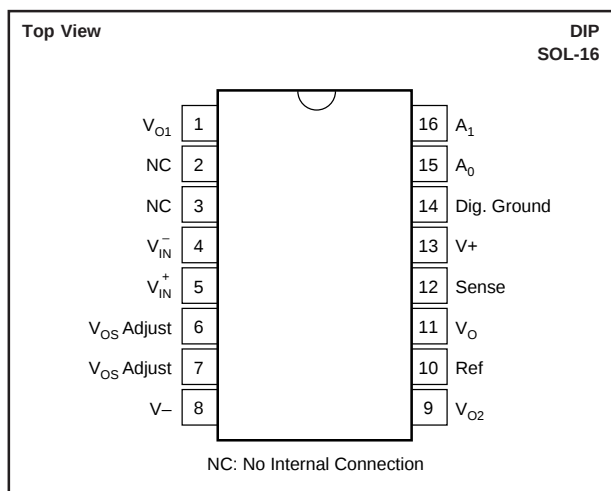
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_I = 2\text{k}\Omega$ unless otherwise noted.

* Specification same as PGA206P or PGA207P.

NOTES: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

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PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
PGA206PA	16-Pin Plastic DIP	180
PGA206P	16-Pin Plastic DIP	180
PGA206UA	SOL-16 Surface Mount	211
PGA206U	SOL-16 Surface Mount	211
PGA207PA	16-Pin Plastic DIP	180
PGA207P	16-Pin Plastic DIP	180
PGA207UA	SOL-16 Surface Mount	211
PGA207U	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	±V _S
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ORDERING INFORMATION

PRODUCT	GAINS	PACKAGE	TEMPERATURE RANGE
PGA206PA	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206P	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206UA	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA206U	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207PA	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207P	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207UA	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207U	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C



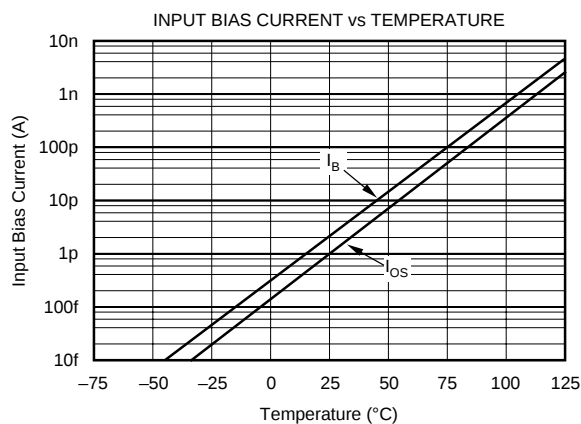
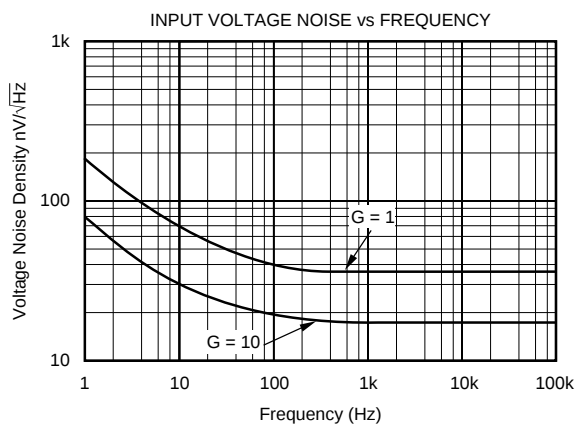
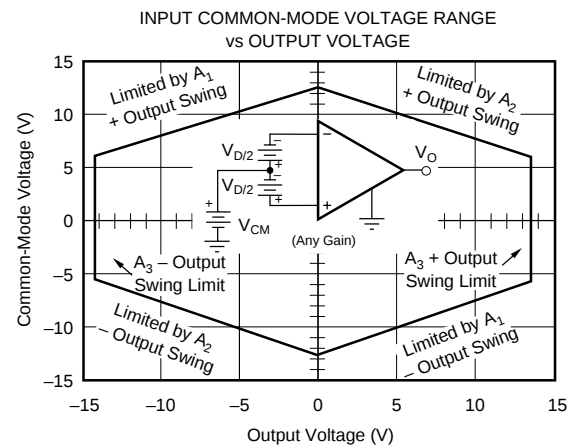
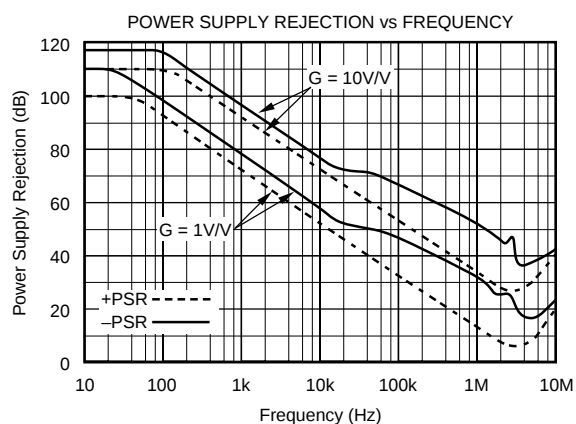
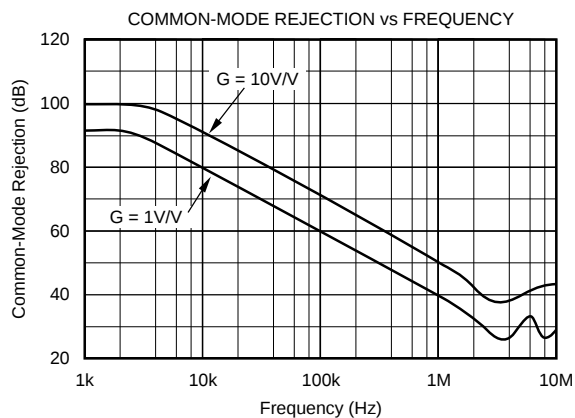
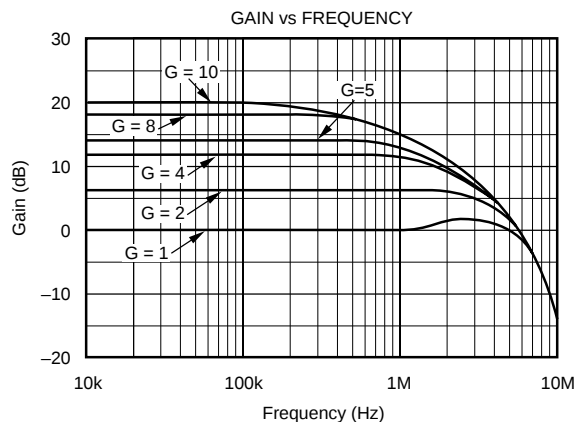
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

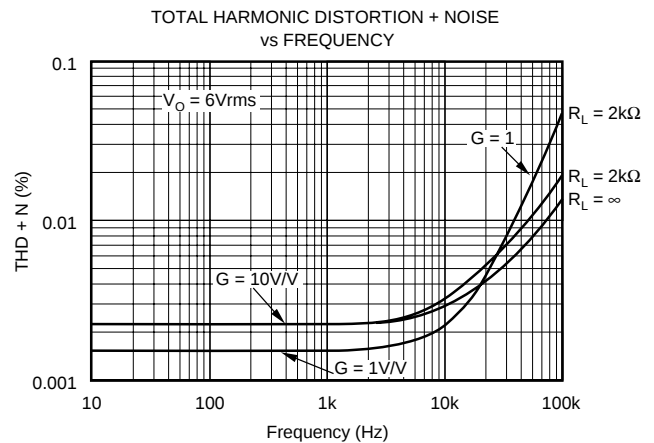
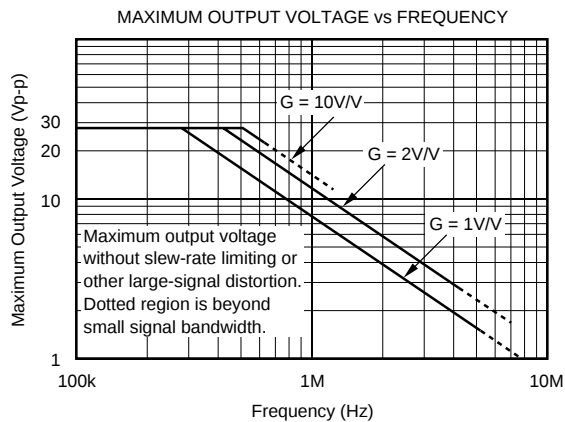
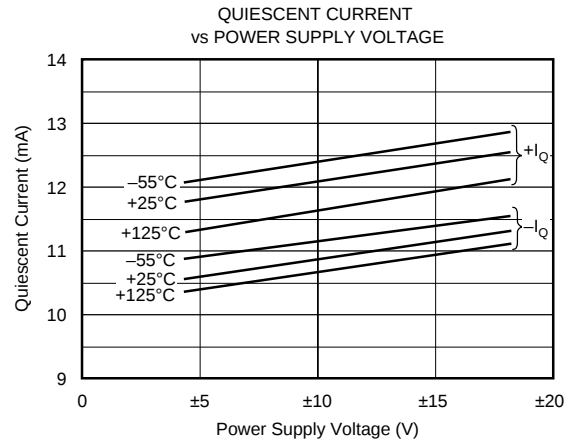
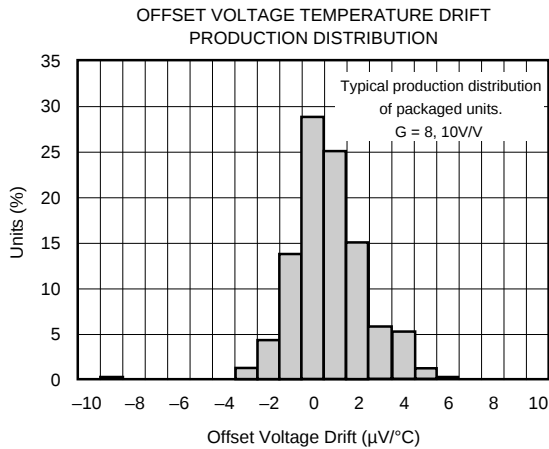
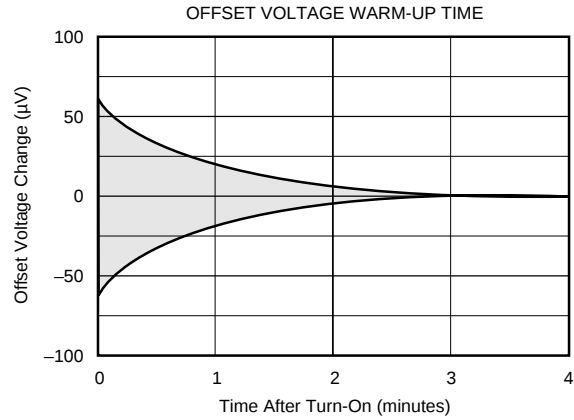
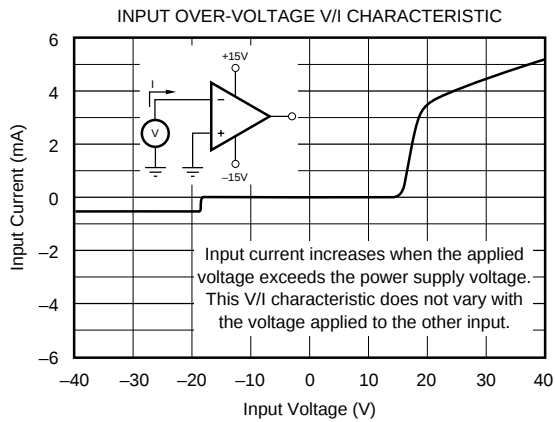
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

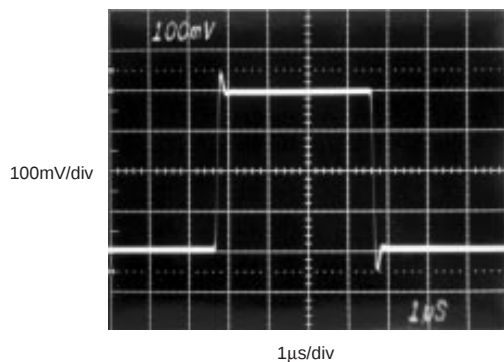
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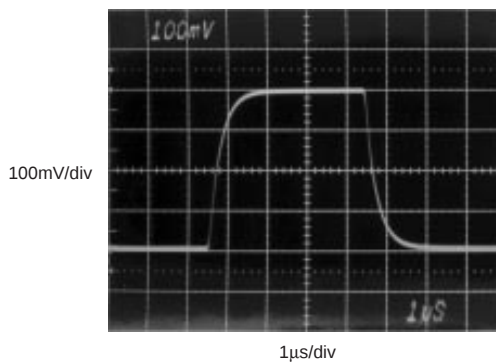
TYPICAL PERFORMANCE CURVES (CONT)

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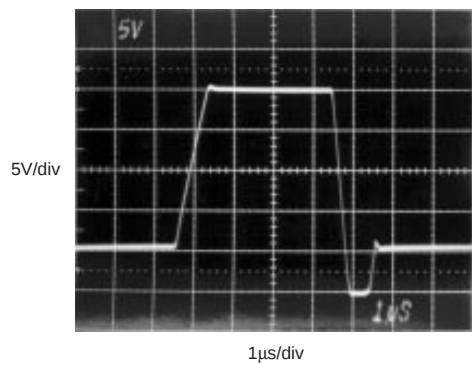
SMALL SIGNAL RESPONSE
 $G = 1$, $C_L = 50\text{pF}$



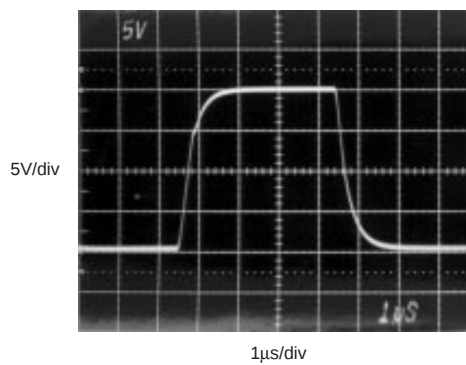
SMALL SIGNAL RESPONSE
 $G = 10$, $C_L = 50\text{pF}$



LARGE SIGNAL RESPONSE
 $G = 1$, $C_L = 50\text{pF}$



LARGE SIGNAL RESPONSE
 $G = 10$, $C_L = 50\text{pF}$



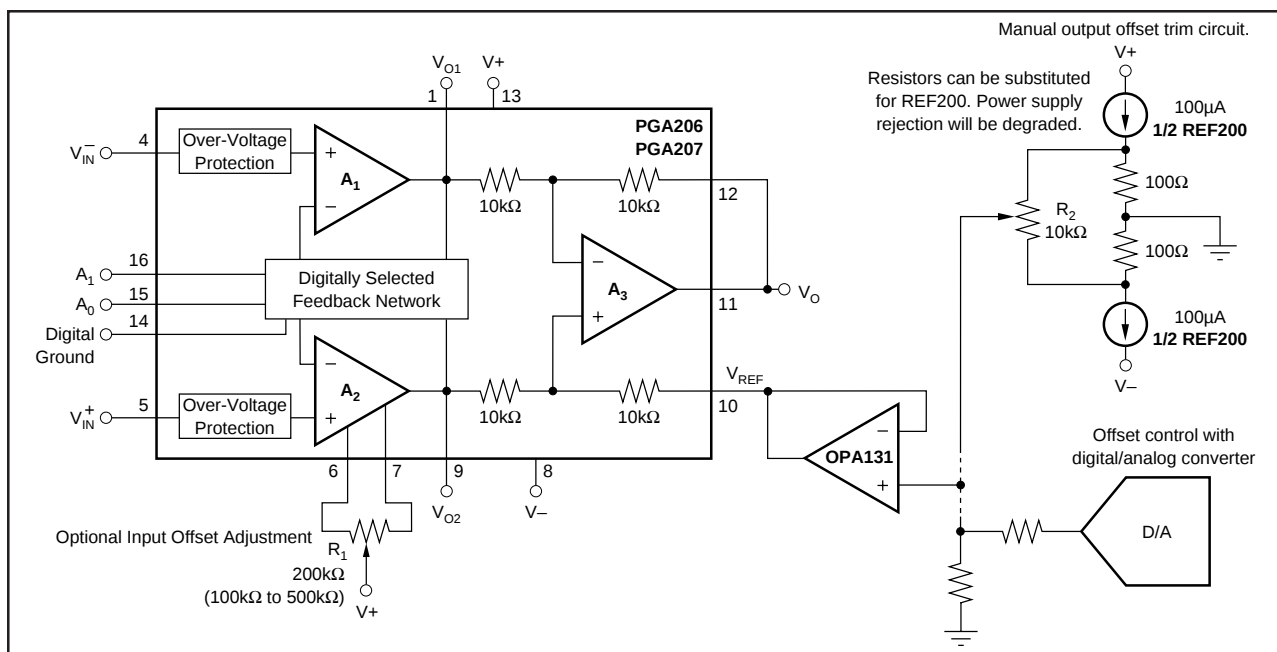


FIGURE 2. Optional Offset Voltage Trim Circuits.

R_1 adjusts the offset of the input amplifiers. Output stage offset is adjusted with R_2 . A buffer op amp is required in the output offset adjustment circuit, as shown, to assure that the Ref pin is driven by a low source impedance. To adjust for low offset voltage in all gains, first adjust the input stage offset in the highest gain. Then adjust the output stage offset (R_2) in $G = 1$. Iterate the adjustments for lowest offset in all gains.

Offset can also be adjusted under processor control with a D/A converter as shown in Figure 2. The D/A's output voltage can be reduced with a resistor divider for better adjustment resolution, but an op amp buffer following the divider is required to provide a low source impedance to the ref terminal. A different offset value is required for each amplifier gain.

INPUT BIAS CURRENT RETURN PATH

The FET inputs of the PGA206 and PGA207 provide extremely high input impedance. Still, a path must be provided for the bias current of each input. Figure 3 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the linear input voltage range and the input amplifiers will saturate.

If the differential source resistance is low, a bias current return path can be connected to only one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 3). These applications do not require additional resistor(s) for proper operation.

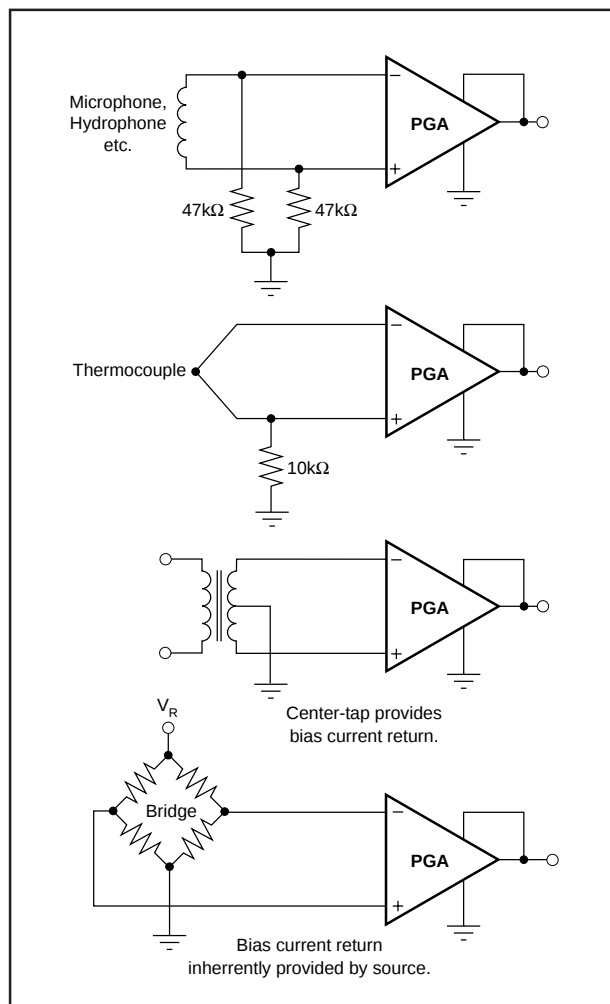


FIGURE 3. Providing an Input Bias Current Path.

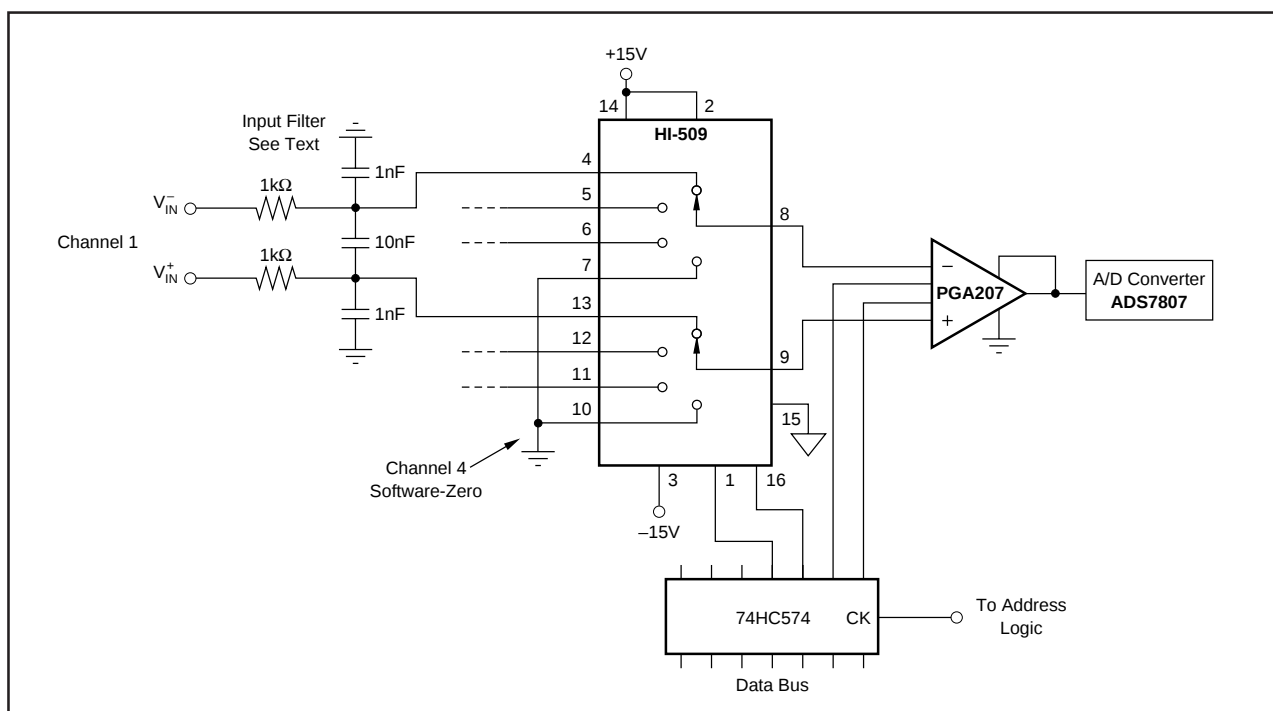


FIGURE 4. Multiplexed-Input Signal Acquisition System.

INPUT COMMON-MODE RANGE

The linear input voltage range of the PGA206 and PGA207 is from approximately 2.3V below the positive supply voltage to 1.5V above the negative supply. As a differential input voltage causes output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2 . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage”.

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA206 or PGA207 will be near 0V even though both inputs are overloaded. This condition can be detected by sensing the voltage on the V_{O1} and V_{O2} pins to determine whether they are within their linear operating range.

INPUT PROTECTION

The inputs of the PGA206 and PGA207 are individually protected for voltages up to $\pm 40V$. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value. The typical performance curve “Input Overload V/I Characteristic” shows this behavior. The inputs are protected even if no power supply voltage is applied.

MULTIPLEXED INPUTS

The PGA206 and PGA207 are ideally suited for multiple channel data acquisition. Figure 4 shows a typical application with an analog multiplexer used to connect one of four differential input signals to a single PGA207.

Careful circuit layout will help preserve accuracy of multiplexed signals. Run the inverting and non-inverting connections of each channel parallel to each other over a ground plane, or directly adjacent on top and bottom of the circuit board. Grounded guard traces between channels help reduce stray signal pick-up.

Multiplexed signals from high impedance sources require special care. As inputs are switched by the multiplexer, charge can be injected into the source, disturbing the input signal. Since many such sources involve slow signals, a simple R/C filter at the input can be used to dramatically reduce this effect. The arrangement shown filters both the differential signal and common-mode noise.

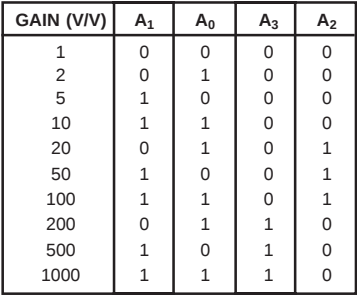


FIGURE 6. Wide Gain Range Programmable IA.

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