

DATA SHEET

**P83CL883; P87CL883;
P83CL884; P87CL884**
TELX microcontrollers for CT0
handset/basestation applications

Preliminary specification
File under Integrated Circuits, IC20

1997 Aug 18

**TELX microcontrollers for CT0
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**P83CL883; P87CL883;
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1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
 - minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
 - non-page oriented instructions
 - direct addressing
 - four 8-byte RAM register banks
 - stack depth limited only by available internal RAM (maximum 256 bytes)
 - multiply, divide, subtract and compare instructions
- 8-bit ports:
 - P83CL883 and P87CL883: 3 (19 I/O lines)
 - P83CL884 and P87CL884: 3 (18 I/O lines)
- Program Memory:
 - P87CL883/P87CL884: 8 kbytes One Time Programmable (OTP)
 - P83CL883/P83CL884: 8 kbytes ROM
- 256 bytes RAM
- 128 bytes EEPROM Data Memory, accessed internally via I²C-bus interface (P83CL884 and P87CL884 only)
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
 - edge or level sensitive triggering selectable via software
 - power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator (P83CL884/P87CL884 only)
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Watchdog Timer

- Full duplex enhanced UART with double buffering
- I²C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency range: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pins SO package.

2 GENERAL DESCRIPTION

The P8xCL883/P8xCL884 - denoting the P83CL883; P87CL883; P83CL884 and P87CL884 - are manufactured in an advanced CMOS technology. The P83CL883 and P87CL883 are based on single chip technology and the P83CL884 and P87CL884 are based on MCM (Multi-Chip-Module) technology as the EEPROM is integrated on a separate chip.

The P8xCL883/P8xCL884 are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1, CT1+ standards). For this purpose, features like DTMF, EEPROM, MSK modem and POR/LVD are integrated on-chip.

The device is optimized for low power consumption. The P8xCL883/P8xCL884 have two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL883/P8xCL884 is based on that of the 8051. The P8xCL883/P8xCL884 also function as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. Due to the missing port P2, there is no external data or memory access and the MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL883/P8xCL884; for details of the P8xCL883/P8xCL884 core and the derivative functions see the "TELX family" data sheet and "Data Handbook IC20; 80C51-based 8-bit Microcontrollers".

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3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL883DDT	SO28 ⁽¹⁾	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL883DDT			
P83CL884DDT			
P87CL884DDT			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

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4 BLOCK DIAGRAM

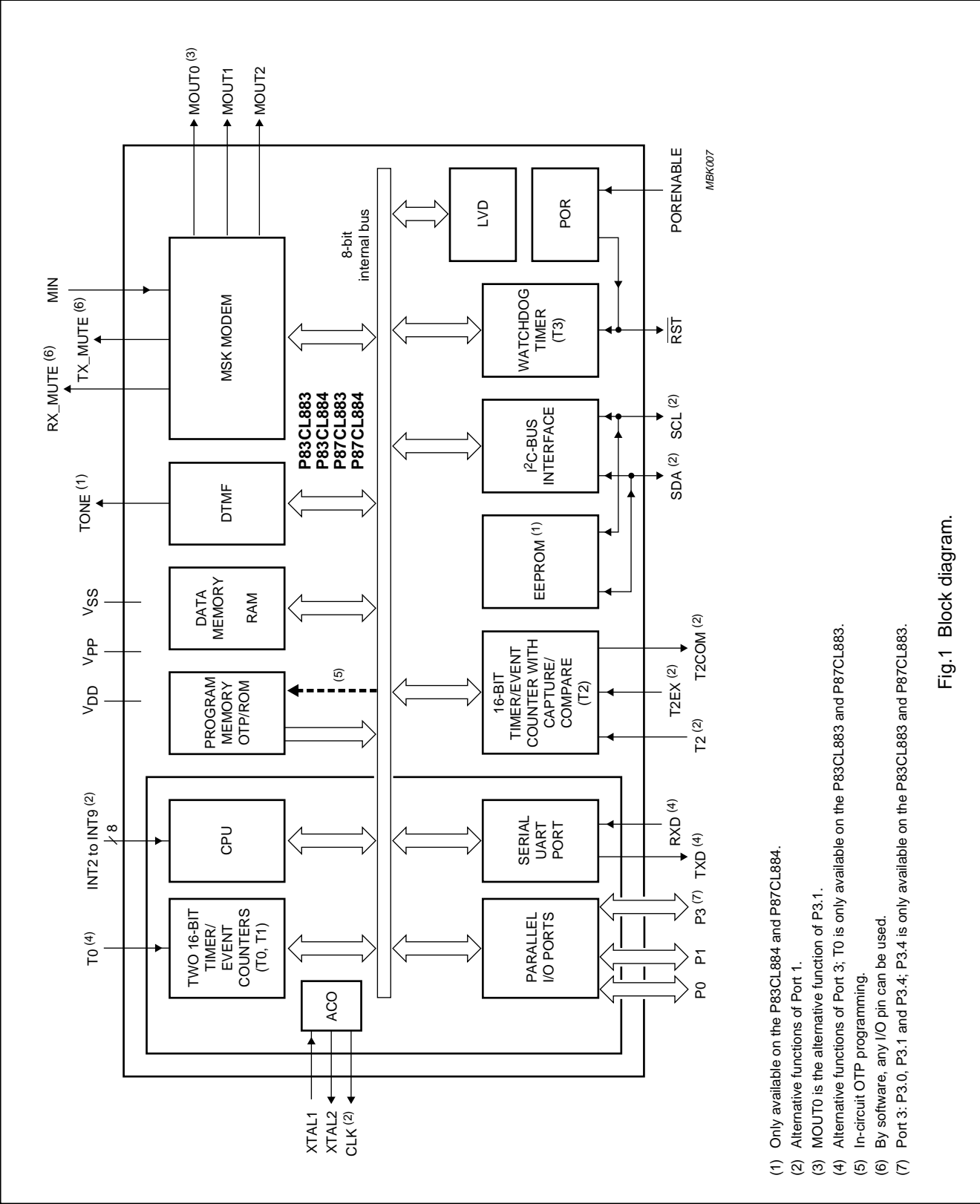


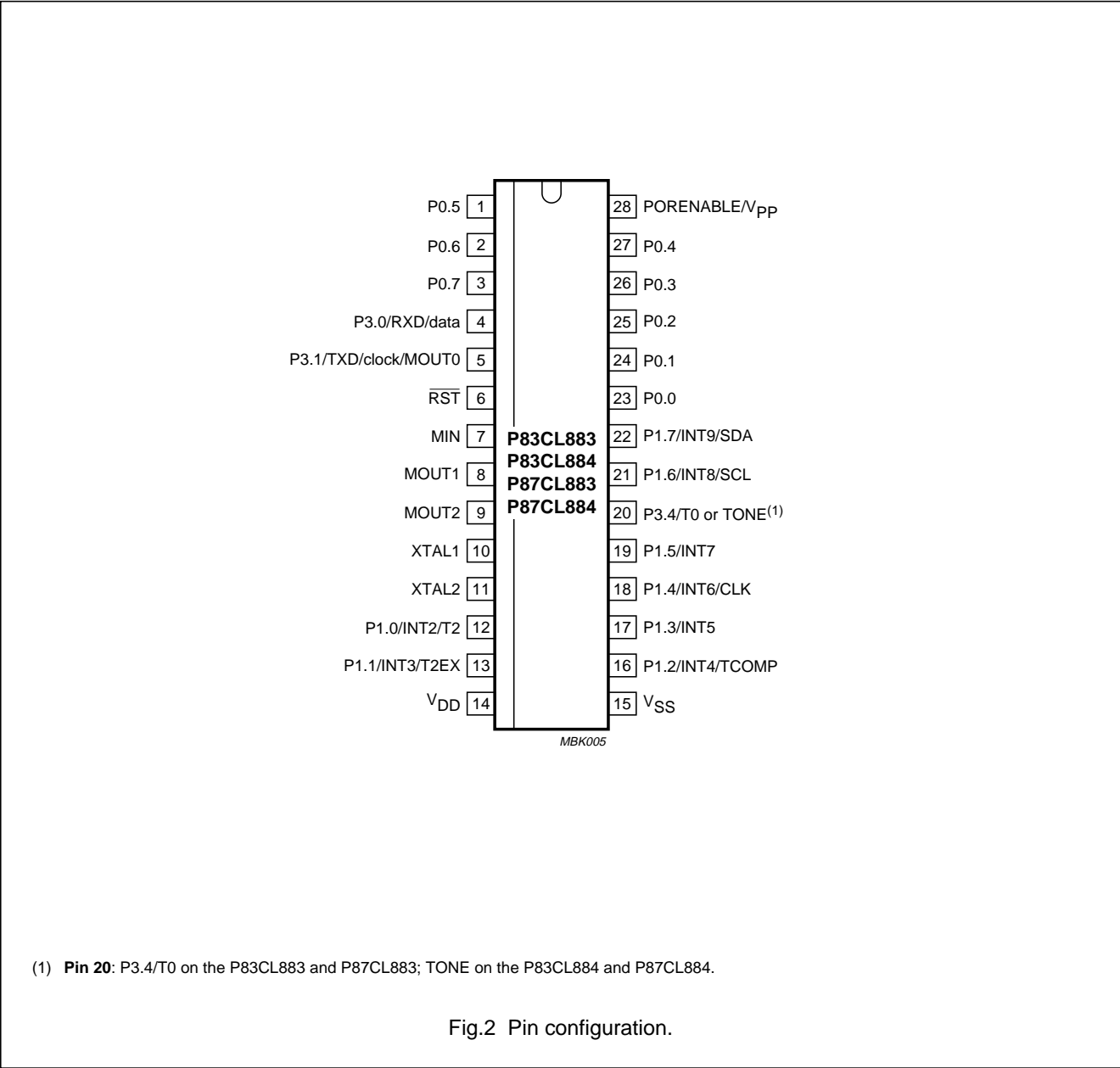
Fig.1 Block diagram.

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5 PINNING INFORMATION

5.1 Pinning



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5.2 Pin description

SYMBOL	PIN	DESCRIPTION
$\overline{\text{RST}}$	6	Active low reset: a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{\text{RST}}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital MSK modem input.
MOUT1	8	Digital MSK modem outputs.
MOUT2	9	
XTAL1	10	Crystal input: Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	Crystal output: Output of the Amplitude Controlled Oscillator. To be left non-connected when an external oscillator clock is used.
V _{DD}	14	Power supply.
V _{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	Port 0: 8-bit bidirectional I/O port. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	Port 1: 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I ² C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: INT2 to INT9 interrupts; Timer T2 external inputs T2 and T2EX ; Timer T2 compare output T2COMP ; external clock output CLK ; I ² C-bus clock SCL and data in/outputs SDA .
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	Port 3: 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: RXD/data is the serial port receiver data input (asynchronous) or data I/O (synchronous); TXD/clock is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output MOUT0 ; T0 is an external input for Timer 0. P3.4/T0 is only available on the P83CL883 and P87CL883.
P3.1/TXD/clock/ MOUT0	5	
P3.4/T0	20	
TONE	20	DTMF output; TONE is only available on the P83CL884 and P87CL884.
PORENABLE/V _{PP}	28	PORENABLE: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V _{PP} .

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6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers (SFRs)

Table 1 List of SFRs

REGISTER	ADDRESS (HEX)	RESET VALUE ⁽¹⁾ (MSB..LSB)
80C51 core		
ACC	E0	0000 0000
B	F0	0000 0000
DPL	82	0000 0000
DPH	83	0000 0000
PCH	no SFR	0000 0000
PCL	no SFR	0000 0000
PCON	87	0000 0000
PRESC	F3	0000 0000
PSW	D0	0000 0000
SP	81	0000 0111
T0/T1		
TCON	88	0000 0000
TH0	8C	0000 0000
TH1	8D	0000 0000
TL0	8A	0000 0000
TL1	8B	0000 0000
TMOD	89	0000 0000
Port		
ALTP	A3	0000 0000
P0	80	1111 1111
P0CFGA	8E	1111 1111
P0CFGB	8F	0000 0000
P1	90	1111 1111
P1CFGA	9E	0011 1111
P1CFGB	9F	0000 0000
P3	B0	XXX1XX11
P3CFGA	BE	XXX1XX11
P3CFGB	BF	XXX0XX00
P4	C1	XXXXXXX0
TIMER2		
COMP2H	AB	0000 0000
COMP2L	AA	0000 0000
RCAP2H	CB	0000 0000
RCAP2L	CA	0000 0000

REGISTER	ADDRESS (HEX)	RESET VALUE ⁽¹⁾ (MSB..LSB)
T2CON	C8	0000 0000
TH2	CD	0000 0000
TL2	CC	0000 0000
EEPROM interface		
EECON	FB	0000 0000
DTMF		
HGF	A2	0000 0000
LGF	A1	0000 0000
Interrupt logic		
IEN0	A8	0000 0000
IEN1	E8	0000 0000
IEN2	F1	0000 0000
IP0	B8	0000 0000
IP1	F8	0000 0000
IP2	F9	0000 0000
ISE1	E1	0000 0000
IX1	E9	0000 0000
IRQ1	C0	0000 0000
LVD		
LVDCON	F2	0000 0000
POR/ACO		
RSTAT	E6	XXX01001 ⁽²⁾
MSK		
MCON	D3	0000 0000
MBUF	D1	XXXXXXXX
MSTAT	D2	XX00 0000
UART		
S0BUF	99	0000 0000
S0CON	98	0000 0000
I²C-bus		
S1ADR	DB	0000 0000
S1CON	D8	0000 0000
S1DAT	DA	0000 0000
S1STA	D9	1111 1000

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REGISTER	ADDRESS (HEX)	RESET VALUE ⁽¹⁾ (MSB..LSB)
WDT		
WDCON	A5	10100101
WDTIM	FF	00000000
OTP interface		
OAH	D5	X00XXXXX
OAL	D4	XXXXXXXX
ODATA	D6	XXXXXXXX
OISYS	DC	000X0000
OTEST	D7	00000000
Reserved locations; do not write		
reserved	E7, FD	—

Notes

- Where: X = undefined state or not implemented bit.
- Defined by VIA mask.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL883 and P8xCL884 have 19 and 18 I/O lines respectively, treated as 19 and 18 individually addressable bits or as three parallel 8-bit addressable ports. The alternative functions are detailed below:

Port 0 Offers no alternative function.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I²C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 are serial port receiver input and transmitter output (UART)
- P3.4/T0 as counter input; available only in P8xCL883.

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor 'p1' is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter IN1. This inverter and transistor 'p3' form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in port configuration SFRs. There are 2 SFRs for each port, called PnCFGa and PnCFGb, where 'n' indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins. For instance, the output type of Port 1 pin 3 is controlled by the setting of bit 3 in the SFRs P1CFGa and P1CFGb.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

- Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; see Fig.3b. Except for the I²C pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.
- Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up 'p1' is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through 'p2' and 'very weakly' driven through 'p3' (see Fig.3b).
- Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome (see Fig.3c).

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Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs (see Fig.3d).

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 3.

Tables 2 and 3 show the configuration register settings for the 4 port output types.

Table 2 Port Configuration Registers PnCFGA and PnCFGB (n = 0 to 3) settings

MODE ⁽¹⁾	PnCFGA	PnCFGB	PORT OUTPUT MODE	
			NORMAL PORTS	I ² C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 3 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 output data ⁽¹⁾	P0	80	1111 1111
Port P0 configuration A	P0CFGA	8E	1111 1111
Port P0 configuration B	P0CFGB	8F	0000 0000
Port P1 output data ⁽¹⁾	P1	90	1111 1111
Port P1 configuration A	P1CFGA	9E	0011 1111
Port P1 configuration B	P1CFGB	9F	0000 0000
Port P3 output data ⁽¹⁾	P3	B0	XXX1 XX11 ⁽²⁾
Port P3 configuration A	P3CFGA	BE	XXX1 XX11 ⁽²⁾
Port P3 configuration B	P3CFGB	BF	XXX0 XX00 ⁽²⁾

Note

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode 1 (quasi-bidirectional, driving a weak HIGH) and the I²C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).
2. Port pin P3.4 is only available on P8xCL883.

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6.2.3 ALTERNATIVE PORT FUNCTION REGISTER (ALTP)

This 4-bit register controls the alternative function of some port pins.

Table 4 Alternative Port Function Register (SFR address A3H)

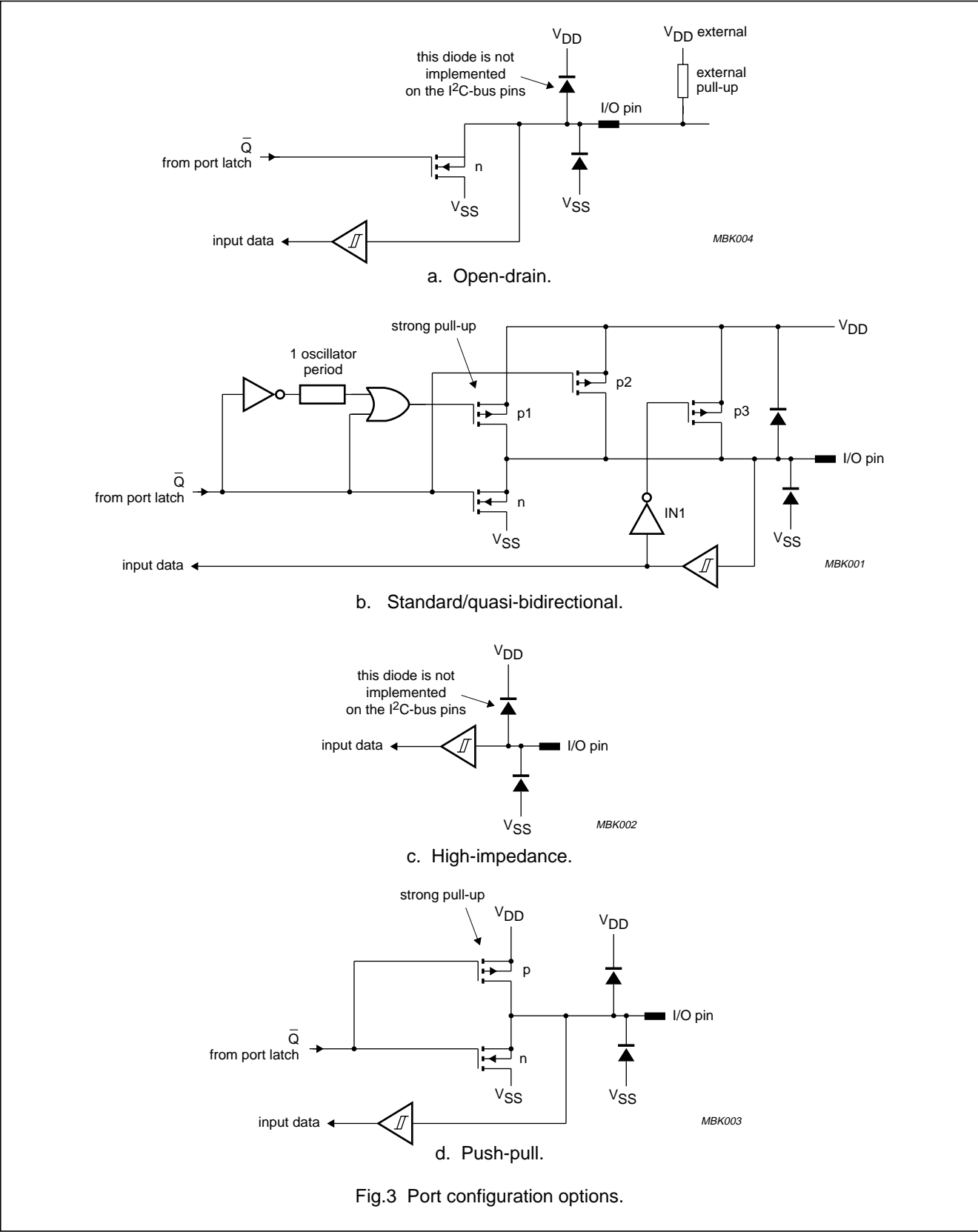
7	6	5	4	3	2	1	0
–	–	–	–	EMOUT0	ECLK	EMLDY	ETONE

Table 5 Description of ALTP bits

BIT	SYMBOL	DESCRIPTION
7 to 4	–	Reserved.
3	EMOUT0	If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	If this bit is set, the TONE output of the DTMF generator is enabled.

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6.3 Timer/event counters

The P8xCL883/P8xCL884 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $\frac{1}{6} \times f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{6} \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

- Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.
- Mode 1 16-bit time-interval or event counter.
- Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.
- Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

Note that the T0 input is only available on P8xCL883.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL883/P8xCL884 deviates from the timer T2 described in the "TELX family" data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the $\overline{C/T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timer T2 is incremented, the contents of the compare registers COMP2H and COMP2L is compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a chip reset will set the flag COMP. The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

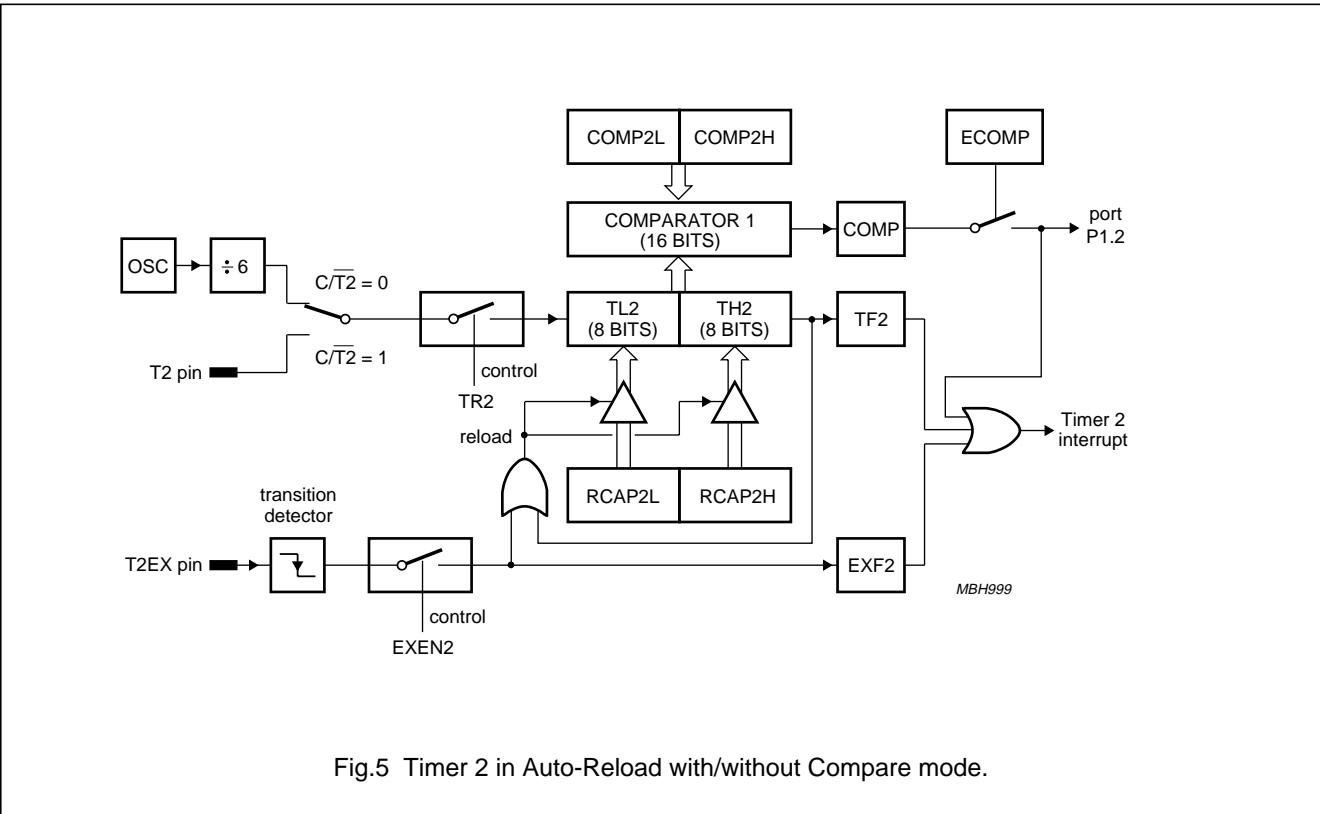
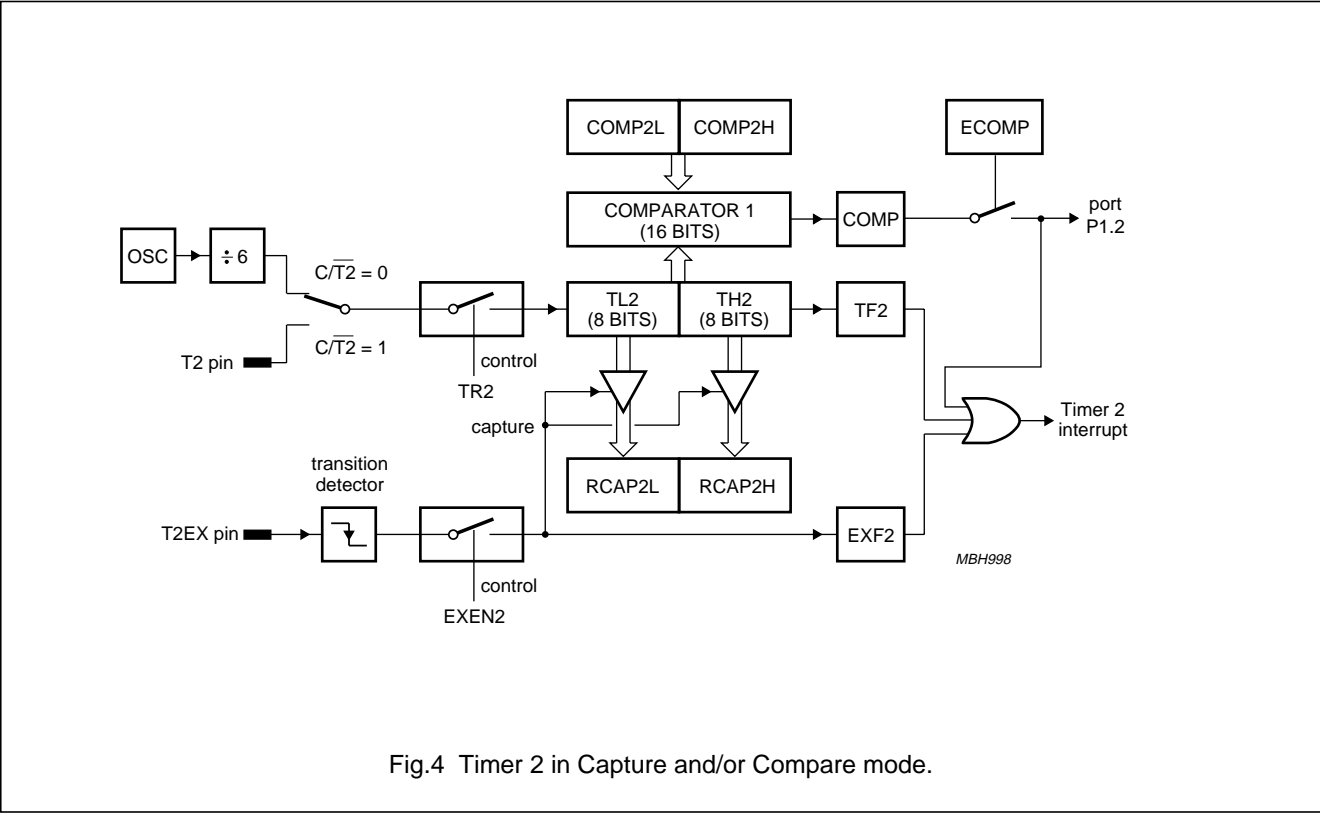
The Auto-reload mode can also be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, $\overline{CP/RL2}$ and TR2 in register T2CON.

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6.3.2 TIMER/COUNTER 2 CONTROL REGISTER (T2CON)

Table 6 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/T $\overline{2}$	CP/RL $\overline{2}$

Table 7 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	Timer 2 overflow flag. TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	Timer 2 external flag. EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	Interrupt flag. When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	Enable compare output bit. When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 start/stop control. Control bit for Timer 2.
1	C/T $\overline{2}$	Timer 2 timer or counter select. C/T $\overline{2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6} \times f_{osc}$. C/T $\overline{2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/RL $\overline{2}$	Capture/reload flag. When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 8 Timer 2 operating modes

ECOMP	CP/RL $\overline{2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

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6.4 MSK modem

For the P8xCL883/P8xCL884, MIN is no longer the alternative function of P4.0, but MIN is a separate pin. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer

The Watchdog Timer differs from the description in the "TELX family" data sheet in that the external \overline{EW} pin does not exist on the P8xCL883/P8xCL884.

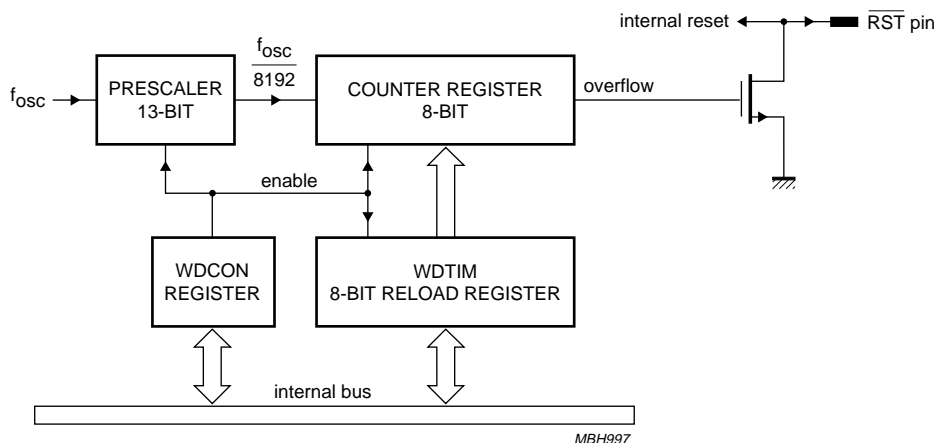


Fig.6 Functional diagram of the T3 Watchdog Timer.

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 8 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C5H, indicates P87CL883 and P87CL884

(060H) = 00H, currently not used.

6.6.1.2 Security

The following protection levels are available to protect TELX applications against software piracy and unwanted access to data stored in the application.

1. Preventing programming of an already programmed OTP. Note that security Level 1 also disables In System Programming.
2. Preventing the reading of program code in OTP by disabling access of the programmer to the Program Memory. Also verification of code during In System Programming is disabled. In this mode signature and security level verification is still possible.
3. This level has the same functionality as Level 2.

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Table 9 describes how these protections can be selected by programming the three least significant bits of the security byte.

Table 9 Security bits and levels of protection

BITS	LEVEL	DESCRIPTION
UUU	0	no security
UUP	1	Level 1 is activated
UPP	2	Levels 1 and 2 are activated
PPP	3	Levels 1, 2 and 3 are activated

6.6.2 IN SYSTEM PROGRAMMING MODE

In the In System Programming mode the OTP can be programmed under control of the CPU. A program to control programming has to be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In System Programming four SFRs are used to control the OTP.

Table 10 SFRs for In System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In System Register

6.6.2.1 OTP In System Programming Register (OISYS)

The OISYS SFR controls the In System Programming mode. The data that has to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 11 OTP In System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	SEC	SIG	WE	InSysMode

Table 12 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	Reserved.
4	VPon	V _{PP} status (read only).
3	SEC	Security bits enable.
2	SIG	Signature bytes enable.
1	WE	Write Enable, enables programming.
0	InSysMode	In System Programming status bit.

6.6.2.2 Mode entry

The In System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I²C-bus is used for data transfer in this mode. If the I²C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I²C-bus interrupt.

If high voltage is present the In System Program interrupt routine has to start that writes the InSysMode bit (OISYS.0) and controls the address and data transfer.

Note that this paragraph is only applicable for the first series, it can be neglected in the future. During In System Programming the OTP memory has to be in DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In System Programming mode is left 00H has to be written into the OTEST SRF.

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The program voltage has to be available and stable for at least 10 μ s before the mode is entered and has to be stable until the circuit has left the In System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.3 Program cycle

The data and address have to be supplied to the microcontroller and the control program has to write the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 μ s cycle and the WE bit of the OISYS SFR has to be set. Now the core has to be set into Idle mode. As long as the circuit is in idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 8 kbytes address space.

6.6.2.4 Verify for In System Programming

Verify is done in similar way as programming. The circuit is put into idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 μ s. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in a normal way. To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.5 Signature bytes and security

The signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes (and other test addresses) are always readable independent of the security.

Security has the same meaning as in Parallel Program mode. Security can be programmed and verified by setting the SEC bit of the OISYS SFR. The security bits can be programmed like normal bits. To program Level 1, 01H has to be loaded in the ODATA SFR. These values are 03H and 07H for Level 2 and Level 3 respectively. The SEC bit of the OISYS SFR has to be HIGH during the program cycle. Loading an address is not necessary. The timer has to be initialized for a 200 μ s instead of 100 μ s for security or two standard pulses have to be applied. If the SEC bit is HIGH during verify, the security bits can be read from the ODATA SFR. Verifying a normal address while security level - Level 2 or Level 3 - has been programmed will result in reading 00H.

Verifying is disabled immediately after programming Level 2 or Level 3. Programming is disabled if a verify or a reset is applied after programming security level: Level 1 or higher.

6.6.2.6 How to connect the PORENABLE/ V_{PP} pin in the In System Programming mode

If the V_{PP} pin is dual-mode (e.g. PORENABLE/ V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13 V**, i.e. cannot have clamping diodes or low bread-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.7.

In the example (see Fig.7) the POR is enabled in normal mode of operation (pin PORENABLE/ V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee min. 12.5 V on the PORENABLE/ V_{PP} pin.

Note that if in the application the Power-on-reset is disabled (pin PORENABLE/ V_{PP} = 0), applying a high voltage to the PORENABLE/ V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

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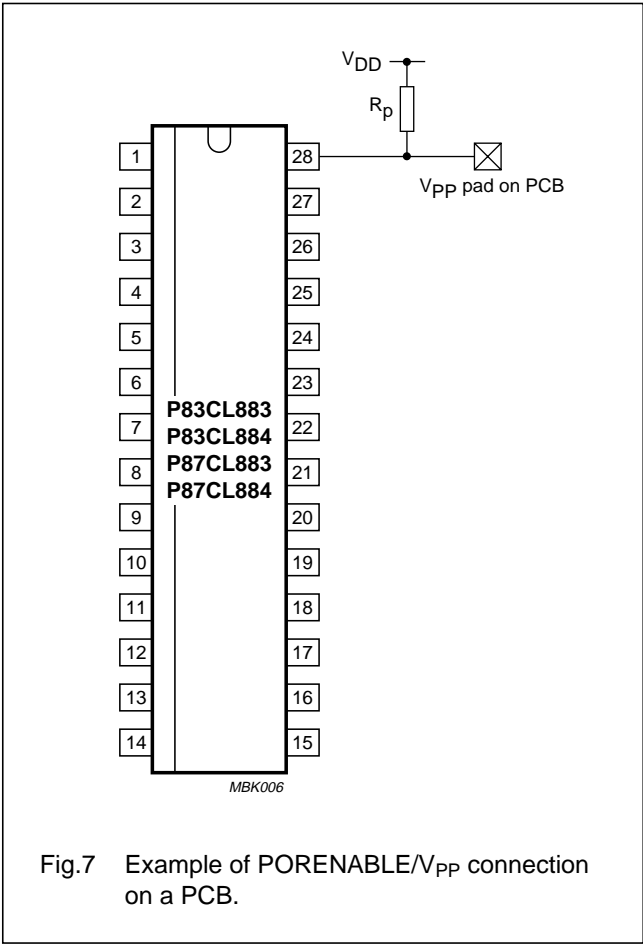


Fig.7 Example of PORENABLE/ V_{PP} connection on a PCB.

6.7 Oscillator circuitry

General information on the oscillator circuitry can be found in the “TELX family” data sheet.

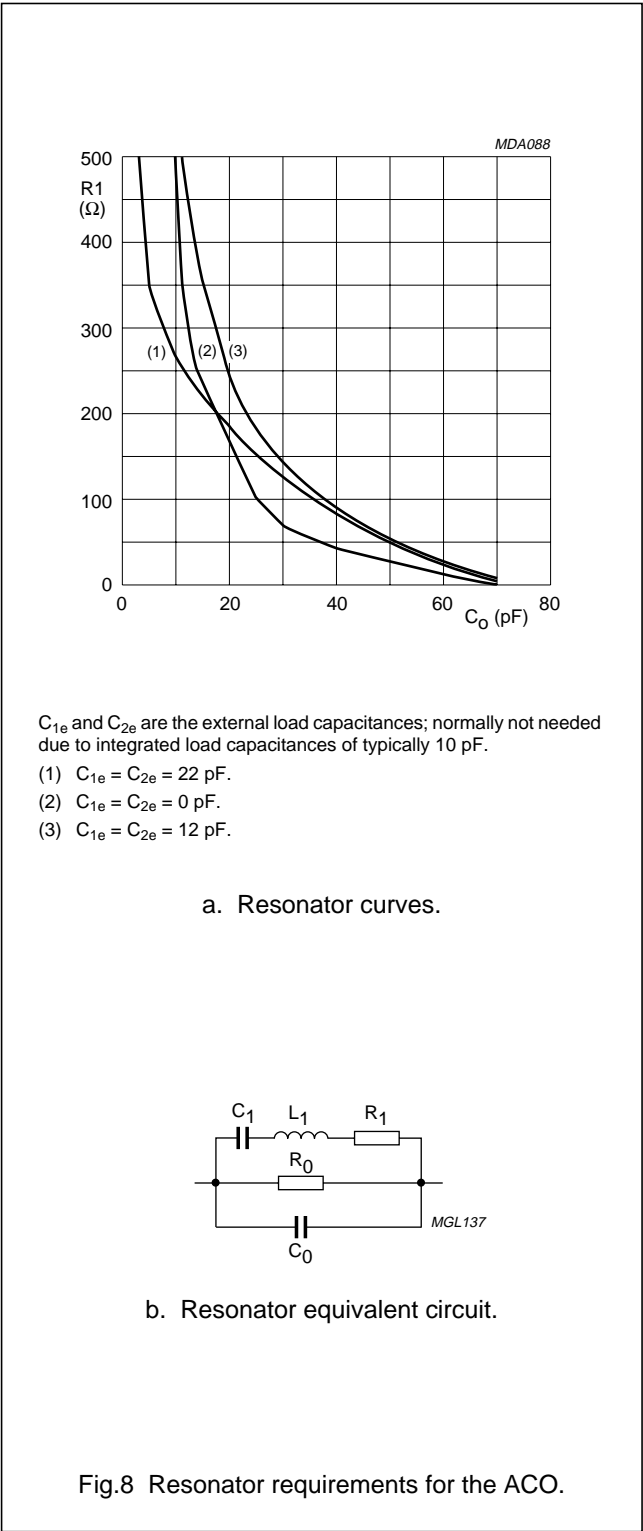
6.7.1 RESONATOR REQUIREMENTS

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 k Ω .

The wiring between chip and resonator should be kept as short as possible.

6.7.2 RECOMMENDED RESONATOR TYPES

- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).



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6.8 Emulation

The emulator for the P8xCL883/P8xCL884 uses the P87CL880 microcontroller in emulation mode.

The P87CL880 is a super-set of the P8xCL883/P8xCL884, i.e. it contains all the functions of the P8xCL883/P8xCL884 plus a number of other additional functions. It should be noted that some functional differences between P87CL880 and P8xCL883/P8xCL884 exist; see Table 13.

Table 13 Differences between functions existing in P87CL880 and P8xCL883/P8xCL884

FUNCTION	P87CL880	P8xCL883/P8xCL884
Timer 2	see P87CL880 specification	see P8xCL883/P8xCL884 specification
OTP Program Memory	32 kbytes AFROM	8 kbytes EPROM or pre-programmed ROM
RAM	512 bytes	256 bytes
$\overline{\text{EW}}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL883/P8xCL884 specification
In System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL883/P8xCL884 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Package	QFP64	SO28

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6.9 Read-Modify-Write bug

The first versions of P8xCL883/P8xCL884 and P87CL880 contain a bug which affects all instructions of type Read-Modify-Write (RMW) to an I/O port.

The instructions affected are: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV Px.y,C, CLR Px.y and SET Px.y. The detailed explanation of the normal function of these instructions are explained in the *"Data Handbook IC20; 80C51-based 8-bit Microcontrollers"*.

The ports affected are P0, P1 and P3 on P8xCL883/P8xCL884, and ports P0 and P3 on P87CL880. Normally, a RMW instruction first reads the value which is present on the port latch (not the state of the port pins), modifies this value, and writes it back to the port latch.

Due to a critical timing between two internal signals in the present design, the RMW instructions do not work correctly. Due to the bug, the RMW instructions on the port pins should be avoided. However, a software workaround exist.

Instead of using the normal RMW instruction, each manipulation should be done on a copy-byte of the port latch (e.g. a bit addressable RAM byte for each port), and thereafter the new value of the copy-byte should be written to the port latch. It is important that any value to be written to a port must be copied in the copy-byte, see the example in Section 6.9.1 "Example 1: Writing 'directly' to a port".

6.9.1 EXAMPLE 1: WRITING 'DIRECTLY' TO A PORT

Normally:

```
MOV P1,#53h           ;write value directly to port
```

Work-around:

```
MOV Plcopy,#53h       ;write value to copy-byte
MOV P1,Plcopy          ;write value of copy-byte to port
```

6.9.2 EXAMPLE 2: SETTING ONE BIT OF THE PORT

Normally:

```
SET P1.0              ;set bit 0 of port P1
```

Work-around:

```
SET Plcopy.0          ;set bit 0 of port Plcopy, assuming register Plcopy is chosen to
                        ;be in the bit addressable RAM area
MOV P1, Plcopy         ;write value of copy-byte to port
```

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DD}	supply voltage	-0.5	+4.0	V
V _I	input voltage on any pin with respect to ground (V _{SS})	-0.5	V _{DD} + 0.5	V
P _{tot}	total power dissipation	—	800	mW
T _{stg}	storage temperature	-65	+150	°C

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8 CHARACTERISTICS

$V_{DD} = 2.7$ to 3.6 V; $V_{SS} = 0$ V; $f_{xtal} = 3.58$ MHz; $T_{amb} = -25$ to $+70$ °C;

T_{amb} (during In System Programming) = $+20$ to $+40$ °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	–	3.6	V
	operating		1.0	–	3.6	V
	RAM data retention in Power-down mode		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	$V_{DD} = 3$ V; note 1	–	–	2.0	mA
		$V_{DD} = 3$ V; $T_{amb} = 25$ °C; note 1; see Fig.10	–	1	–	mA
$I_{DD(id)}$	supply current Idle mode	$V_{DD} = 3$ V; note 2	–	–	0.55	mA
		$V_{DD} = 3$ V; $T_{amb} = 25$ °C; note 2; see Fig.11	–	0.26	–	mA
$I_{DD(pd)}$	supply current Power-down mode	$V_{DD} = 3$ V; $T_{amb} = 25$ °C; note 3; see Fig.12				
		POR and LVD enabled	–	2	5	μA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	$V_{DD} = 3$ V; $T_{amb} = 25$ °C; notes 4 and 5				
	EEPROM erase/write		–	460	–	μA
	DTMF	no load on TONE output	–	240	–	μA
	MSK modem		–	140	–	μA
	Watchdog		–	110	–	μA
	I ² C-bus		–	90	–	μA
	UART		–	90	–	μA
	Timer T2		–	90	–	μA
	Timer T0 or T1		–	5	–	μA
Inputs (Ports, MIN, RST, MOUT0 to MOUT2, PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$ I_{IL} $	LOW-level input current (ports in Mode 1)	$V_{IN} = 0.4$ V; note 8; see Fig.9	–	10	50	μA
$ I_{IL(T)} $	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.9	–	200	1000	μA
$ I_{LI} $	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Port outputs (Ports, $\overline{\text{RST}}$, MOUT0 to MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	$V_{OL} = 0.4 \text{ V}$	2	–	–	mA
I_{OL1}	LOW-level output current; P1.3 (for LED)	$V_{OL} = 0.4 \text{ V}$	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	$V_{OL} = 0.4 \text{ V}$; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4 \text{ V}$	2	–	–	mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4 \text{ V}$	6	–	–	mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4 \text{ V}$	3	–	–	mA
$I_{\overline{\text{RST}}}$	$\overline{\text{RST}}$ pull-up transistor current	$V_{DD} = 3 \text{ V}$; $V_{OH} = V_{DD} - 0.4 \text{ V}$	5	20	–	μA
		$V_{DD} = 3 \text{ V}$; $V_{OH} = V_{SS}$	–	50	200	μA
Power-on-reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on-reset trip level HIGH	option 5 in “TELX family” specification	2.13	2.37	2.61	V
V_{PORL}	Power-on-reset trip level LOW	option A in “TELX family” specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.13)						
$V_{HG(rms)}$	HGF voltage (RMS)	$V_{DD} = 3 \text{ V}$	158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	$V_{DD} = 3 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; notes 5 and 12	–	25	–	dB
EEPROM (notes 5 and 13)						
$t_{E/W}$	erase/write time		8	10	12	ms
$N_{E/W}$	erase/write cycles		10^5	–	–	
t_{DR}	data retention time	$T_{amb} = +70 \text{ }^\circ\text{C}$	10	–	–	years
In System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	μs
$t_{prog(security)}$	program cycle time security	note 14	180	200	220	μs
t_{ver}	verify cycle time		1	–	–	μs
$t_{Vpp(setup)}$	program voltage setup time		10	–	–	μs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{Vpp}	program voltage current	In System Programming	–	–	40	mA

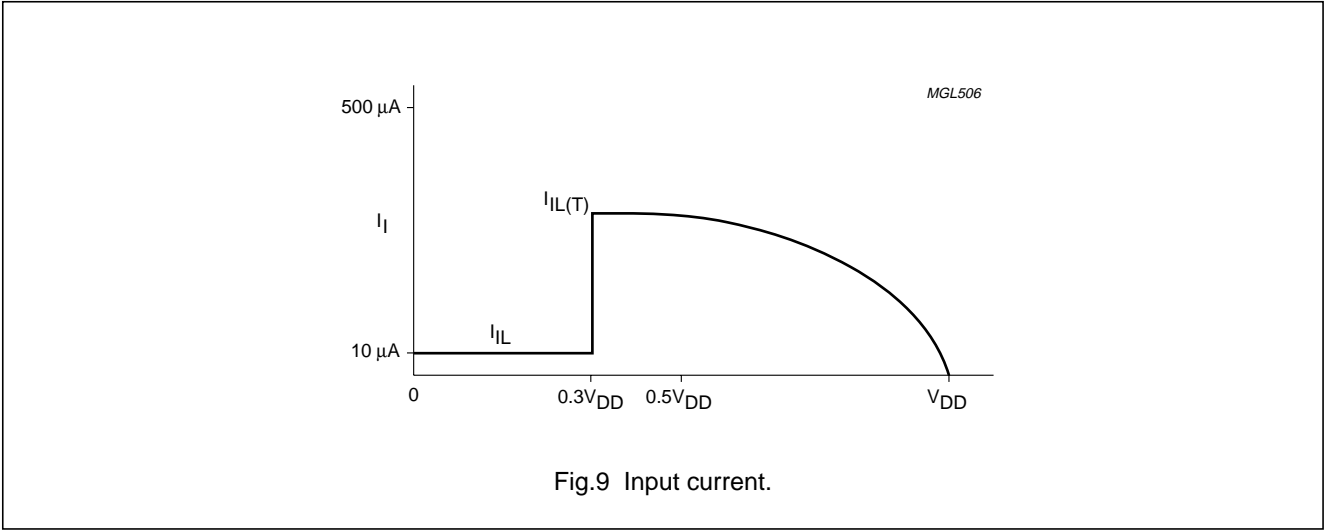
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ACO (Amplitude Controlled Oscillator)						
V _{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V _{DD}	mV
Z _{i(XTAL1)}	input impedance on XTAL1		300	1000	–	kΩ
C _{1i} ; C _{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 15	–	10	–	pF

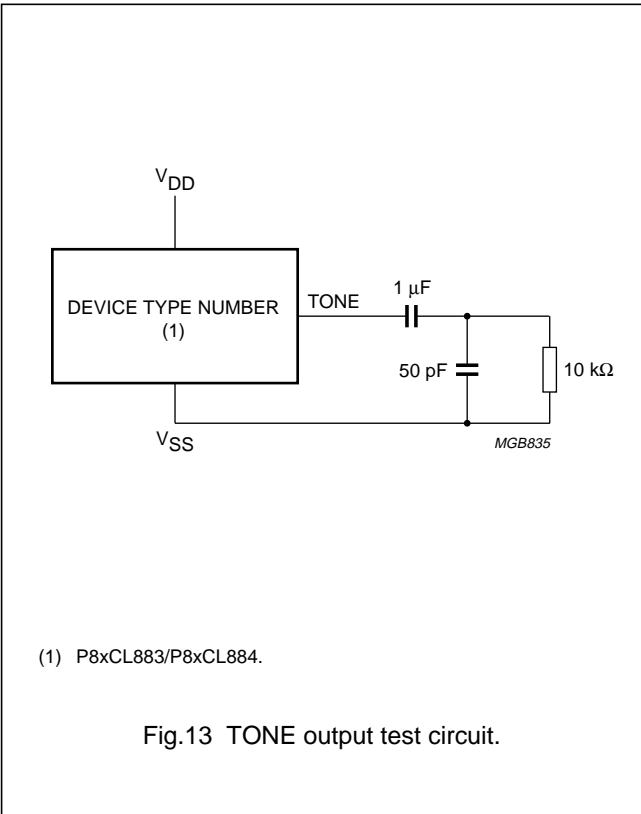
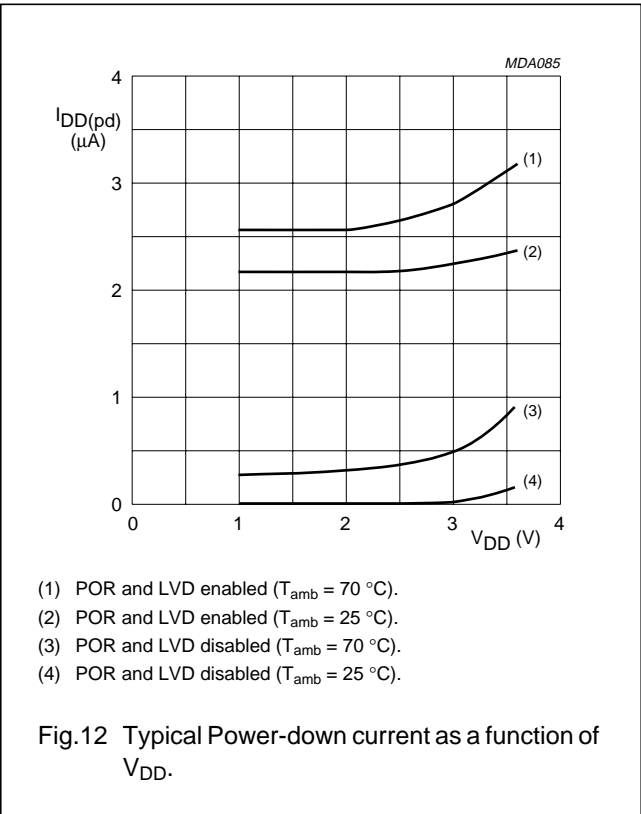
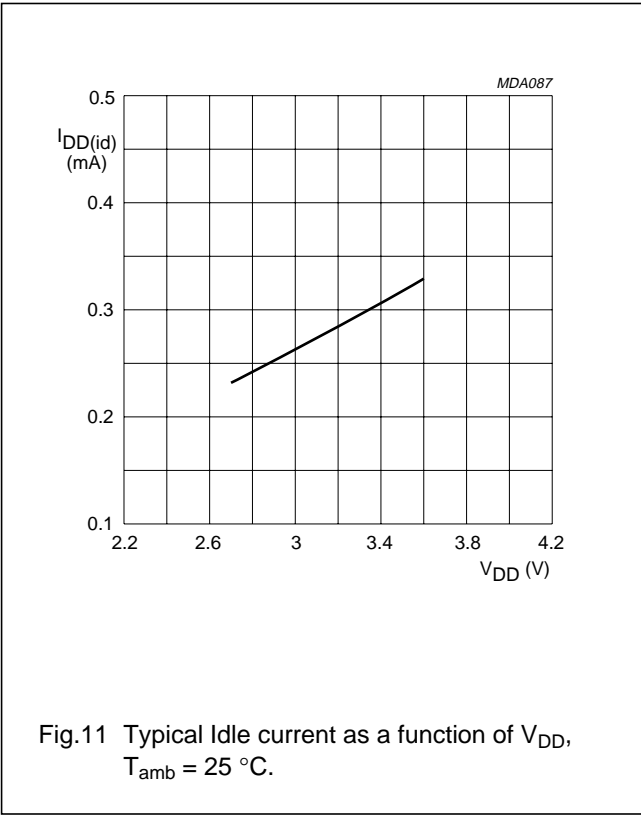
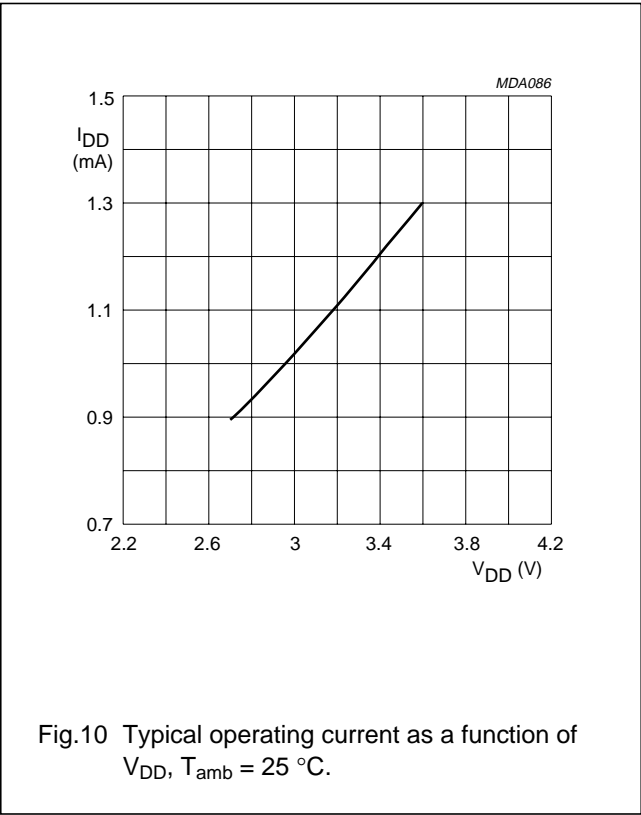
Notes

1. The operating supply current is measured with all output pins disconnected; V_{IL} = V_{SS}; V_{IH} = V_{DD}; $\overline{\text{RST}}$ = V_{DD}; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{\text{RST}}$ disconnected; V_{IL} = V_{SS}; V_{IH} = V_{DD}; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{\text{RST}}$ disconnected; V_{IL} = V_{SS}; V_{IH} = V_{DD}; XTAL1 and XTAL2 not connected;.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (1 + 0.11 + 0.09) mA = 1.2 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I²C-bus specification. Therefore, an input voltage below 0.3V_{DD} will be recognized as a logic 0 and an input voltage above 0.7V_{DD} will be recognized as a logic 1.
7. For pin PORENABLE the V_{IL(max)} = 0.1V_{DD}.
8. Not valid for pins SDA, SCL, $\overline{\text{RST}}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the specification in the data sheet “TELX family; Chapter: Low Voltage Detection”.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. After final testing the value of each EEPROM bit is typically logic 1.
14. Can also be done by two 100 μs pulses.
15. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance, leadframe capacitance).



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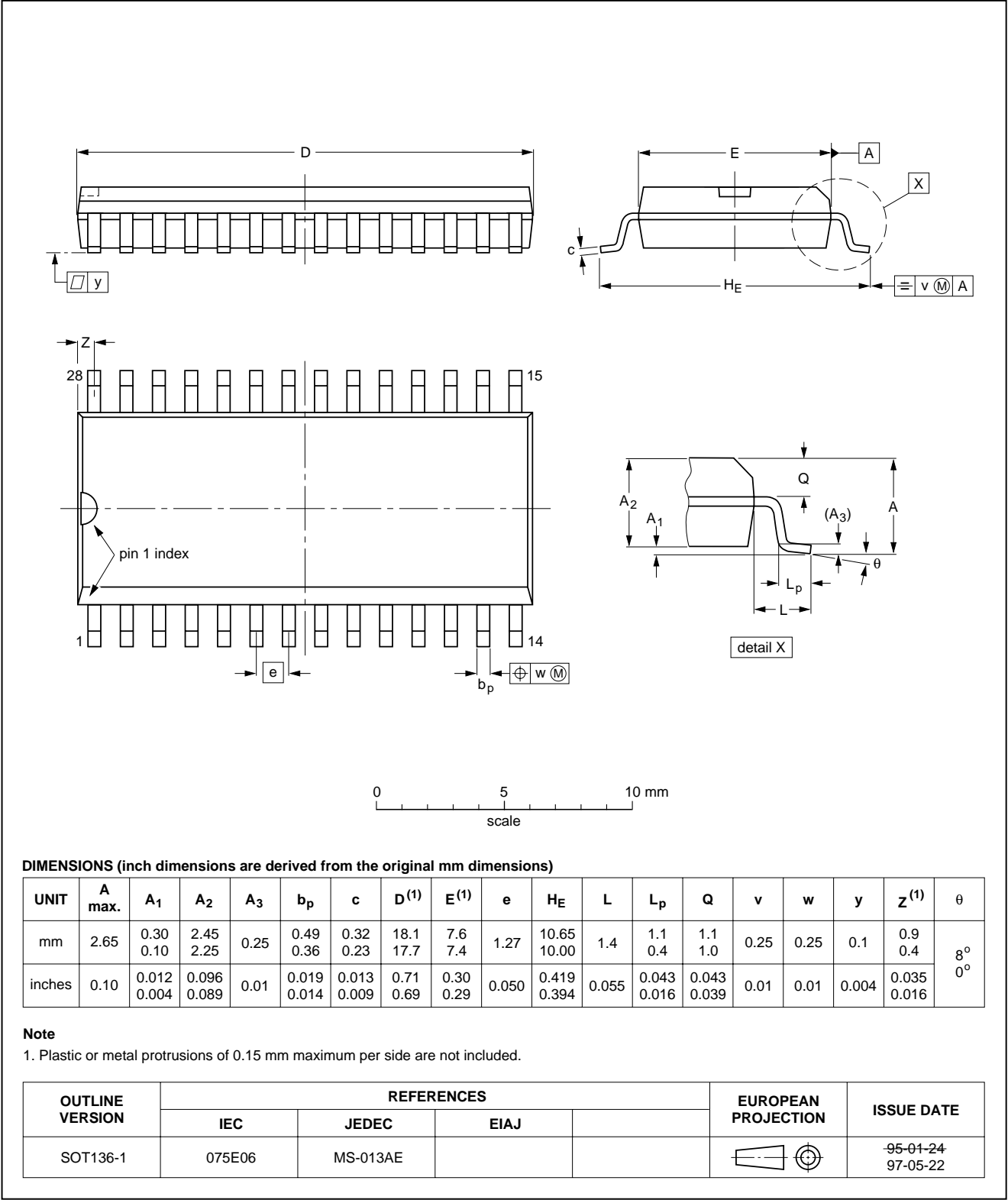
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9 PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1



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10 SOLDERING

10.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

10.2 Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

10.3 Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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11 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

12 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

13 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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NOTES

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NOTES

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